TI + Oregano PTP stack features

2024-08-19

LMK5B/5C33xxx(A)

LMK5B/5C33xxx(A)-S1

What makes Oregano PTP stack special?

- Accuracy in the ns range
- Meets all telecom specifications for class D end devices
- syn1588® technology
  - Most versatile PTP Stack available (both commercial and open source)
  - Widely deployed in many industries
  - +30 technology licenses
  - +500 customers using syn1588® NIC
  - >> 10.000 Meinberg PTP Grandmasters in the field using syn1588® technology
  - Continuous support and development

Oregano expertise

- Active in the clock synchronization industry since more than 20 years
  - Advanced expertise on all aspects of PTP
  - Customers in all application domains
  - Participate in several related standardization committees (SMPTE, IEEE)
- PTP stack deployed to several architectures
  - Intel, ARM, etc.
- IP cores
  - Video clocking (HSYNC, VSYNC)
- Released Networking Products
  - PCIe NIC
  - Gigabit ethernet switch

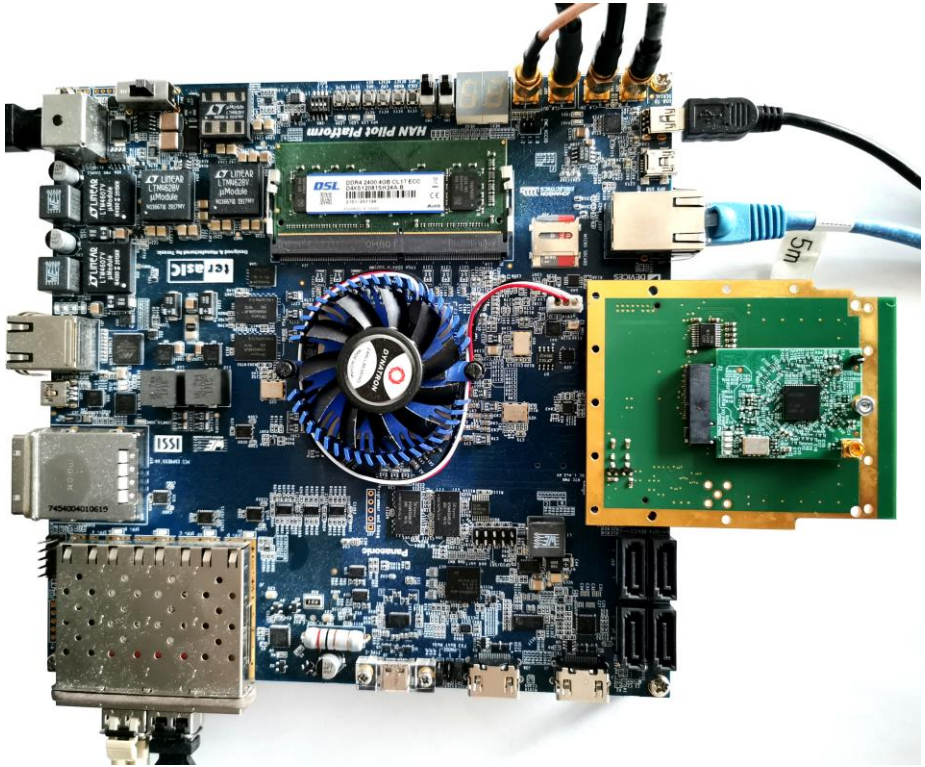
Oregano Success Stories

- Check Oregano System Website for release notes on PTP Stack
  - https://www.oreganosystems.at/downloads/syn1588r-software-suite-release-notes
- Meinberg PTP Grandmasters synchronized the Superbowl and the Oscars
  - https://www.linkedin.com/posts/game-creek-video_meinberg-ptp-synchronize-activity-7041829775690100736-HTrF/
- Numerous publications in journals and at conferences
  - IEEE Transactions
  - SMPTE Technical Journal
  - NAB BEITC – Broadcast Engineering and IT Conference
  - EBU Technical journals
  - Broadcast beat
- Full publication list available upon request

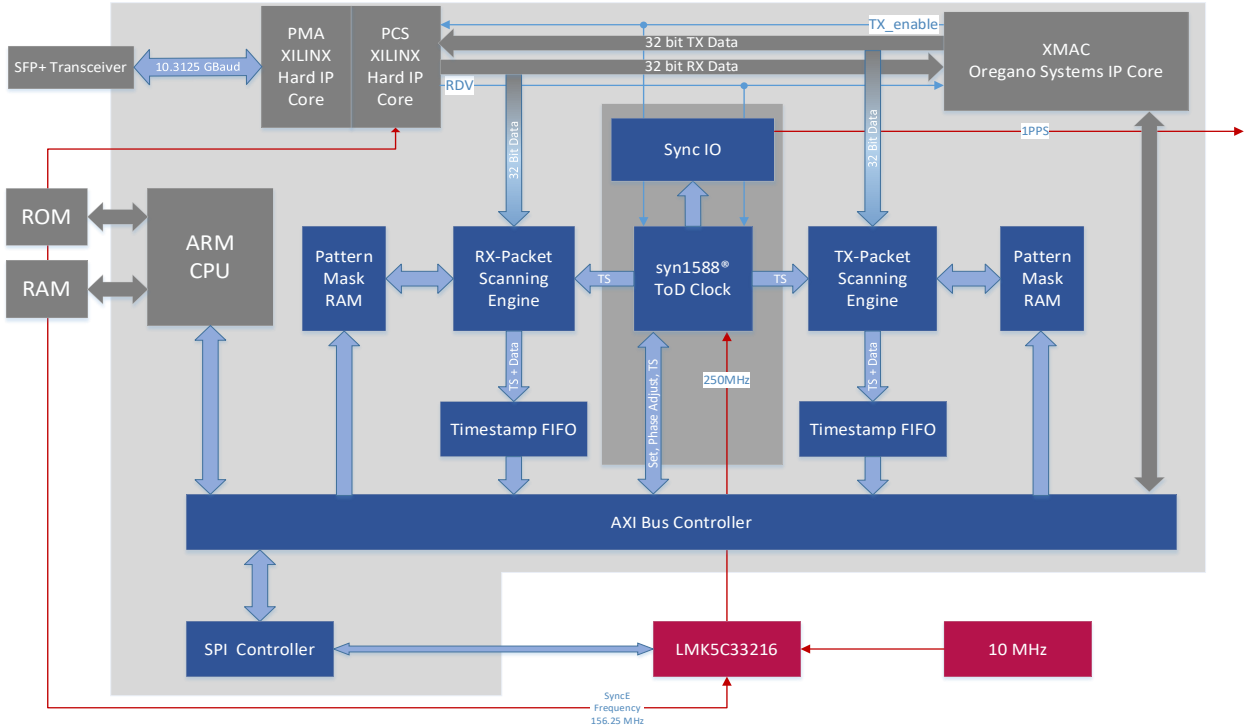
Demos of TI clocking devices with Oregano PTP stack

- LMK family of Network Synchronizer devices provide
  - Extremely high resolution for DCO adjustment
  - SyncE support
  - Hitless switchover
  - Ability to generate frequencies derived from and thus phase locked to absolute time
- Demo systems
  - Intel ARRIA 10
    - syn1588® technology ported to FPGA EVM (INTEL ARRIA10) with LMK daughterboard
    - Calnex measurement reports made with the demo system (add link to app note)
  - Texas Instruments AM64x Sitara
    - Operation on SK-AM64B EVK with modification for connection to LMK5B33216EVM.
    - To become single board TI PTP clocking reference design.

Intel ARRIA 10 demo setup



Block Diagram Arria 10 FPGA with syn1588 IP Core and MAC



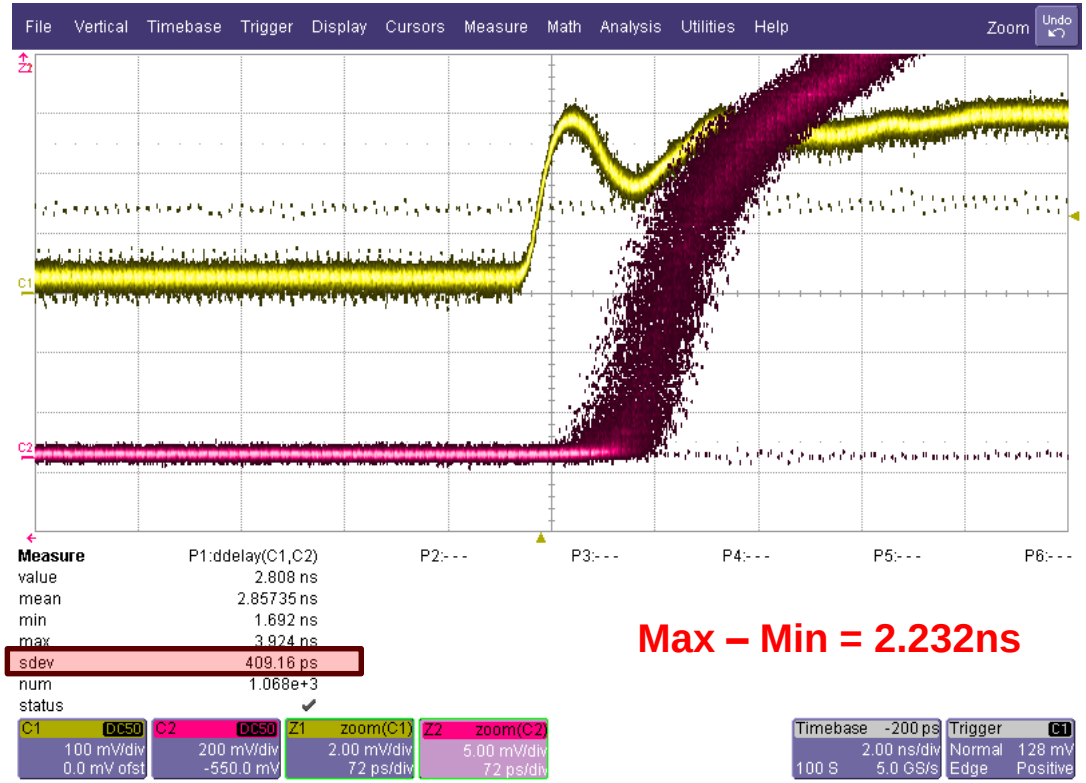
G.8275 G.8262 Compliance Test Results Summary

- The G8275.1 implementation using the LMK5B/C33xxx(A) network synchronizer to adjust the frequency of the PTP hardware Time-of-Day clock complies with telecom accuracy Class A (100 ns), Class B (70 ns), Class C (30 ns), **and even Class D.**
  - **For full timing support 1PPS signal did not deviate more than ±5 ns**

- For G.8271.2 networks with partial timing support, the configuration of the PTP stack was optimized to handle PDVs in excess of 230 µs while staying within the requested boundaries of ±1.5 µs with a headroom of 500 ns.

- For G.8262.1 SyncE networks the short term phase transients fall well within the allowable limits

DSO Results Comparing 1 PPS Signals



Max – Min = 2.232ns

8273.2 Noise Generation Specification summary

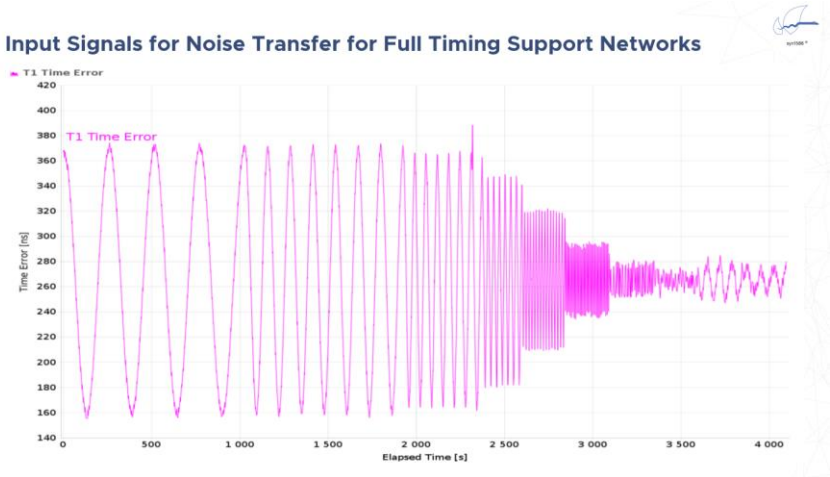
T-BC/T-TSC Class	max|TE| (ns)	max|TE_L| (ns)	cTE (ns)	dTE_L MTIE < 1000 s T = ±1 ºC (ns)	dTE_L TDEV < 1000 s T = ±1 ºC (ns)	dTE_H (ns)	
A	100	-	±50	40	4	70	
B	70	-	±20	40	4	70	
C	30	-	±10	10	2	FFS	
D	FFS	5	FFS	FFS	FFS	FFS	

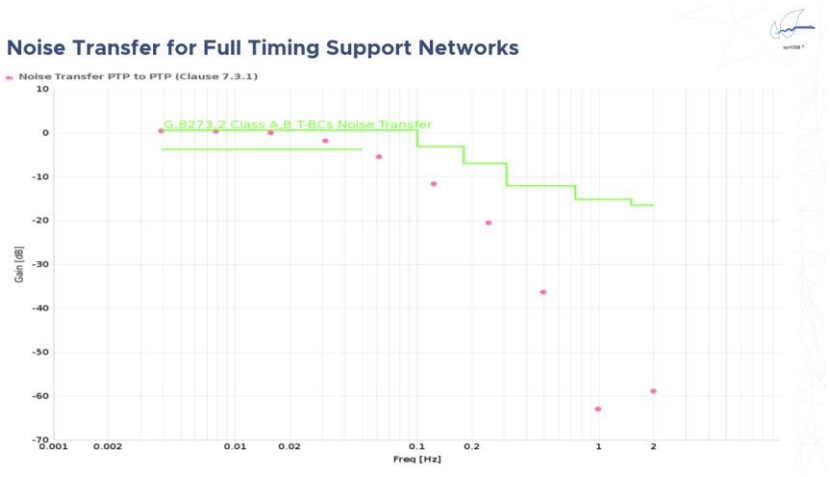
TE = Maximum absolute time error
TE_L = Maximum absolute time error low-pass filtered
cTE = Permissible range of constant time error
FFS = For further study

Oregano Data for:
G.8273.2 Class A, B T-BCs Noise Transfer

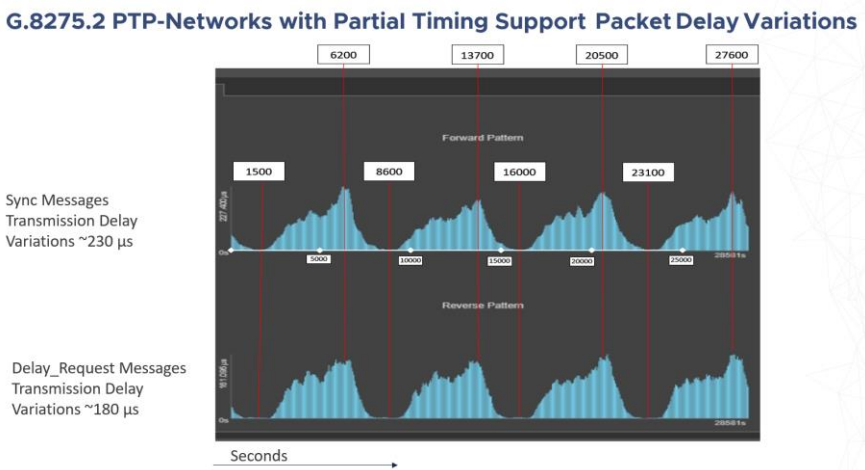
Input T1 Time Error for plot →

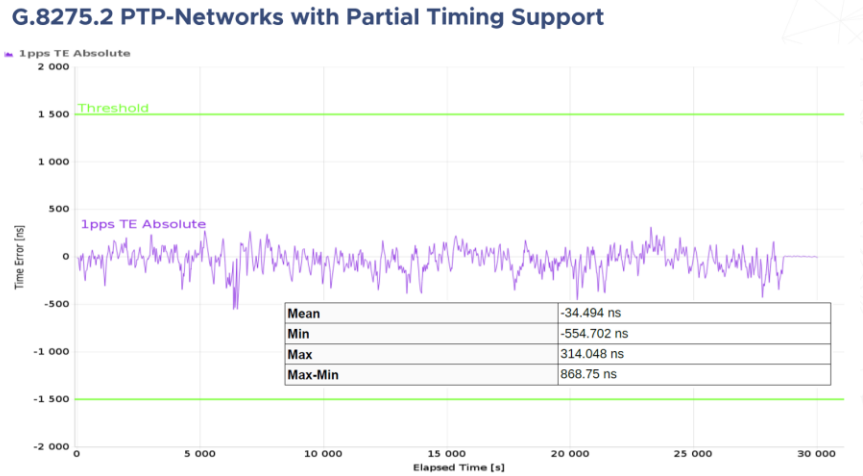
Noise transfer result with T1 time error modulated





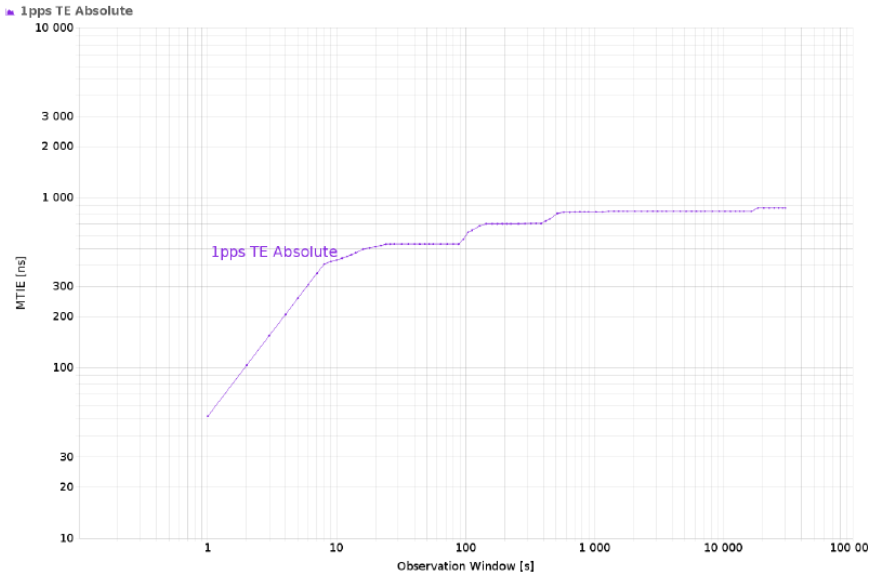
Oregano Data for:
G.8275.2 Class A, B T-BCs Noise Transfer





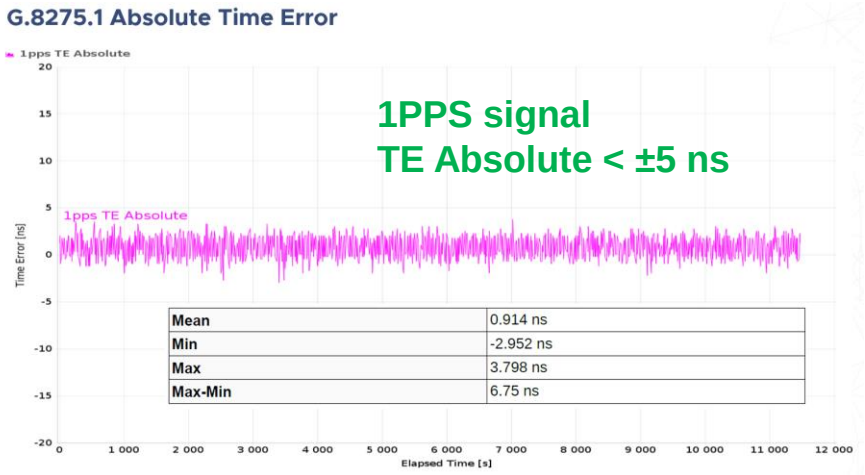
G.8275.2 Partial Timing Support MTIE

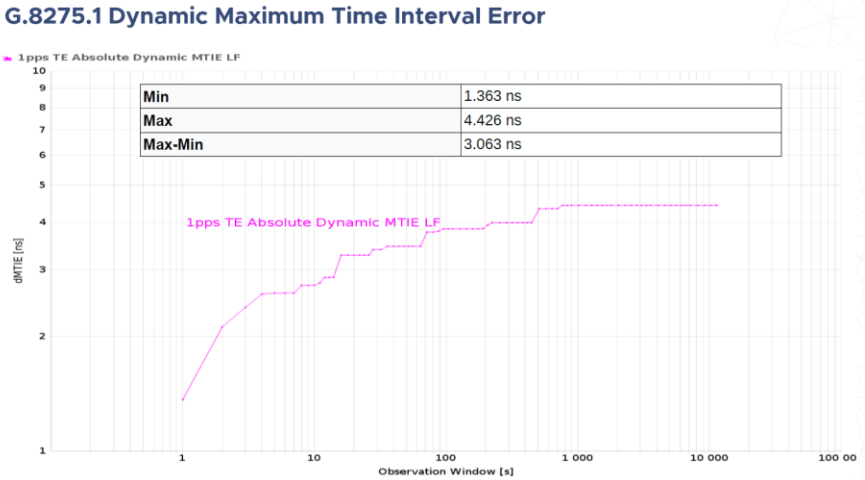
MTIE Analysis



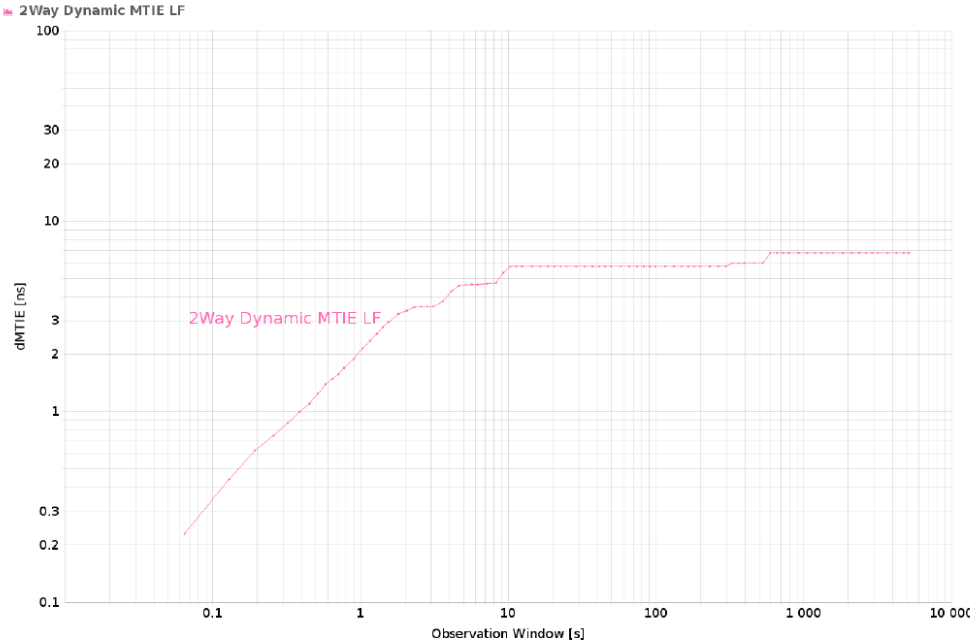
Min	52 ns
Max	868.75 ns
Max-Min	816.75 ns

Oregano Data for:
G.8275.1 T-BC Time Error Absolute (no filter)



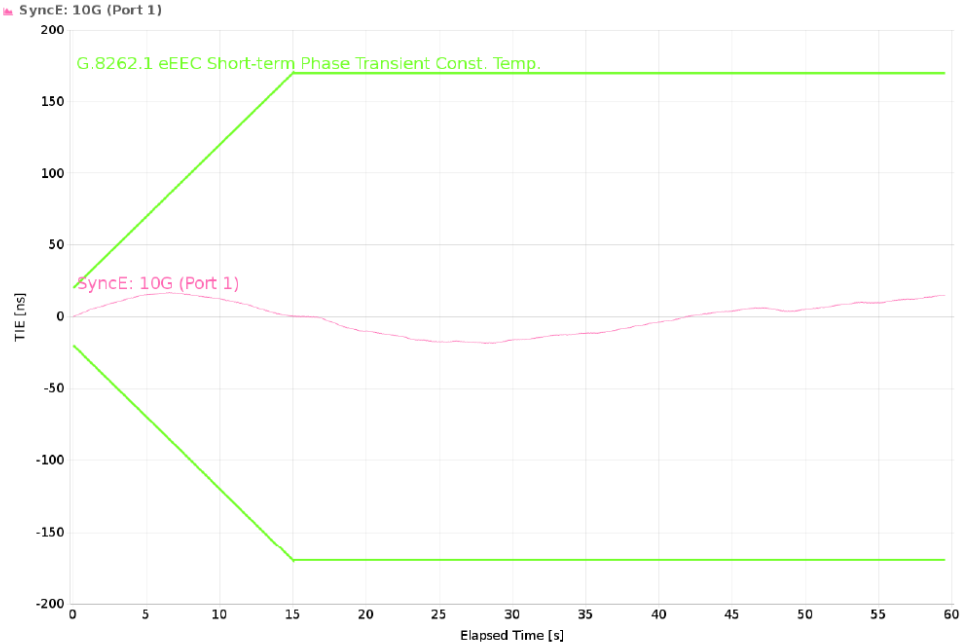


G.8275.1 T-BC Two-Way Dynamic MTIE



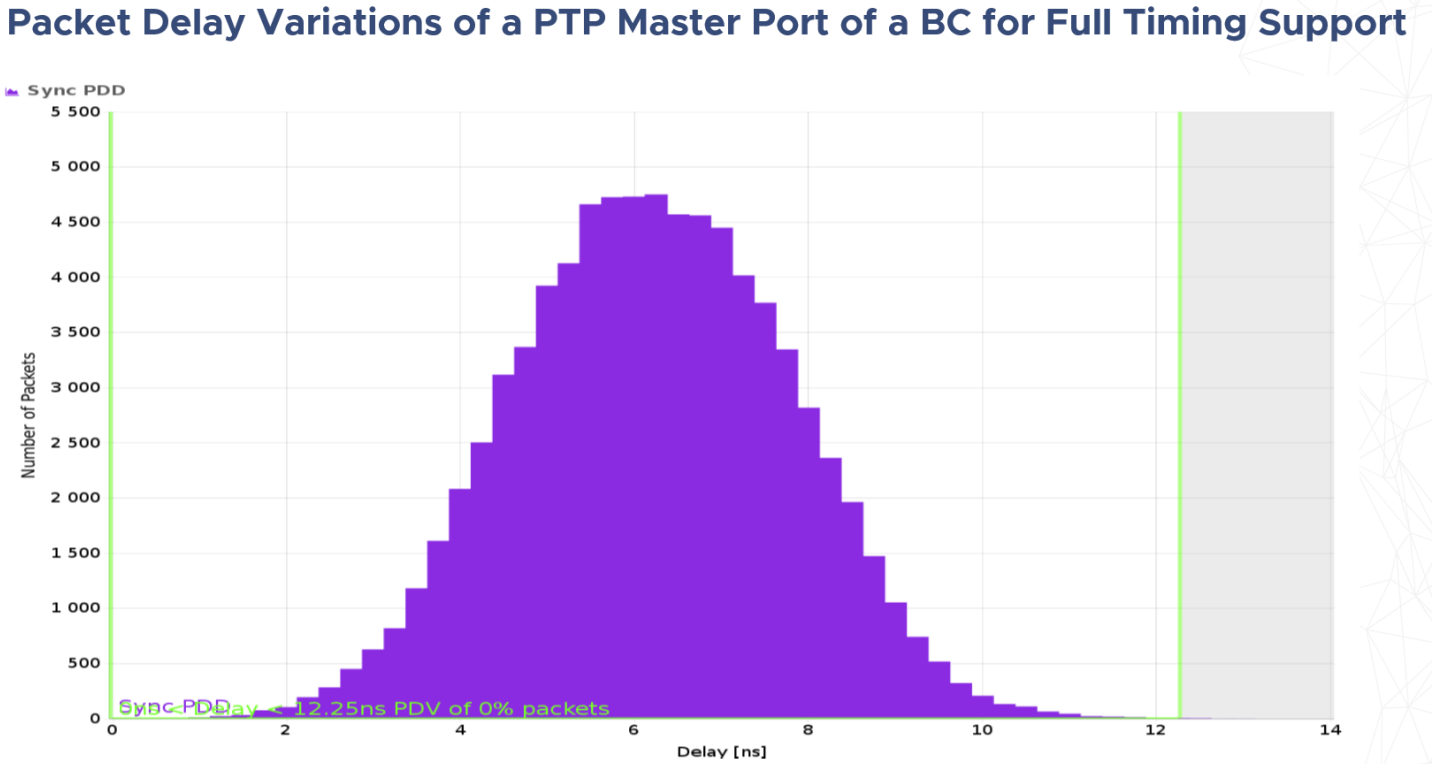
Min	0.229 ns
Max	6.813 ns
Max-Min	6.584 ns

G.8262.1 SyncE Short Term Transient



Mean	18.119 ns
Min	0 ns
Max	33.074 ns
Max-Min	33.074 ns
Rate	30.00/second

Packet Delay Variations of a PTP Master Port of a BC for Full Timing Support



Test Results

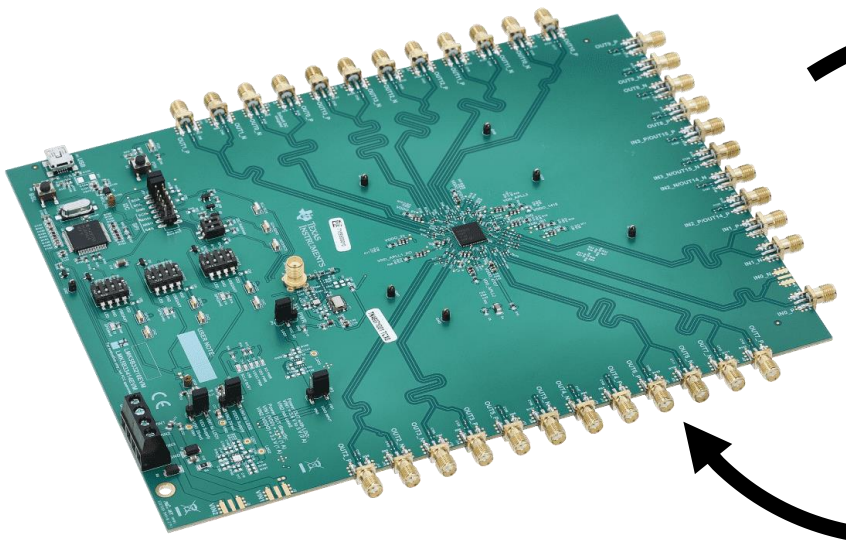
- The combined PTP solution fulfils all ITU telecom test specifications
  - Ordinary Clock & Boundary Clock
  - Full & partial timing support
  - 50% headroom to most stringent boundaries
- **Class D** performance reached
- **Test were made with industry standard equipment (Calnex Neo)**

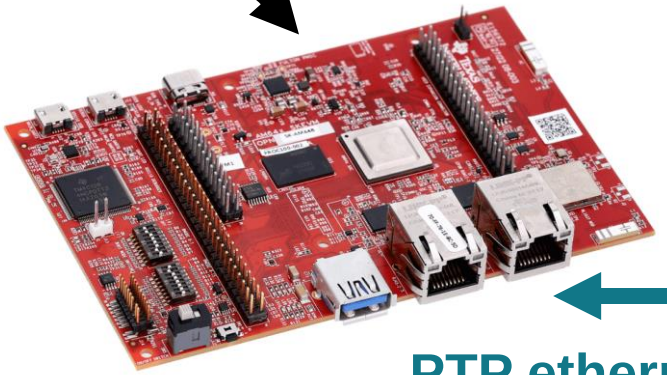
Firmware resource utilization example

- FPGA design with 2 Ethernet ports and full PTP
  - Family: Arria 10 Device: 10AS066K3F40E2SG
  - Final Logic utilization (in ALMs): 33,223 / 251,680 (13 %)
  - Total registers: 55308 Total pins: 464 / 864 (54 %)
  - Total block memory bits: 5,402,112 / 43,642,880 (12 %)
  - Total RAM Blocks: 364 / 2,131 (17 %)
  - Total DSP Blocks: 0 / 1,687 (0 %)
  - Total HSSI RX channels: 2 / 36 (6 %)
  - Total HSSI TX channels: 2 / 36 (6 %)
  - Total PLLs: 10 / 80 (13 %)

TI AM64 demo setup

LMK5B33216 provides clock for AM64 and ethernet PHYs





PTP ethernet traffic

AM64 sends DCO commands to servo LMK5B frequency to align AM64 hardware ToD clock

Purchasing the -S1 option LMK devices includes

- Execution of the "Standard Path"
- 40 hours of support for you as customer from Oregano Systems which includes
  - Consulting to optimize system architecture
  - Basic training on PTP
  - Design-in support
  - Network topology aspects with respect to PTP

Do you want to know more?

- Let us know…
  - Your application market
  - Your system requirements
  - Your hardware environment

- And we can discuss how the TI clocking + Oregano PTP stack solution can work for you.