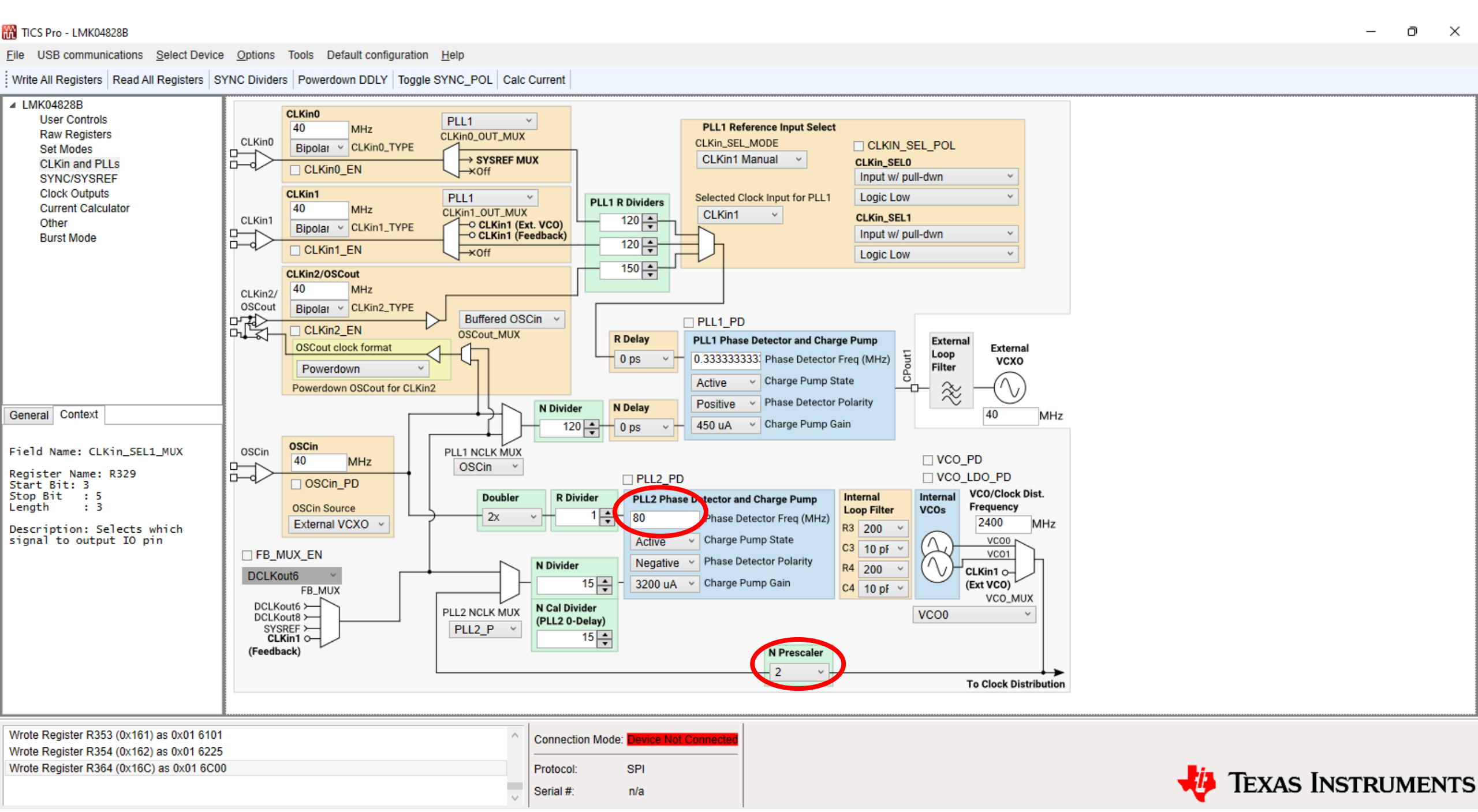
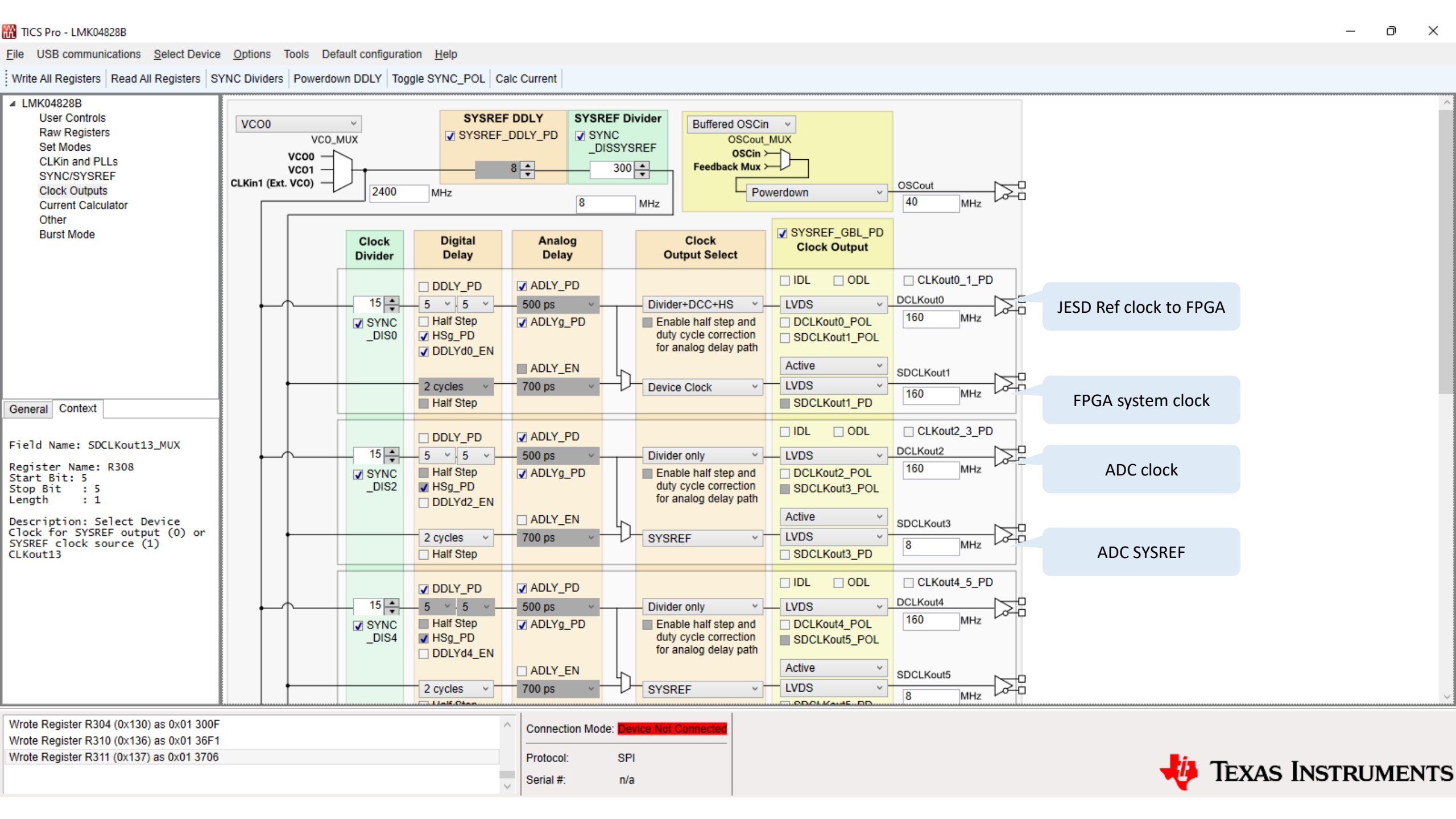
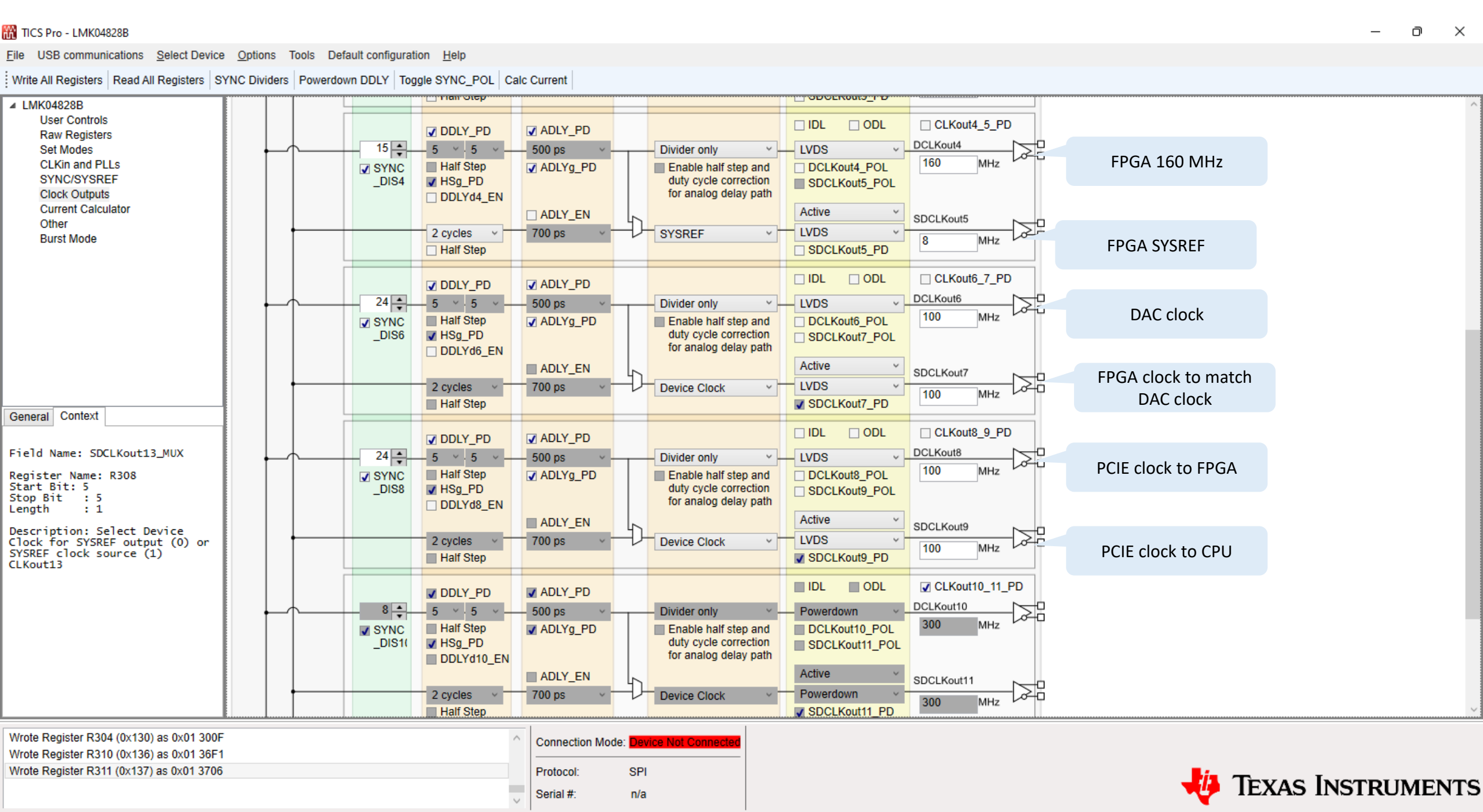

TICS Pro - LMK04828B
File
USB communications
Select Device
Options
Tools
Default configuration
Help
Write All Registers
Read All Registers
SYNC Dividers
Powerdown DDLY
Toggle SYNC_POL
Calc Current
LMK04828B
User Controls
Raw Registers
Set Modes
CLKin and PLLs
SYNC/SYSREF
Clock Outputs
Current Calculator
Other
Burst Mode
General
Context
Field Name: CLKin_SEL1_MUX
Register Name: R329
Start Bit: 3
Stop Bit : 5
Length : 3
Description: Selects which signal to output IO pin
CLKin0
CLKin0_TYPE
CLKin0_EN
CLKin0_OUT_MUX
SYSREF MUX
CLKin1
CLKin1_TYPE
CLKin1_EN
CLKin1_OUT_MUX
CLKin1 (Ext. VCO)
CLKin1 (Feedback)
CLKin2/OSCout
CLKin2_TYPE
CLKin2_EN
Buffered OSCin
OSCout_MUX
OSCout clock format
Powerdown
Powerdown OSCout for CLKin2
PLL1 R Dividers
PLL1 Reference Input Select
CLKin_SEL_MODE
CLKin1 Manual
Selected Clock Input for PLL1
CLKIN_SEL_POL
CLKin_SEL0
Input w/ pull-dwn
Logic Low
CLKin_SEL1
PLL1_PD
R Delay
PLL1 Phase Detector and Charge Pump
Phase Detector Freq (MHz)
Charge Pump State
Phase Detector Polarity
Charge Pump Gain
CPout1
External Loop Filter
External VCXO
N Divider
N Delay
PLL1 NCLK MUX
OSCin
OSCin_PD
OSCin Source
External VCXO
PLL2_PD
Doubler
R Divider
PLL2 Phase Detector and Charge Pump
Internal Loop Filter
Internal VCOs
VCO/Clock Dist. Frequency
VCO_PD
VCO_LDO_PD
FB_MUX_EN
DCLKout6
FB_MUX
DCLKout8
SYSREF
(Feedback)
PLL2 NCLK MUX
PLL2_P
N Cal Divider (PLL2 0-Delay)
VCO_MUX
VCO0
VCO1
N Prescaler
To Clock Distribution
Wrote Register R353 (0x161) as 0x01 6101
Wrote Register R354 (0x162) as 0x01 6225
Wrote Register R364 (0x16C) as 0x01 6C00
Connection Mode: Device Not Connected
Protocol: SPI
Serial #: n/a
Texas Instruments


TICS Pro - LMK04828B
File
USB communications
Select Device
Options
Tools
Default configuration
Help
Write All Registers
Read All Registers
SYNC Dividers
Powerdown DDLY
Toggle SYNC_POL
Calc Current
LMK04828B
User Controls
Raw Registers
Set Modes
CLKin and PLLs
SYNC/SYSREF
Clock Outputs
Current Calculator
Other
Burst Mode
General
Context
Field Name: SDCLKout13_MUX
Register Name: R308
Start Bit: 5
Stop Bit : 5
Length : 1
Description: Select Device Clock for SYSREF output (0) or SYSREF clock source (1)
CLKout13
VCO0
VCO_MUX
VCO0
VCO1
CLKin1 (Ext. VCO)
2400
MHz
SYSREF DDLY
SYSREF_DDLY_PD
8
SYSREF Divider
SYNC _DISSYSREF
300
8
MHz
Buffered OSCin
OSCout_MUX
OSCin
Feedback Mux
Powerdown
OSCout
40
MHz
Clock Divider
Digital Delay
Analog Delay
Clock Output Select
SYSREF_GBL_PD
Clock Output
15
SYNC _DIS0
DDLY_PD
5
5
Half Step
HSg_PD
DDLYd0_EN
2 cycles
Half Step
ADLY_PD
500 ps
ADLYg_PD
ADLY_EN
700 ps
Divider+DCC+HS
Enable half step and duty cycle correction for analog delay path
Device Clock
IDL
ODL
CLKout0_1_PD
LVDS
DCLKout0_POL
SDCLKout1_POL
DCLKout0
160
MHz
Active
LVDS
SDCLKout1_PD
SDCLKout1
160
MHz
JESD Ref clock to FPGA
FPGA system clock
15
SYNC _DIS2
DDLY_PD
5
5
Half Step
HSg_PD
DDLYd2_EN
2 cycles
Half Step
ADLY_PD
500 ps
ADLYg_PD
ADLY_EN
700 ps
Divider only
Enable half step and duty cycle correction for analog delay path
SYSREF
IDL
ODL
CLKout2_3_PD
LVDS
DCLKout2_POL
SDCLKout3_POL
DCLKout2
160
MHz
Active
LVDS
SDCLKout3_PD
SDCLKout3
8
MHz
ADC clock
ADC SYSREF
15
SYNC _DIS4
DDLY_PD
5
5
Half Step
HSg_PD
DDLYd4_EN
2 cycles
ADLY_PD
500 ps
ADLYg_PD
ADLY_EN
700 ps
Divider only
Enable half step and duty cycle correction for analog delay path
SYSREF
IDL
ODL
CLKout4_5_PD
LVDS
DCLKout4_POL
SDCLKout5_POL
DCLKout4
160
MHz
Active
LVDS
SDCLKout5
8
MHz
Wrote Register R304 (0x130) as 0x01 300F
Wrote Register R310 (0x136) as 0x01 36F1
Wrote Register R311 (0x137) as 0x01 3706
Connection Mode: Device Not Connected
Protocol: SPI
Serial #: n/a
Texas Instruments


TICS Pro - LMK04828B
File
USB communications
Select Device
Options
Tools
Default configuration
Help
Write All Registers
Read All Registers
SYNC Dividers
Powerdown DDLY
Toggle SYNC_POL
Calc Current
LMK04828B
User Controls
Raw Registers
Set Modes
CLKin and PLLs
SYNC/SYSREF
Clock Outputs
Current Calculator
Other
Burst Mode
General
Context
Field Name: SDCLKout13_MUX
Register Name: R308
Start Bit: 5
Stop Bit : 5
Length : 1
Description: Select Device Clock for SYSREF output (0) or SYSREF clock source (1)
CLKout13
FPGA 160 MHz
FPGA SYSREF
DAC clock
FPGA clock to match DAC clock
PCIE clock to FPGA
PCIE clock to CPU
Wrote Register R304 (0x130) as 0x01 300F
Wrote Register R310 (0x136) as 0x01 36F1
Wrote Register R311 (0x137) as 0x01 3706
Connection Mode: Device Not Connected
Protocol: SPI
Serial #: n/a
Texas Instruments

PLLatinum Sim

File Options Data Export Resources Help

2370 to 2600 MHz

x 2

Fpd 80 MHz

Kpd 3.2 mA

2400 MHz Fvco

Fosc 40 MHz

Input Path
Input Multiplier 2

Feature Level
- Simple
- Intermediate
- Advanced

Loop Filter Components

C1	0 nF			
C2	27 nF	R2	0.82 kΩ	
C3	0.01 nF	R3	0.2 kΩ	
C4	0 nF	R4	0 kΩ	

Forced Component

VCO Characteristics

Kvco	18.3 MHz/V
VCOCap	0 pF

Max. Calculation Time 60 s

÷ 30

÷ 15 Fout 160 MHz

LVDS

Select Device | Filter Designer | Phase Noise | Bode Plot

Simulation Shown: Phase Noise

Filter Architecture
Filter Order: 4th Order
Filter Type: Passive

Filter Parameters
Calculate Loop Filter
Auto Parameter Strategy: Optimize Jitter

	Design Target		Min / Max		Actual
Loop Bandwidth	254.7527 kHz	Auto	0.0	100	254.7229 kHz
Phase Margin	73.8 deg	Auto	1	89	87.4486 deg
Gamma	10.192	Auto	0.0	50	0.5782
T3/T1 Ratio	4.461 %	Auto			0 %
T4/T3 Ratio	0 %	Auto			0 %

Min. High Order Cap 0 pF Actual 10 pF

Capacitor Value Step 10% Resistor Value Step 10%

Design Warnings
VCOCap/MinHighCap Restrict BW

Restrict Components

C1		nF			
C2		nF	R2		kΩ
C3	0.01	nF	R3	0.2	kΩ
C4	0.01	nF	R4	0.2	kΩ

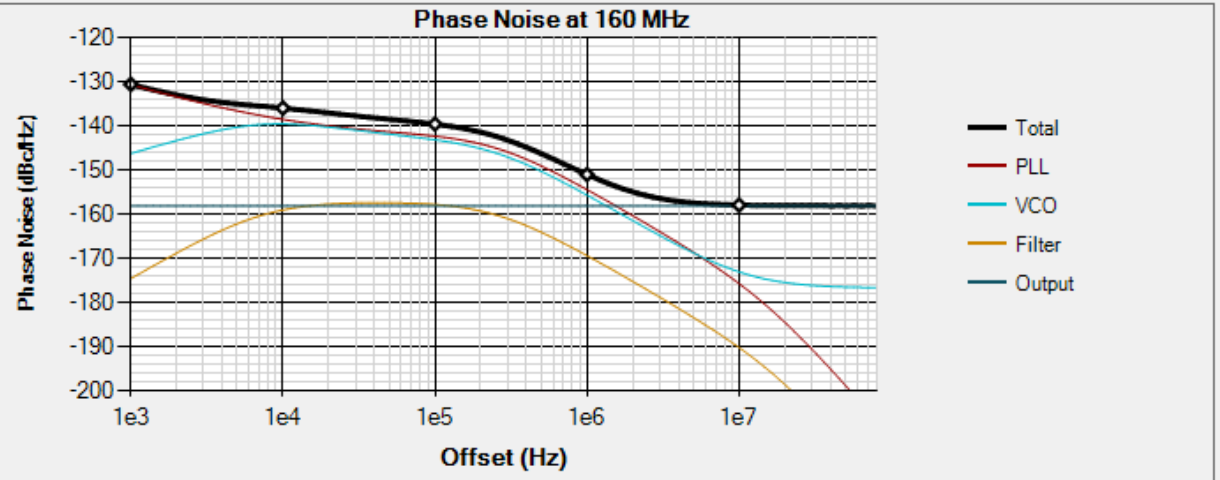
Smart force selected values

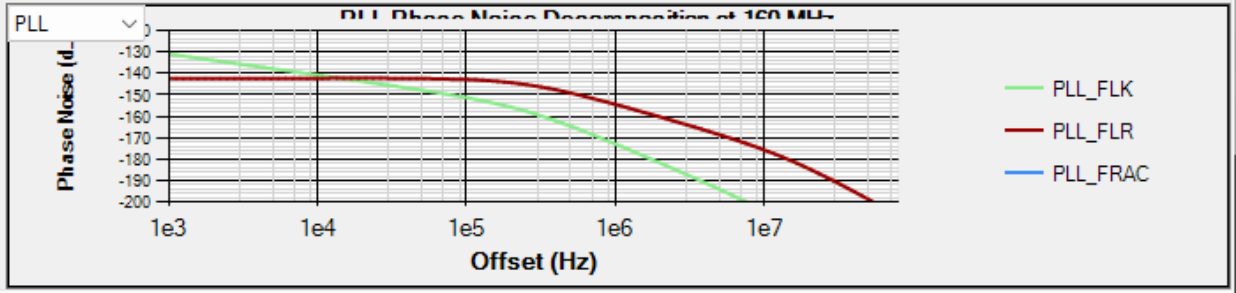
Filter Optimizer
Setup Conditions other Tabs
Optimize: Jitter (fs) 130

Parameter	Achieved	Limit
Jitter (fs)	130	50
Disabled		
Disabled		
Disabled		
Disabled		

Filter Parameters Time

Restrict Components Time





Device Selected = LMK04828B Loop Bandwidth = 254.7229 kHz Phase Margin = 87.4 deg

Texas Instruments

PLLatinum Sim

File Options Data Export Resources Help

2370 to 2600 MHz

x 2

Fpd 80 MHz

Kpd 3.2 mA

2400 MHz Fvco

Fosc 40 MHz

Input Path
Input Multiplier 2

Feature Level
- Simple
- Intermediate
- Advanced

Loop Filter Components

C1	0 nF		
C2	27 nF	R2	0.82 kΩ
C3	0.01 nF	R3	0.2 kΩ
C4	0 nF	R4	0 kΩ

Forced Component

VCO Characteristics
Kvco 18.3 MHz/V
VCOCap 0 pF

Max. Calculation Time 60 s

÷ 30

÷ 15 Fout 160 MHz

LVDS

Select Device | Filter Designer | Phase Noise | Bode Plot

Graph Settings
Points 101 Autoscale Axes

	min	max	
X Axis	0.001	80	MHz
Y Axis	-200	-120	dBc/Hz

Load Comparison Trace

Total Phase Noise at Offsets

	Offset (kHz)	Noise
MKR1	0.1	-120.9
MKR2	1	-130.5
MKR3	10	-135.9
MKR4	100	-139.5
MKR5	1000	-151
MKR6	10000	-157.9

Crossover Metrics

InBand to VCO	224.7 kHz
PLL 1/f to Floor	14.2 kHz
VCO 1/f^3 to 1/f^2	29.4 kHz
VCO 1/f^2 to Floor	11.3 MHz

Integrated Noise

Lower Limit	1	kHz
Upper Limit	20	MHz
RMS Jitter	130	fs

Other Noise Metrics

RMS Phase Error	0.007 deg
EVM	.012 %
Integrated Noise	1.707e-8
SNR	-77.7 dBc/Hz
Avg Noise Floor	-153.7 dBc/Hz

Other Noise Sources
- Include Spurs
- Enable Loop Filter Noise
- Enable Distribution Path Noise

Output/Distribution Path Metrics

1/f (Total)	-1000	dBc/Hz
Floor (DistPath)	-158.1	dBc/Hz
Floor (Div/Mult)	-1000	dBc/Hz

OSC, PLL, and VCO Noise

Input Source (OSC) Noise
- Disable
- Use Metrics
- Load Data

VCO Noise
- Disable
- Use Metrics
- Load Data

Noise Metrics (dBc/Hz)

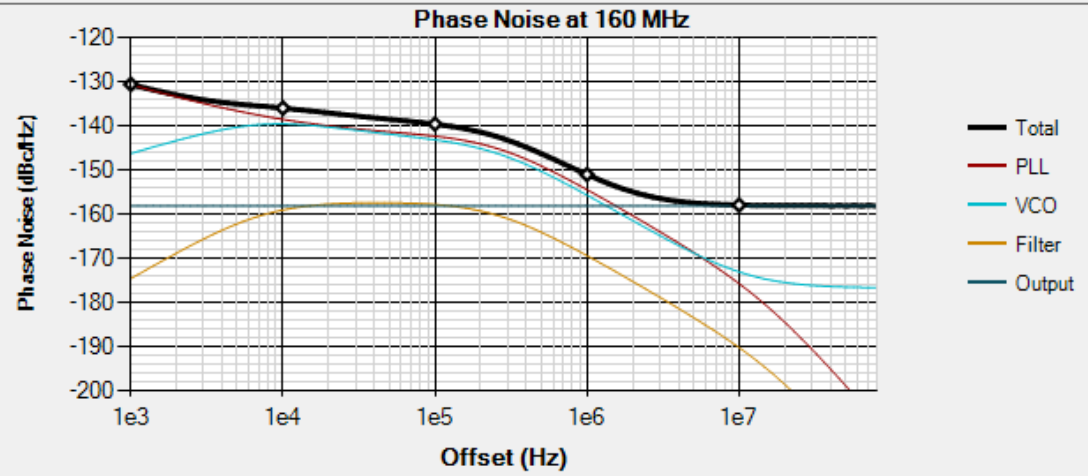
1/f^3	-155.08
1/f^2	-139.76
Floor	-160.81

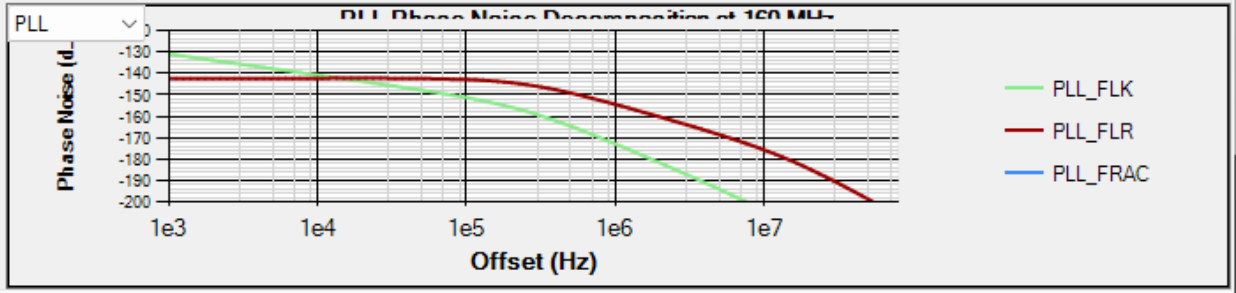
PLL Noise
- Disable
- Use Metrics
- Load Data

Noise Metrics (dBc/Hz)

Figure of Merit	-227.5
Normalized 1/f	-125
Fractional	-1000

Manual Override



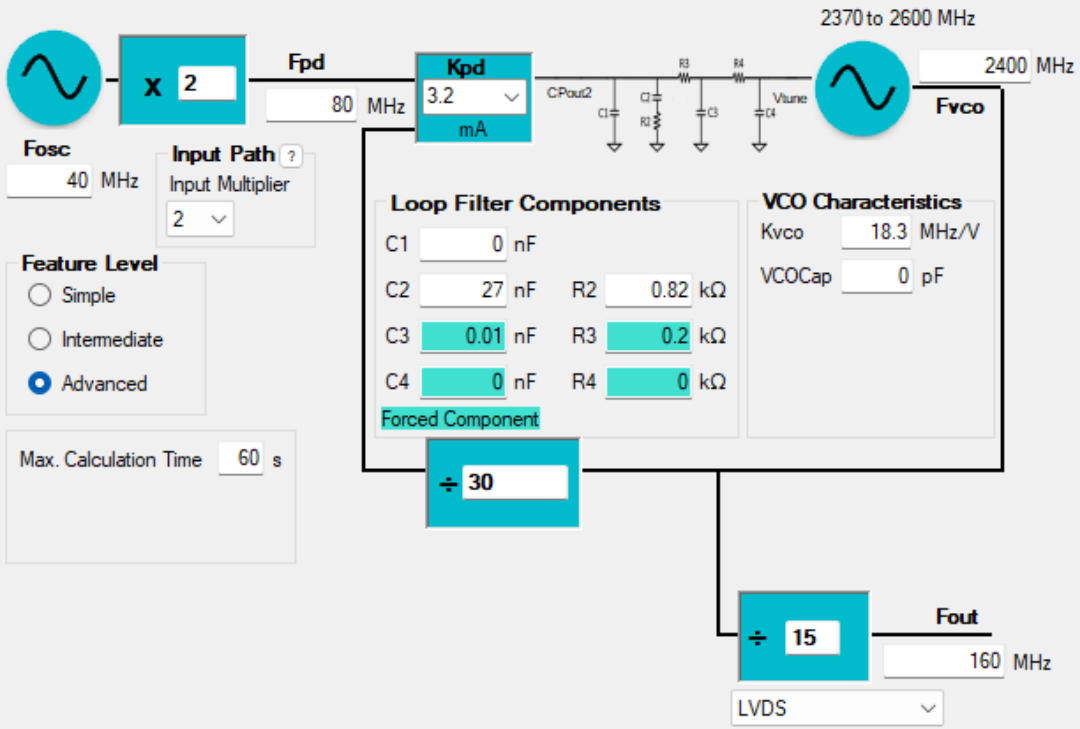


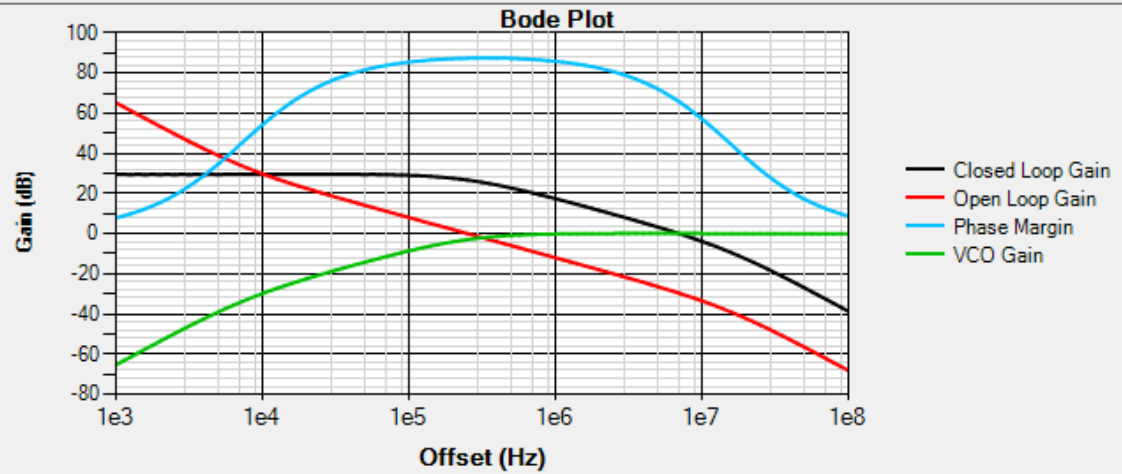
Device Selected = LMK04828B Loop Bandwidth = 254.7229 kHz Phase Margin = 87.4 deg

Texas Instruments

PLLatinum Sim

File Options Data Export Resources Help





Select Device | Filter Designer | Phase Noise | Bode Plot

Graph Settings

		min	max	
Points	101	X Axis	0.001	100 MHz
Autoscale Axes		Y Axis	-100	100 dB/degrees

Loop Filter Characteristics

Loop Bandwidth	254.72292	kHz
Phase Margin	87.4486	deg
Gamma	.5782	
T3/T1 Ratio		%
T4/T3 Ratio		%
Gain Margin	1000	dB
Damping Factor	0.5112613	dB
Natural Frequency	249.11223	kHz

Bode Plot Markers

Offset (kHz)	VCO Gain (dB)	Open Loop (dB)	Closed Loop (dB)
1	-65.3	65.3	29.5
10	-29.8	29.9	29.7
100	-8.5	8.1	29.2
1000	-0.1	-11.9	17.5
10000	0.1	-33.4	-3.7

Closed Loop Poles

	Real	Imaginary	Frequency	
p0	-5.722e-4	0e0	2.7814e-1	s/kHz
p1	-4.9038e7	1.1204e11	1.4205e-15	s/kHz
p2	-4.9038e7	-1.1204e11	1.4205e-15	s/kHz
p3	0	0	n/a	s/kHz

Poles and Time Constants

	Design Target	Actual			Design Target	Actual	
T2	2.4231e-5	2.214e-5	s	T2	6.5682e0	7.1886e0	kHz
T1	2.0623e-2	1.0196e-8	s	T1	7.7174e-3	1.5609e4	kHz
T3	9.1999e-4	0	s	T3	1.73e-1	n/a	kHz
T4	0	0	s	T4	n/a	n/a	kHz

Device Selected = LMK04828B Loop Bandwidth = 254.7229 kHz Phase Margin = 87.4 deg

Texas Instruments