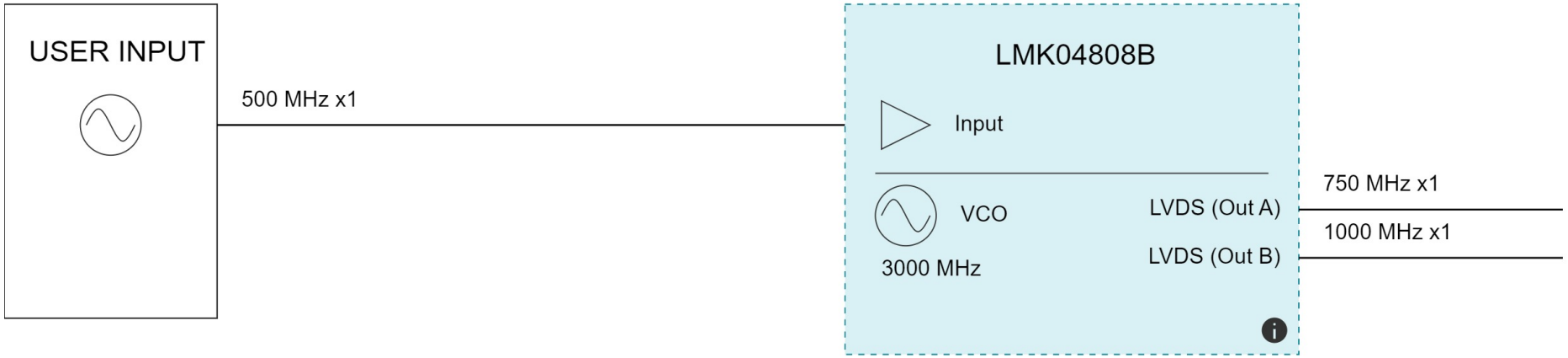
Clock tree architect design report

1. Selected solution details:

1.a. Block diagram:



https://webench.ti.com/clock-tree-architect

1.b. Solution details:

Devices	Area (mm²)	BOM price estimate ($)	Jitter (fs rms)	Power (mW)
LMK04808B	81.00	7.660	100 Out A: 100 Out B: 100	589

1.c. Device details:

Devices	Area (mm²)	BOM price estimate ($)	Current (mA)	Power (mW)
LMK04808B	81.00	7.660	179	589

1.d. Output details:

Devices	Output	Frequency	Format	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Deterministic phase
LMK04808B	Out A	750 MHz	LVDS	1	100	-157	Yes [1]
	Out B	1000 MHz	LVDS	1	100	-157	Yes [1]

[1] Requires some settings at device level. Kindly, refer the datasheet.

2. Other solutions:

Devices	Area (mm²)	BOM price estimate ($)	Jitter (fs rms)	Power (mW)
LMK04821	81.00	9.860	88	535
LMK04208	81.00	5.710	100	589
LMK04832	81.00	14.960	50	713
CDCE62002 and LMX2571	61.00	7.700	321	947
LMK04805B and LMX2571	117.00	12.500	321	750
LMK05028 and LMX2571	117.00	19.800	321	389
LMK04610 and LMX2571	100.00	20.280	321	663
CDCE72010 and	297.00	33.500	321	964

Devices	Area (mm²)	BOM price estimate ($)	Jitter (fs rms)	Power (mW)
LMX2571				
LMX1204	36.00	200.000	254	1630
LMK04828B	81.00	9.860	88	535

3. Required system specifications and parameters:

3.a. Required output details:

Name	Format	Frequency	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Additional specs
Out A	Any	750 MHz	1	1000	-50	-
Out B	Any	1000 MHz	1	1000	-50	-

3.b. Input details:

One or more of the below inputs or TI oscillators may be used.

Name	Frequency	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Additional specs
Input A	500 MHz	1	10	-	-

3.c. System configuration options:

Application: Test & measurement
Jitter integration bandwidth: 12 kHz to 20 MHz
Max. number of stages: 5
System features required:
Radiation hardened: Exclude
Solution scoring:
Jitter: Very important, Power: Important, Price: Less important, Area: Less important

3.d. External VCO and VCXO computation parameters:

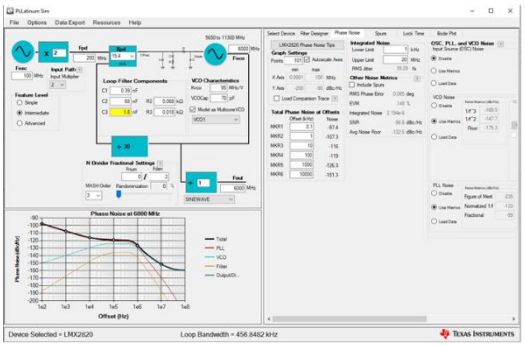
VCO attribute	Value	VCXO attribute	Value
Price ($)	30	Price ($)	20
Area (mm²)	140	Area (mm²)	180
Current (mA)	15	Current (mA)	15
Noise floor (dBc/Hz)	-156	Noise floor (dBc/Hz)	-168
Jitter (fs rms)	50	Jitter (fs rms)	50
Min frequency (MHz)	1	Frequency (MHz)	500
Max frequency (MHz)	10000	Auto pick VCXO frequency	true

Featured clocks & timing tools

Clock tree architect design tool helps you select the right clocks & timing products to design a clock tree based on user entered output, input and system specifications. Along with the clock tree structure – it provides an approximate metric for power, area, jitter and other system parameters. Users are recommended to use the below tools to help with more accurate in-depth simulations, device programming, loop filter design and configuration.

PLLatinum Simulator Tool (PLLATINUMSIM-SW)

The PLLATINUMSIM-SW simulator tool lets you create detailed designs and simulations of our PLLATINUM™ integrated circuits which include the LMX series of PLLs and synthesizers. Users can design active and passive filters, do detailed simulations of phase noise, purs, lock time and bode plots.



TICS Pro Software (TICSPRO-SW)

The TICS Pro software is used to program the evaluation modules (EVMs) for device numbers with these prefixes: CDC, LMK and LMX. These devices include PLLs and voltage-controlled oscillators (PLL+VCO), synthesizers and clocking devices. Users can program EVMs through USB2ANY interface adaptor or onboard USB interface and export the programming configurations for use in end application. Even without an EVM, TICS Pro is very useful tool in determining and validating register configurations and how to set up the device.

Clocks & timing product portfolio and additional resources

Visit Clocks & timing home page to explore the full product portfolio and additional resources to help you with your designs. Also, checkout TI Precision Labs - Clocks and timing videos to learn more about clocks and timing basics, phase lock loop fundamentals, noise, network synchronizers and design tips.

Technical support

TI E2E™ support forums

Receive fast and reliable technical support from our engineers throughout every step of your design.

Get answers now

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