6.6 Clock driver Characteristics

Table 83 — Clock driver Characteristics at application frequency (frequency band 1)

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400/2666/3200		Unit
			Min	Max	Min	Max	
$t_{jit(cc+)}$	Cycle-to-cycle period jitter		0	0.025 x t_{CK}	0	0.025 x t_{CK}	ps
$t_{jit(cc-)}$			0	0.025 x t_{CK}	0	0.025 x t_{CK}	ps
t_{STAB}	Stabilization time	CK_t/CK_c stable	-	5	-	5	ms
t_{CKsk}	Fractional Clock Output Skew[1]			10		10	ps
t_{jit}(per)	Yn Clock Period jitter		- 0.025 x t_{CK}	0.025 x t_{CK}	- 0.025 x t_{CK}	0.025 x t_{CK}	ps
t_{jit}(hper)	Half period jitter		- 0.032 x t_{CK}	0.032 x t_{CK}	- 0.032 x t_{CK}	0.032 x t_{CK}	ps
$t_{PW,H/L}$[2]	Yn_t/Yn_c Pulse Width duration						ns
t_{QSK1}[3]	Qn Output to clock tolerance		- 0.125 x t_{CK}	0.125 x t_{CK}	- 0.125 x t_{CK}	0.125 x t_{CK}	ps
t_{staoff}[4]	Clock delay through the register between the input clock and output clock [5]		$t_{PDM(min)}$ + 1/2 * tCK	$t_{PDM(max)}$ + 1/2 * tCK	$t_{PDM(min)}$ + 1/2 * tCK	$t_{PDM(max)}$ + 1/2 * tCK	ns
t_{dynoff}[6]	Maximum re-driven dynamic clock offset[7]		-	50	-	45	ps