Texas Instruments Incorporated
Military Products Department
Military High Reliability Integrated Circuits
Processing Conformance Report

Device Type: **5962-1620701VXC**
SMD: **5962-1620701VXC**
Processing Type: **CLASS V**

PCR Lot Number: **4000308MTT**
Device Description: **QMLV CDCLVP111 DEVCIE SETUP**

Assembly Location: **MMT** Assembly Date Code Year: **2023** Week: **29** Lot Window: **A**
Wafer Lot #: **6026947** Wafer Lot Date Code Year: **2016** Qtr: **2Q** Die Rev: **A** W/F Code: **R**
Wafer #: **01**

Integrated Circuits referenced above have received the following processing per recorded lot history.

SCREEN	METHOD	(MIL-STD-883)	
✓ INTERNAL VISUAL PRECAP	2010	CONDITION A (100X)	
✓ INTERNAL VISUAL PRECAP	2010	CONDITION A (40X)	
✓ INTERNAL VISUAL PRECAP	2010	CONDITION A (L/A)	
Wafer Number(s) used in Production:	**01**		
✓ TEMPERATURE CYCLING	1010	CONDITION C	
✓ CENTRIFUGE	2001	CONDITION E,Y1 PLANE	
✓ PIND TEST	2020	CONDITION A	
✓ RADIOGRAPHY	2012	☐ MONITOR OR ✓ 100%	
✓ INTERIM ELECTRICAL TEST		25c DC / FUNCTIONAL	
✓ BURN IN	1015	TEMP (°C): **125c**	TIME (Hrs): **240**
		PDA 1: **0.00%**	PDA 2: **N/A**
FINAL ELECTRICAL TEST TEMP	✓ 25c ✓ 125c ✓ -55c ☐ **N/A**		☐ **N/A**
TEST PROGRAM #(s)	**I30521/04**	**I30521/04**	**I30521/04**
✓ HERMETICITY	1014		
FINE LEAK		CONDITION A OR B	
GROSS LEAK		CONDITION C	
✓ EXTERNAL VISUAL	2009	(100%)	
✓ EXTERNAL VISUAL	2009	(L/A)	

QUALITY CONFORMANCE ATTRIBUTE DATA GROUP "A " SUMMARY

SUBGROUP	TEST & TEMP	SAMPLE SIZE
✓ A-1/4/7	DC ELECTRICAL - AMBIENT	116 OR 100%
✓ A-2/5/8	DC ELECTRICAL - MAXIMUM	116 OR 100%
✓ A-3/6/8	DC ELECTRICAL - MINIMUM	116 OR 100%
✓ A-9	AC ELECTRICAL - AMBIENT	116 OR 100%
✓ A-10	AC ELECTRICAL - MAXIMUM	116 OR 100%
✓ A-11	AC ELECTRICAL - MINIMUM	116 OR 100%

Device Lead-Finish complies with MIL-PRF-38535 A.3.5.6.3 Microcircuit finishes: "Finishes of all external leads or terminals and all external package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3 as applicable. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. The tin content of solder shall not exceed 97 percent. Tin shall be alloyed with a minimum of 3 percent lead by weight.

SOLDER PROCESSING DATE (IF APPLICABLE): **N/A**
NOTE: The following documents MUST be pulled and sent with each lot.
(A copy to be placed in each box)
1) PROCESS CONFORMANCE REPORT
2) GENERIC GROUP B QCI SUMMARY REPORT
3) GENERIC GROUP D QCI SUMMARY REPORT
4) WAFER LOT ACCEPTANCE REPORT FOR THE WAFER LOT USED IN THIS ASSEMBLY LOT.

Prepared By: **Tharun Natarajan** Date: **02/09/2026**

QCI Group B - Lot #: **4000308**	Date Code: **2329A**	Pkg Type: **36HFG**	Lead Finish: **A**
QCI Group C - Lot #: **6118898**	Date Code: **1627A**	MCG: **140**	Wafer Lot Date Code: **6B**
QCI Group D - Lot #: **3002472**	Date Code: **2311A**	Pkg Type: **20HKH**	Lead Finish: **C**
QCI Group D6 - Lot #: **3011447**	Date Code: **2326A**	Pkg Type: **36HFG**	Lead Finish: **A**
QCI Group E - Lot #:	Wafer Lot #:	Parent Wafer Lot #:	
QCI Group P - Lot #:	Date Code:	Pkg Type:	Lead Finish:
Wafer Lot Accept - Lot #: **6118898**	Wafer Lot #: **6026947**		

Group B Summary Report

Lot Number: 4000308
Device Name: 5962-1620701VXC
Date Code: 2023-29-A
Assembly Site: MMT
Test Start: 02/13/2024
Test Complete: 02/13/2024
Lead Finish: A
Pin: 36
Package: HFG
Package Family: GROUP 9J

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
B1	Resistance To Solvents	TM2015	3	0	1
B2	Bond Strength	TM2011	22	0	2
B2	Die Attach Strength	TM2019 OR TM2027	3	0	
B3	Solderability	TM2003	22	0	3
B4	Ball Shear Test For Bga	JESD22-B117	45	NA	4
B4	Solder Column Pull Test Cga Pa	TM2038	45	NA	5

Notes: 1. Resistance to solvents testing required only on devices using inks or paints as a marking medium.
2. 22 wires / 4 units minimum.
3. 22 leads / 3 packages minimum. Not required for solder columns. Solder temperature +245C +/- 5C.
4. 45 balls from 2 devices minimum. Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot. For devices with solder terminations, Physical dimension test shall be performed with balls/columns.
5. 45 columns from 2 devices minimum.

Comments:

Prepared By: Nattapapat Laokham
Prepared By Email: x1112274@ti.com
Prepare Date: 02/12/2024

Group C Summary Report

Lot Number:	6118898	Device Name:	CDCLVP111-SP	Assembly Site:	MMT
Lot Date Code:	2016-27-A	Wafer Lot Date Code:	2016-2Q-A-R	Wafer Lot Number:	6026947
Parent Die:	RCDCLVP111A0VE	Die Attach:	QMI	Window:	2Q 2016 to 1Q 2017
Pin:	36	Package:	HFG	MCG:	140
Test Start:	08/08/2016	Test Complete:	09/21/2016		

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
C1	Steady-state life test	1005		0	1
C1	Endpoint Electrical Test		45	0	2

Notes: 1. 1,000 hours/125C or equivalent. (If greater than 1,000 hours/125C enter actual conditions into comments below)
2. Endpoint electrical testing in accordance with device test specification.

Comments:
50/0 TESTED

Prepared By:	Jie Xia	Prepared By Email:	jxia@ti.com	Prepare Date:	11/07/2016

Group D Summary Report

Lot Number: 3002472
Date Code: 2023-11-A
Test Start: 05/23/2024
Pin: 20
Window: 11 2023 to 46 2023

Device Name: 5962R2021001VSC
Assembly Site: MMT
Test Complete: 06/14/2024
Package: HKH

Lead Finish: C
Package Family: GROUP 9J

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
D1	Physical Dimensions	TM2016	15	0	
D2	Ball Shear Test For Bga	JESD22-B117	45	0	1
D2	Solder Column Pull Test Cga	TM2038	45	0	2
D2	Lead Integrity	TM2004 AND TM2028	45	0	3
D2	Seal (Fine And Gross)	TM1014	3	0	4
D3	Class P (See Note)	SEE NOTE	30	0	5
D3	Class Y (See Note)	SEE NOTE	30	0	6
D3	Thermal Shock	TM1011	15	0	7
D3	Temperature Cycle	TM1010	15	0	8
D3	Moisture Resistance	TM1004	15	0	
D3	Visual Examination	TM1004 OR TM1010		0	
D3	Seal (Fine And Gross)	TM1014		0	
D3	End-Point Electrical Test			0	9
D4	Mechanical Shock	TM2002	15	0	10
D4	Vibration, Variable Freq	TM2007		0	11
D4	Constant Acceleration	TM2001		0	12
D4	Seal (Fine And Gross)	TM1014		0	13
D4	Visual Examination	TM2007		0	
D4	End-Point Electrical Test			0	
D5	Salt Atmosphere	TM1009	15	0	14
D5	Visual Inspection	TM1009		0	
D5	Seal (Fine And Gross)	TM1014		0	15
D6	Internal Water Vapor	TM1018	3 (5)	0 (1)	16
D7	Adhesion Of Lead Finish	TM2025	15	0	17
D8	Lid Torque	TM2024	5	0	18

Notes: 1. 45 balls from 2 devices minimum.
2. 45 columns from 2 devices minimum.
3. Condition B2, 3 devices, 45 leads total. For PGA and rigid leads use Condition B1 or Method 2028. For LCCC packages only, use condition D and SS of 15 based on the number of pads tested from 3 devices minimum. 45 Solder ball or columns from two(2) devices minimum for BGA/CGA. TM2004 does not apply for LGA/BGA/CGA packages. Per TM 2004, Paragraph 3.2, Procedure for pre-formed leads. When normally straight leads are supplied in a pre-formed condition (including the staggered lead dual-in- line configuration), the lead forming operation shall be considered an acceptable lead fatigue test in place of that specified, provided the lead forming has been done after lead plating and the forming is at least as severe in permanent lead deformation as the specified bending.
4. Seal (Fine and Gross) test applicable for packages with leads exiting through a glass seal only.
5. D3 Class P includes 30u Precondition per JESD22-A113, Acoustic Microscopy, split 15u for Temperature cycle -55/125C, 150cycles per JESD22-A104, split 15u for unbiased HAST 110C/85%RH, 264hr per JESD22-A118, Visual Mechanical per TM1004/1010 for all 30u, Electrical test per applicable device specification for all 30u.
6. D3 Class Y organic substrate includes 30u Precondition per JESD22-A113, split 15u for Temperature cycle -55/125C, 150cycles per JESD22-A104, split 15u for unbiased HAST 110C/85%RH, 264hr per JESD22-A118, Visual Mechanical per TM1004/1010 for all 30u, Electrical test per applicable device specification for all 30u.
7. Condition B, 15 cycles.
8. Condition C, 100 cycles.
9. Endpoint electrical testing in accordance with device test specification.
10. Condition B. Not Applicable for Class P.
11. Condition A.
12. Condition E (20KG) Y1 axis only.
13. Seal not applicable for class Y.
14. Condition A.
15. Seal not applicable for class Y or P.
16. 5000 PPM and 100C. Sample size is 3/0. Not applicable for class Y or P.
17. 15 leads, not performed for LCCC. Any deviations to test methods or conditions, such as centrifuge, will be specificed in the device travler.
18. Glass Frit Seal Only - N/A for MMT Assembly. Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

Comments:

Prepared By: Praveen B
Prepared By Email: p-b1@ti.com
Prepare Date: 06/18/2024

Group D6 Summary Report

Lot Number:	3011447	Device Name:	5962-1620701VXC		
Date Code:	2023-26-A	Assembly Site:	MMT		
Test Start:	12/15/2023	Test Complete:	01/12/2024	Lead Finish:	A
Pin:	36	Package:	HFG	Package Family:	GROUP 9J
Window:	26 2023 to 09 2024				

Comments:

Prepared By:	Watchara Thongnawakoon	Prepared By Email:	x0245876@ti.com	Prepare Date:	12/21/2023

WLA Summary Report

Lot Number: 6118898 Device Name: CDCLVP111-SP
Wafer Lot Date Code: 2016-2Q-A-R Wafer Lot Number: 6026947
Parent Die: RCDCLVP1110VE Lead Finish: C MCG: 140
Test Start: 09/21/2016 Test Complete: 09/21/2016

Sub-Group	Test	Method	Sample Size	Rejects / Data	Notes
WLA-1	Wafer Thickness	5007	2 wafers/lot	0	1
WLA-2	Metallization Thickness	5007	1 wafer/lot	0	2
WLA-3	Thermal Stablility	5007	1 wafer/lot	0	2,3
WLA-4	SEM Inspection Lot Acceptance	2018	2 wafers/lot	0	2
WLA-4	Lab Performing Analysis:			TI	
WLA-5	Glassivation Thickness	5007	1 wafer/lot	0	2
WLA-6	Gold Backing Thickness	5007	1 wafer/lot	0	2,4
WLA-7	Steady-state life test	1005		0	5
WLA-7	Endpoint Electrical Test	1005	45	0	6

Notes: 1. This test is not required when the finished wafer design thickness is greater than 10 mils before backgrind.
2. In-line monitor data for this wafer lot may be used.
3. Applicable to all linear, all MOS, all bipolar digital operating at 10V or more. (VFB/VT/C-V)
4. Gold backed wafers only.
5. 1,000 hours/125C or equivalent
6. Endpoint electrical testing in accordance with device test specification

Comments:

Prepared By: Vut Kangkamanee Prepared By Email: x0194988@ti.com Prepare Date: 12/23/2016