

# Using Clock Architect as of 2017-02-20 with dual loop devices

This document shows the process of simulating dual loop PLLs in Clock Architect and the design that's necessary to achieve best performance. In this document a design showing 119.6 fs rms can be **improved to 84.1 fs rms. Best performance is achieved when only LMK0482x is contributing to final phase noise/jitter.**

# Enter conditions, then open design.

**Basic** Advanced **Generate Solutions**

Part Filter

No filter ▼ Clear Filter 150 parts match this filter.

Clock Design Entry

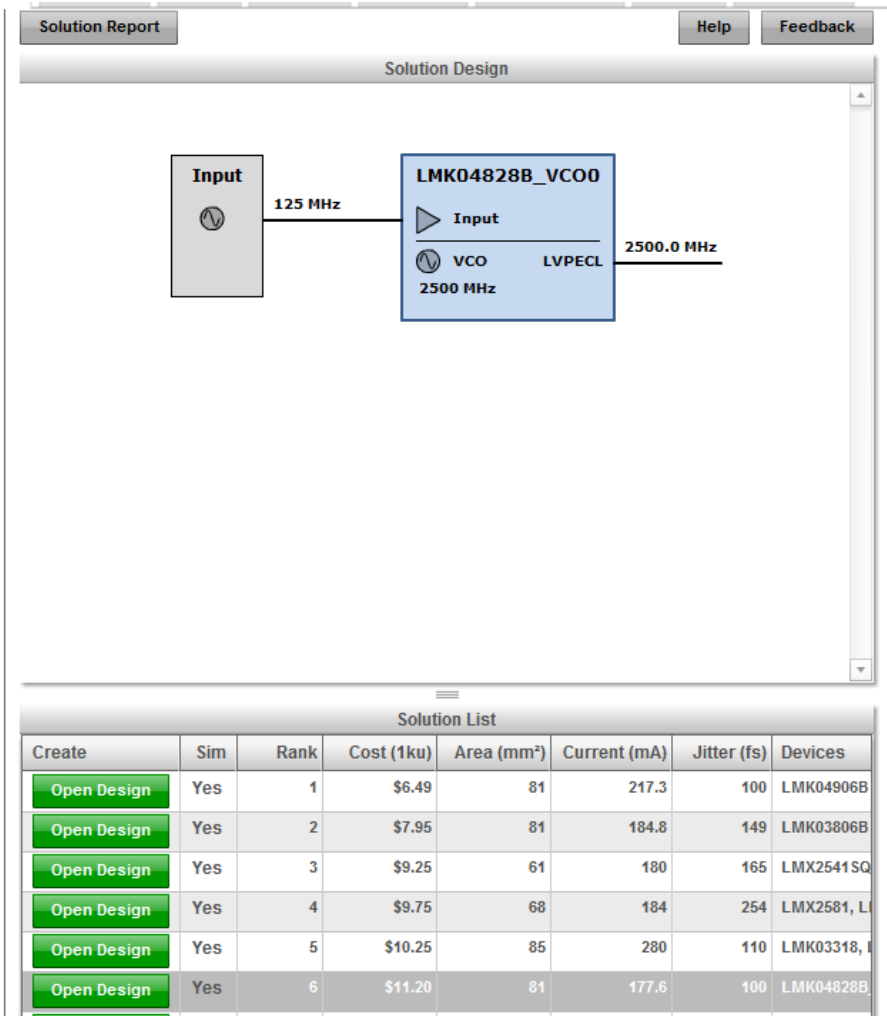
Fixed Output Frequencies Add

Name	Freq (MHz)	Format	Count	
fixed0	2500	LVPECL	1	Remove

☐ Automatically generate input frequencies for each solution.

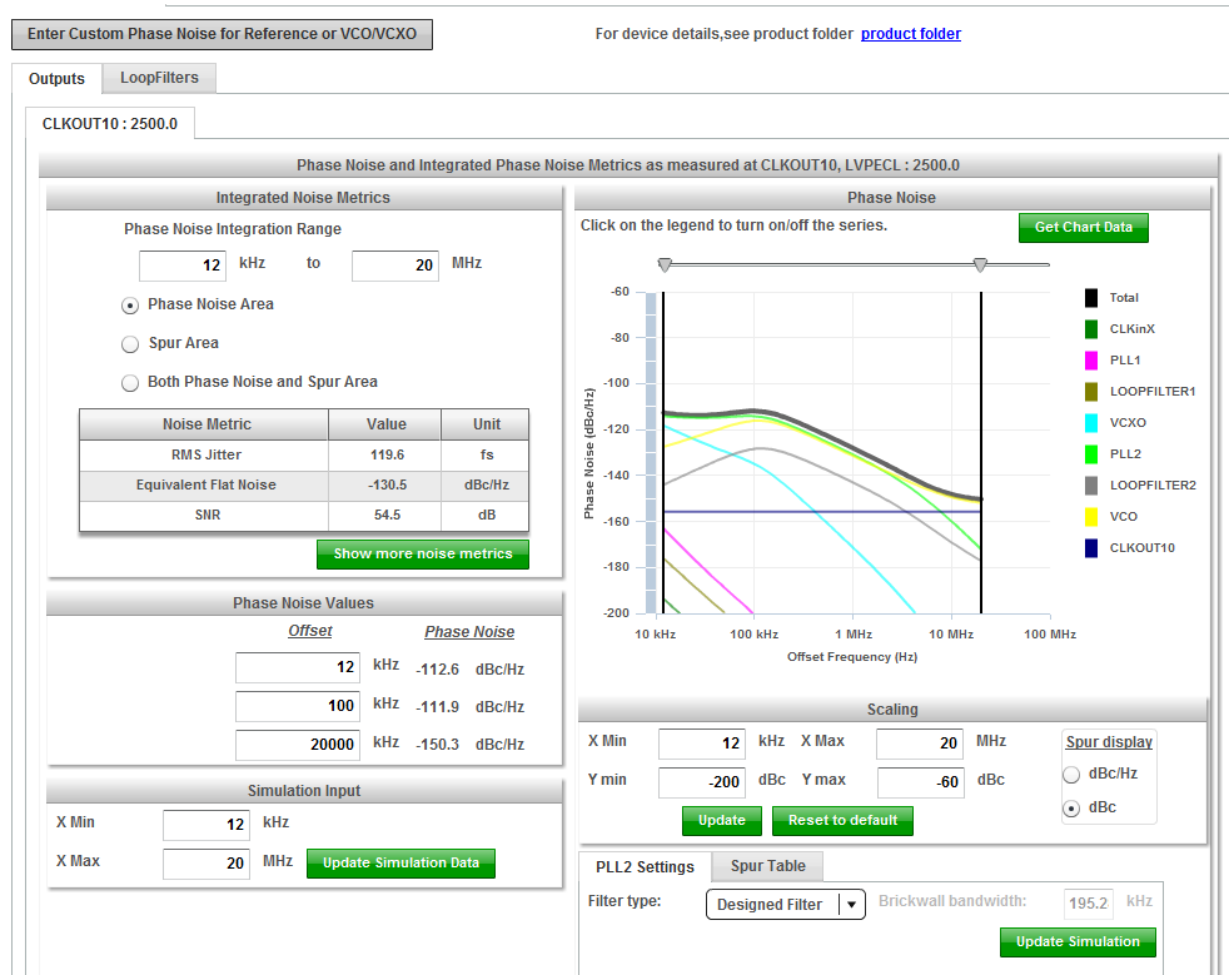
Input Frequencies Add

Name	Freq (MHz)	Count	
input0	125	1	Remove



# Initial sim results

- Need to set jitter integration range to needed range for application.
- Need to update VCXO information
  - Frequency
  - Phase Noise
  - Loop filter
- Need to update PLL2 loop filter based on updated VCXO.



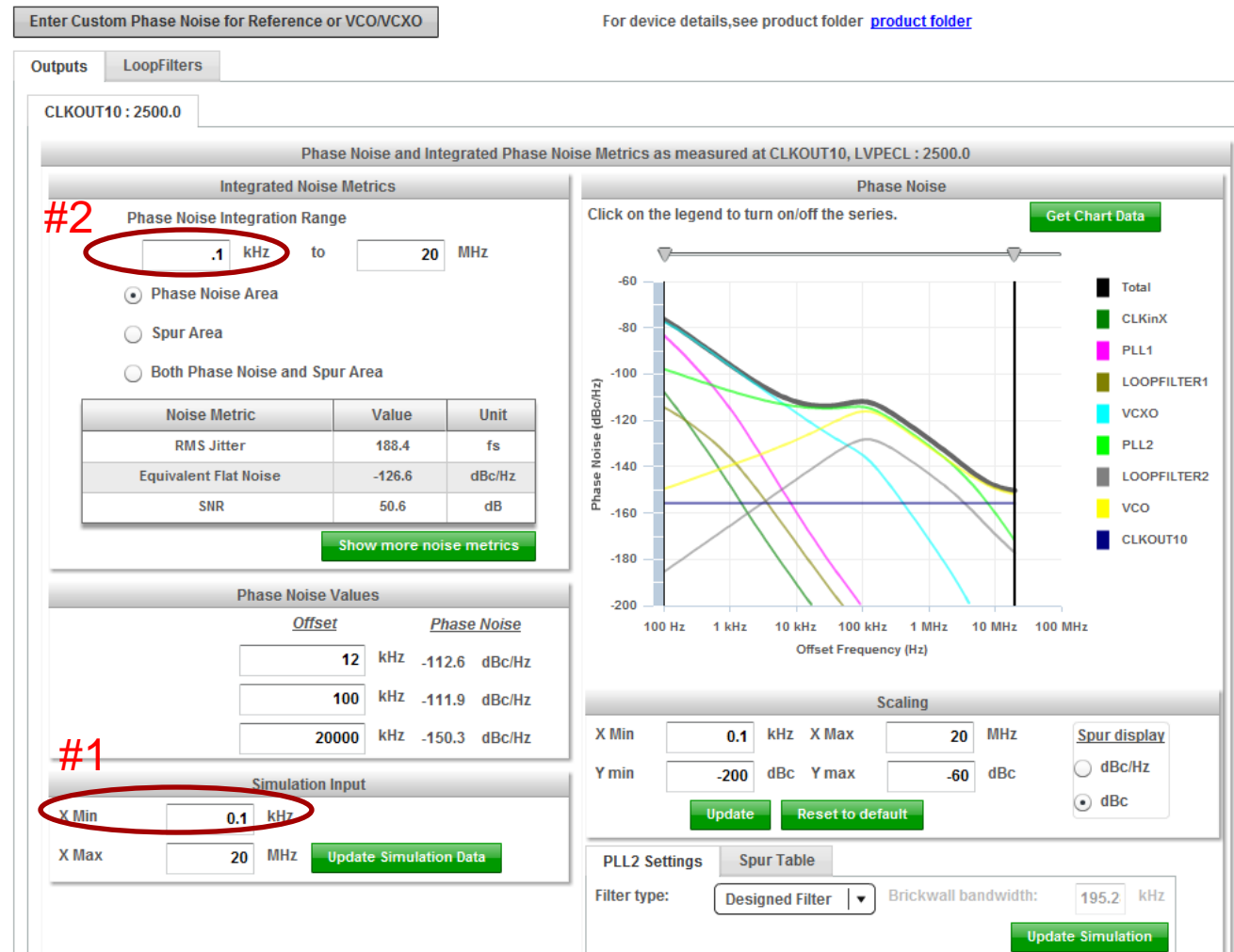
Note 12 kHz to 20 MHz integration = 119.6 fs rms

# Our requirements

- Using a VCXO of 125 MHz
  - VCXO with phase noise profile as below
    - 10 Hz    -76 dBc/Hz
    - 100 Hz   -109 dBc/Hz
    - 1 kHz    -137 dBc/Hz
    - 10 kHz   -152 dBc/Hz
    - 100 kHz   -160 dBc/Hz
    - 1 MHz    -164 dBc/Hz

# Updating range of data to analyze

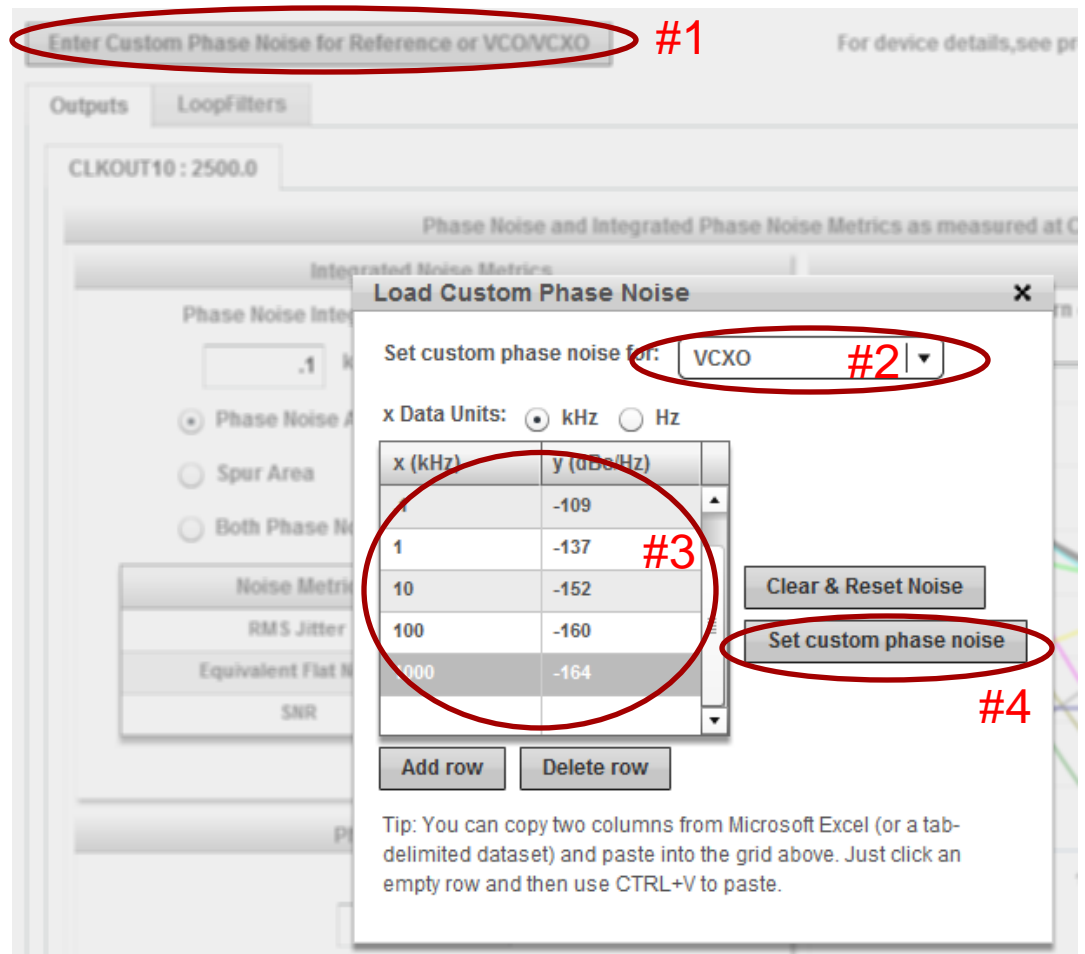
- #1) Changing simulation input to 0.1 kHz to increase amount of data to analyze
  - Setting 100 Hz
- #2) Update integration range to 100 Hz
- Note that VCXO noise dominates below 10 kHz and is impacting our jitter result.



Note 12 kHz to 20 MHz integration = 188.4 fs rms

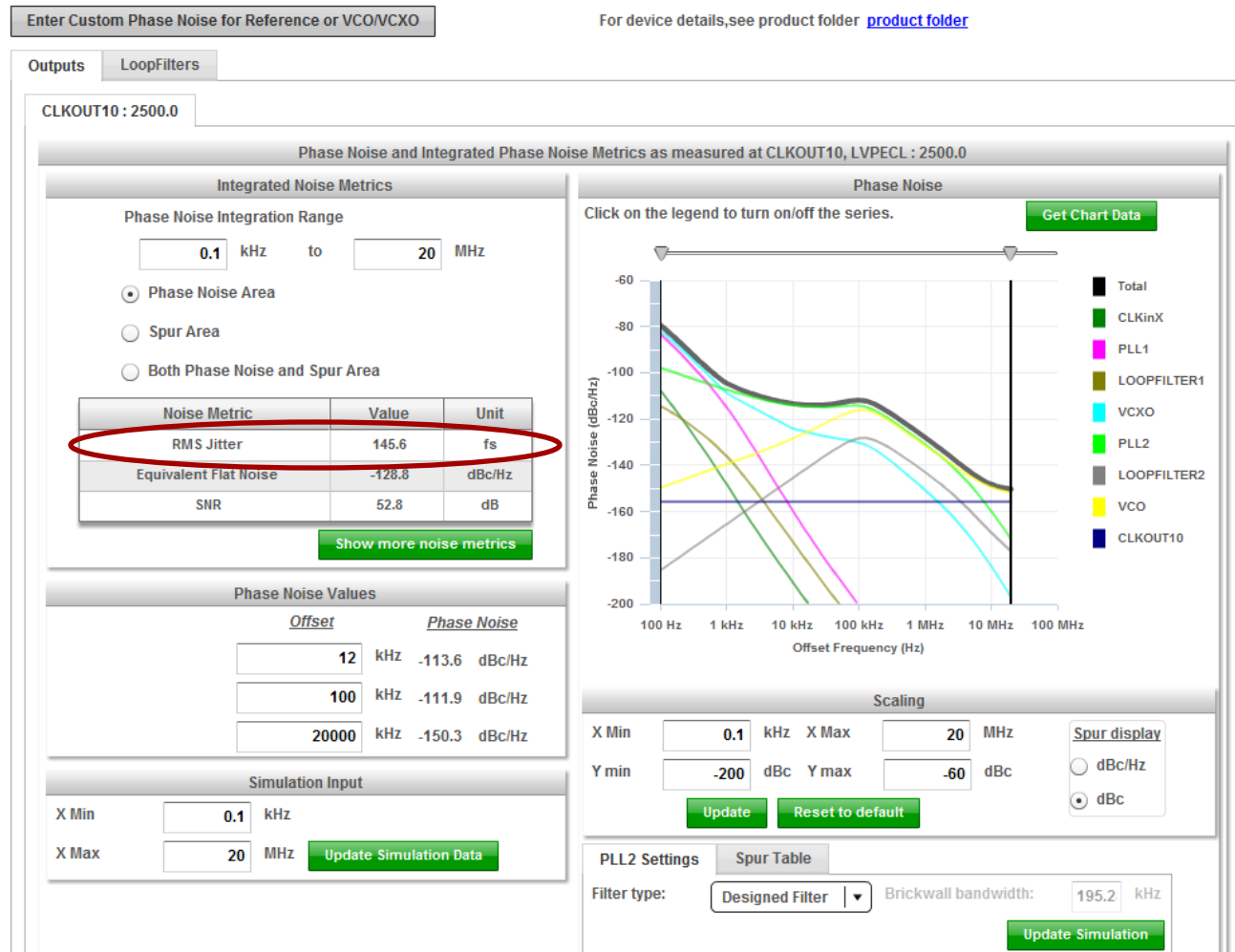
# Update VCXO performance

- #1) Click the “Enter Custom Phase Noise for Reference or VCO/VCXO”
- #2) Select “VCXO”
- #3) Enter tabulated data
  - Note that it is possible to past measured data into this window. Be sure the x Data units above are as required.
- #4) Set custom phase noise.
- Now you are returned to an updated simulation.



# Sim result with new phase noise

- Updated jitter result is 145.6 fs rms.
- It is noted that the VCXO noise profile is much lower below 10 kHz. However still most significant contributor at 100 Hz.
- However, must confirm VCXO frequency used by Clock Architect and PLL2 phase detector frequency.



# Default PLL1 Loop Filter

- Current state is 100 MHz VCXO. The VCXO we are considering is 125 MHz.
- For proper loop filter, VCO Gain must be entered for your specific VCXO, we will assume 2 kHz/V is correct.
- Note the phase detector is 25 MHz, this may be reduced to help reduce capacitor sizes by increasing PLL1 N.
- Charge Pump gain may also be be altered to impact loop performance. After making change, click 'Choose RC Components for me'

Enter Custom Phase Noise for Reference or VCO/VCXO

For device details, see product folder [product folder](#)

Outputs: **LoopFilters** #1

**LOOPFILTER1** LOOPFILTER1 - Locktime LOOPFILTER2 LOOPFILTER2 - Locktime

#2

Loop Filter Preferences and Device Settings

Filter type: Passive Filter Order: 2nd Order

Charge Pump Gain: 0.45 mA VCO Gain: 0.002 MHz/V

VCO Input Capacitance: 0 pF VCO Frequency: **100 MHz** #3

Phase Detector Frequency: 25 MHz

Charge Pump

C1 C2 R2

VCO

Loop Parameters

	Design Targets	Actual
Loop Bandwidth	0.075 kHz	0.08 kHz
Phase Margin	70 deg	70.4 deg
Gamma	0.24	0.27

Choose RC Components for me Help

Loop Filter Components

Capacitor Value Step: 10% C1: 68 nF Calculate C2: 3300 nF Calculate

Resistor Value Step: 10% R2: 2.2 kΩ Calculate

Update Actual Loop Parameters

Bode Plot

Click on the legend to turn on/off the series.

Degrees / dB

Offset Frequency (Hz)

Scaling

X Min: 0.1 kHz X Max: 10 MHz

Y min: -120 dBc Y max: 120 dBc

Update Reset to default



# Update PLL1 Loop Filter / VCXO Frequency

- #1) Updated VCO Frequency to 125 MHz.
- Changed Loop Bandwidth to
  - #2) Force Loop Bandwidth of 40 Hz (default 75 Hz)
    - Lower loop bandwidth provides more filtering of CLKin (PLL1 reference) and PLL1 noise.
  - #3) Force Phase Margin of 50° (default 70 °)
    - Lower phase margin causes the filter to peak more at loop bandwidth, but 'cut' better. Some peaking at loop bandwidth for loop filters with bandwidth less than lower integration typically doesn't negatively impact jitter. Keep phase margin > 45 degrees.
- #4) Update the Loop Filter

Enter Custom Phase Noise for Reference or VCO/VCXO For device details, see product folder

Outputs **LoopFilters**

LOOPFILTER1 **LOOPFILTER1 - Locktime** LOOPFILTER2 LOOPFILTER2 - Locktime

**Loop Filter Preferences and Device Settings**

Filter type: **Passive** Basic **Advanced**

Filter Order: **2nd Order**

Charge Pump Gain: **0.45** mA

VCO Gain: **0.002** MHz/V

VCO Input Capacitance: **0** pF

**#1** VCO Frequency: **125** MHz

Phase Detector Frequency: **25** MHz

Charge Pump

C1

C2

R2

VCO

**Loop Parameters**

	Design Targets	Actual
<b>#2</b>	Loop Bandwidth: <b>0.04</b> kHz <input type="checkbox"/> Auto	0.043 kHz
<b>#3</b>	Phase Margin: <b>50</b> deg <input type="checkbox"/> Auto	52.6 deg
	Gamma: <b>0.24</b> <input checked="" type="checkbox"/> Auto	0.34

**#4** **Choose RC Components for me** **Help**

**Loop Filter Components**

Capacitor Value Step: **10%**

C1: **470** nF ☒ Calculate

C2: **4700** nF ☒ Calculate

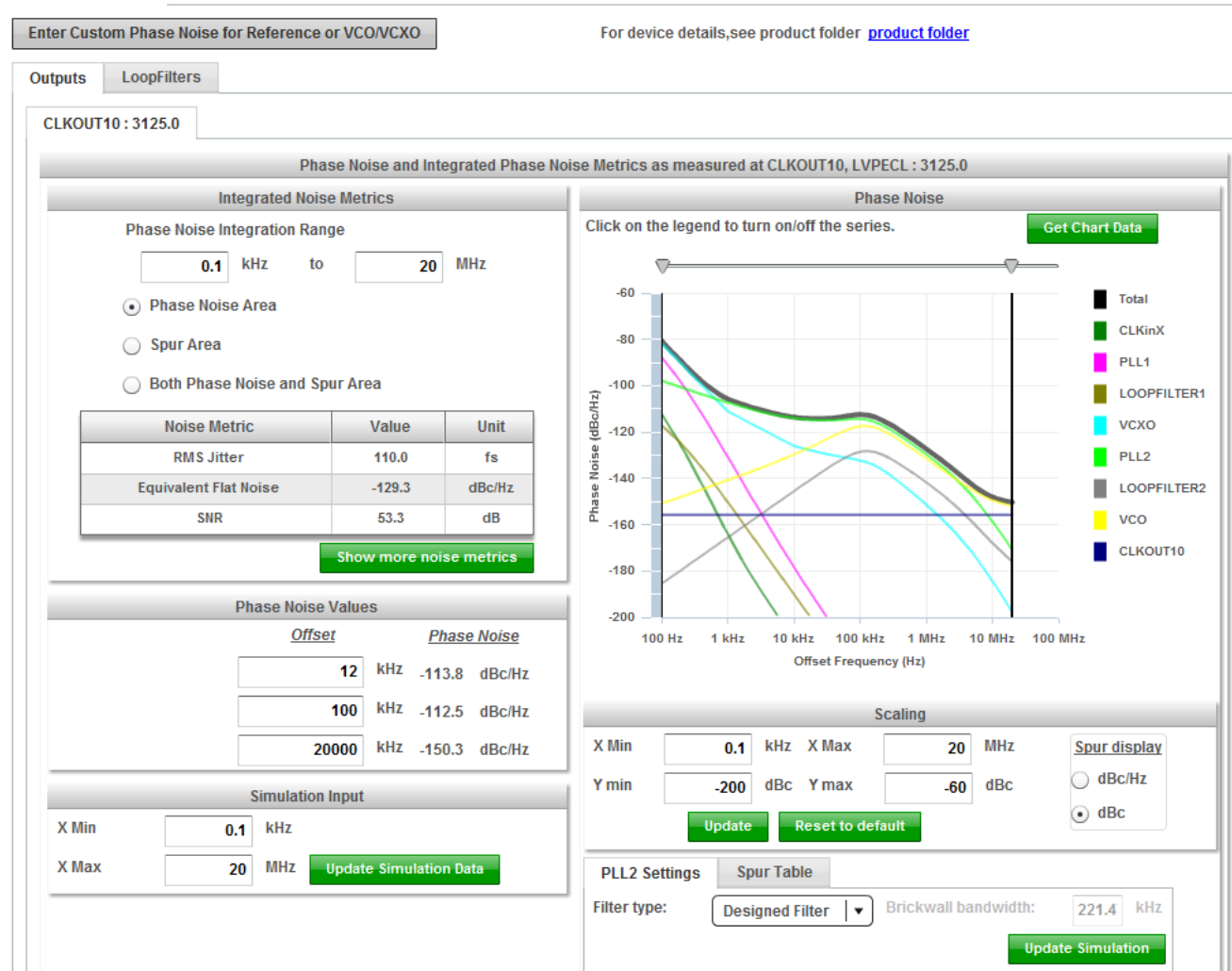
Resistor Value Step: **10%**

R2: **1.5** kΩ ☒ Calculate

**Update Actual Loop Parameters**

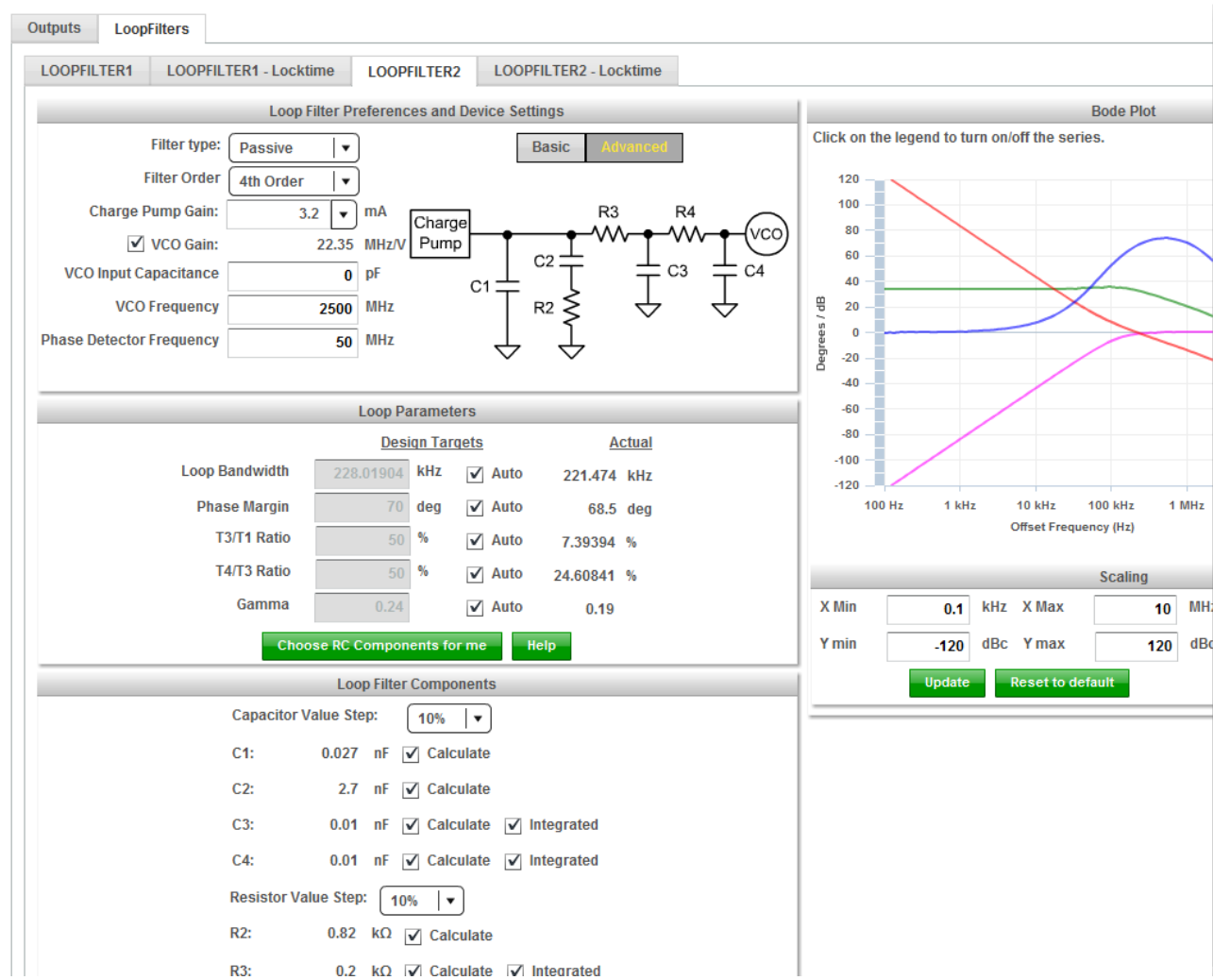
# Results of updating PLL1 Loop Filter

- Note that because we narrowed the loop bandwidth of PLL1, the gap between PLL1 noise and VCXO noise at 100 Hz is larger, this is because the VCXO is filtering the PLL + Reference noise more at 100 Hz.
  - This shows a VCO (VCXO) dominant type loop filter for PLL1.
- Because we changed our VCXO frequency, the clock output frequency has also increased to 3125 MHz, we must update PLL2 loop filter.



# Default PLL2 Loop Filter for this design

- Note from initial simulation, the phase detector was set to 50 MHz, this is sub-optimal and was reducing our jitter performance, the maximum possible phase detector frequency should normally be used for PLL2 when presented with a clean reference.
  - LMK0482x can accept up to 155 MHz PDF.



# Updating PLL2 Loop Filter

- #1) Select Loop Filters tab
- #2) Select LOOPFILTER2
- #3) Select Advanced Mode
- #4) Update the phase detector frequency to be the same as VCXO frequency for PLL R = 1.
  - Note if your VCXO is less than 77.5 MHz, you could enter twice the VCXO frequency to simulate the effect of the PLL2 Reference Doubler, for example 61.44 MHz VCXO could have a PDF = 122.88 MHz.
- #5) Calculate updated loop filter.
  - We stick with the auto here, because this tends to design the optimum loop filter. One possibility for tweaking is trying higher phase margins like 75, 80, or 85 degrees.

The screenshot shows the TI Loop Filter Design tool interface. Red circles and numbers indicate the steps for updating the PLL2 loop filter:

- #1: Select the **LoopFilters** tab in the top navigation bar.
- #2: Select the **LOOPFILTER2** sub-tab.
- #3: Select the **Advanced** mode button.
- #4: Update the **Phase Detector Frequency** to 125 MHz.
- #5: Click the **Choose RC Components for me** button.

The **Loop Filter Preferences and Device Settings** section includes the following parameters:

- Filter type: Passive
- Filter Order: 4th Order
- Charge Pump Gain: 3.2 mA
- VCO Gain: 22.35 MHz/V
- VCO Input Capacitance: 0 pF
- VCO Frequency: 2500 MHz
- Phase Detector Frequency: 125 MHz

A circuit diagram shows the charge pump, capacitors C1, C2, C3, C4, and resistors R2, R3, R4 connected to the VCO.

The **Loop Parameters** table shows the following values:

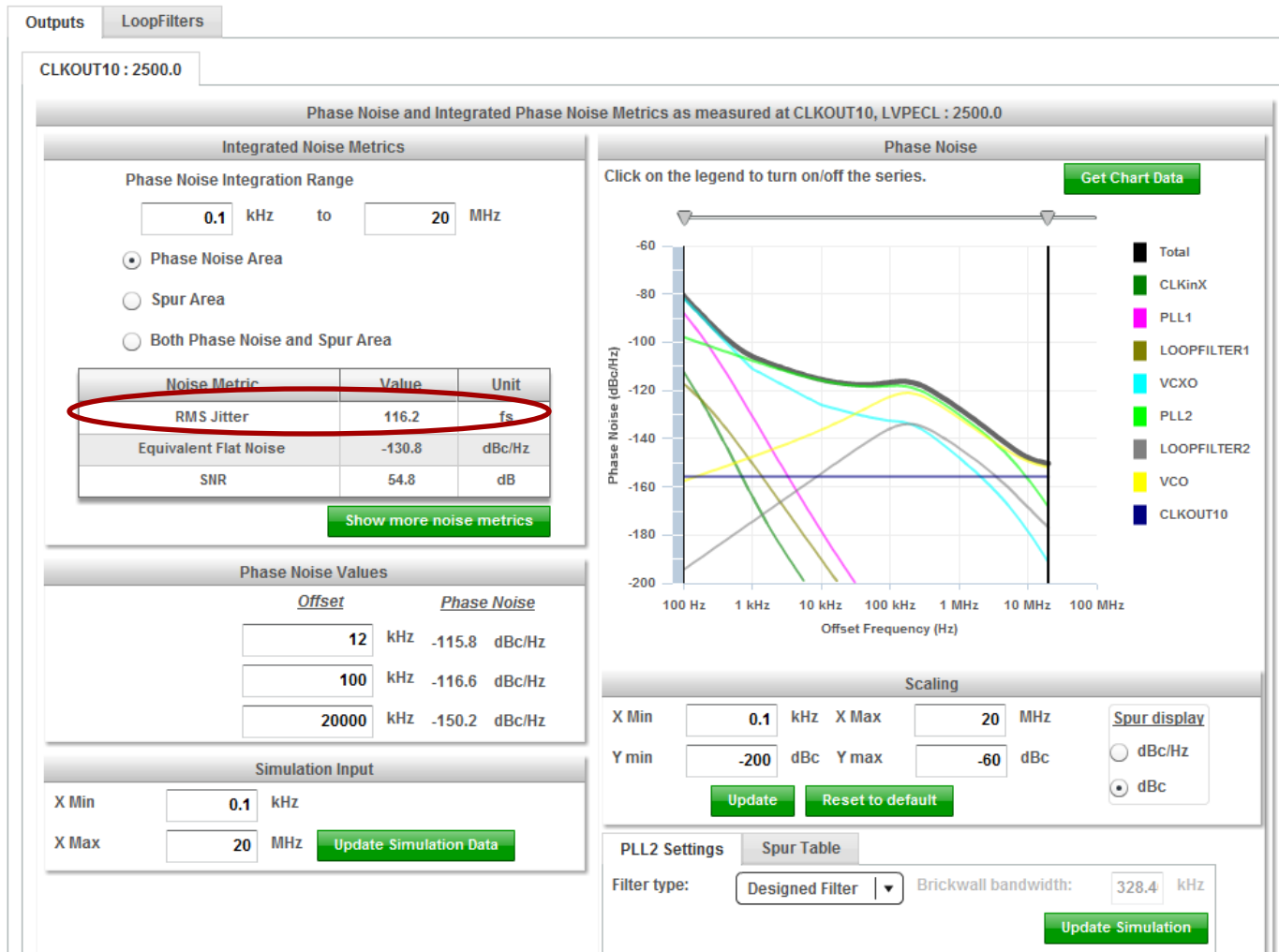
	Design Targets	Actual
Loop Bandwidth	330.65679 kHz	328.4 kHz
Phase Margin	70 deg	68.5 deg
T3/T1 Ratio	50 %	10.22927 %
T4/T3 Ratio	50 %	25.28686 %
Gamma	0.24	0.2

The **Loop Filter Components** section shows the following values:

- Capacitor Value Step: 10%
- C1: 0.027 nF
- C2: 2.7 nF
- C3: 0.01 nF
- C4: 0.01 nF
- Resistor Value Step: 10%
- R2: 0.56 kΩ
- R3: 0.2 kΩ

# Final simulation results using LMK04828 VCO0.

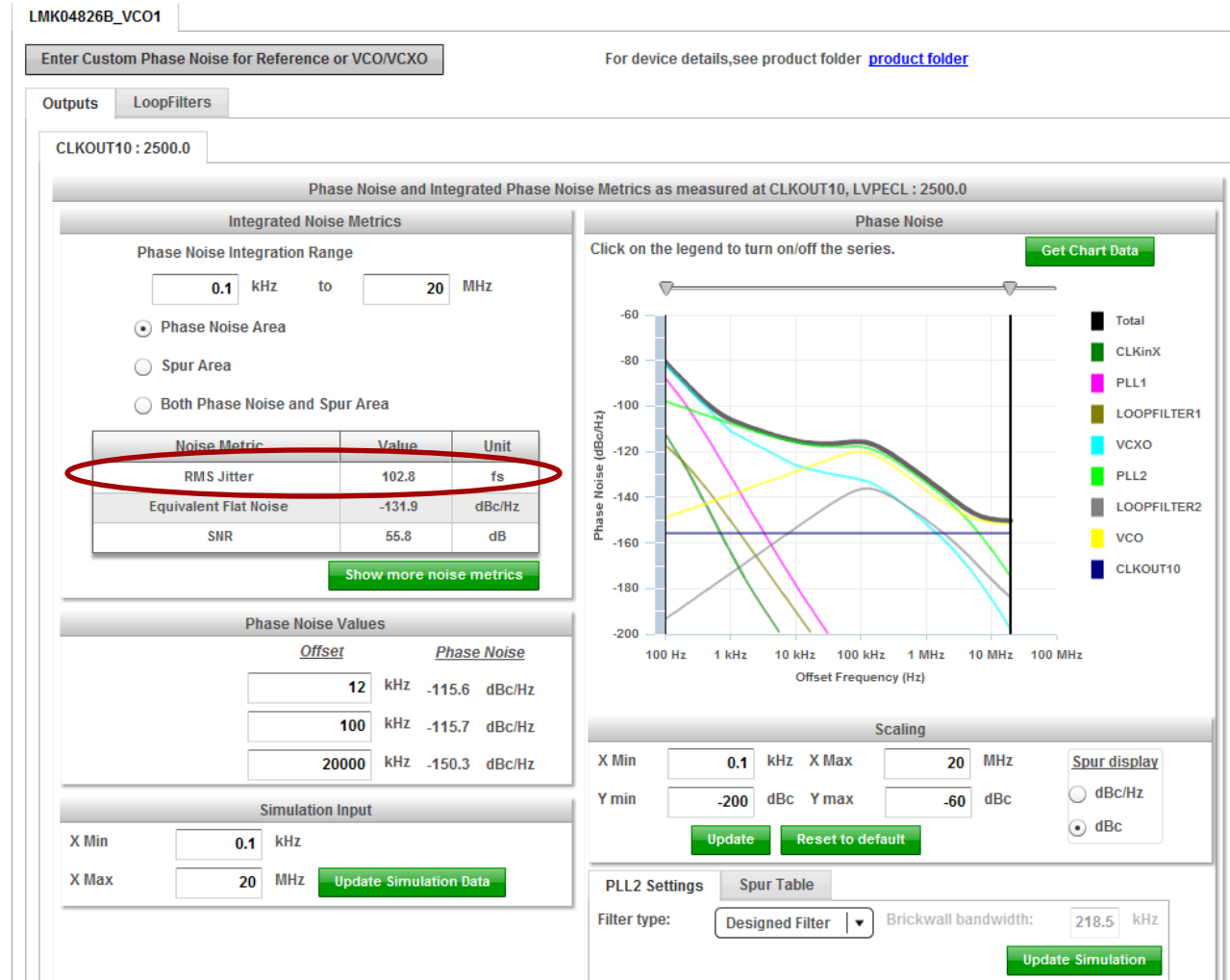
- Here is a [link to the shared project](#).



Note 12 kHz to 20 MHz integration = 116.2 fs rms

# Final simulation results using LMK04826 VCO1.

- In the LMK0482x family, the VCO1 has better open loop performance. Accordingly I've re-created the previous project, but with LMK04826. To return an LMK04826 result, in the search I set a filter for LMK04826.
- With LMK04826 VCO1 at 2500 MHz, **the simulated integrated jitter is 102.8 fs rms.**
- Please find this [link to this shared project](#).

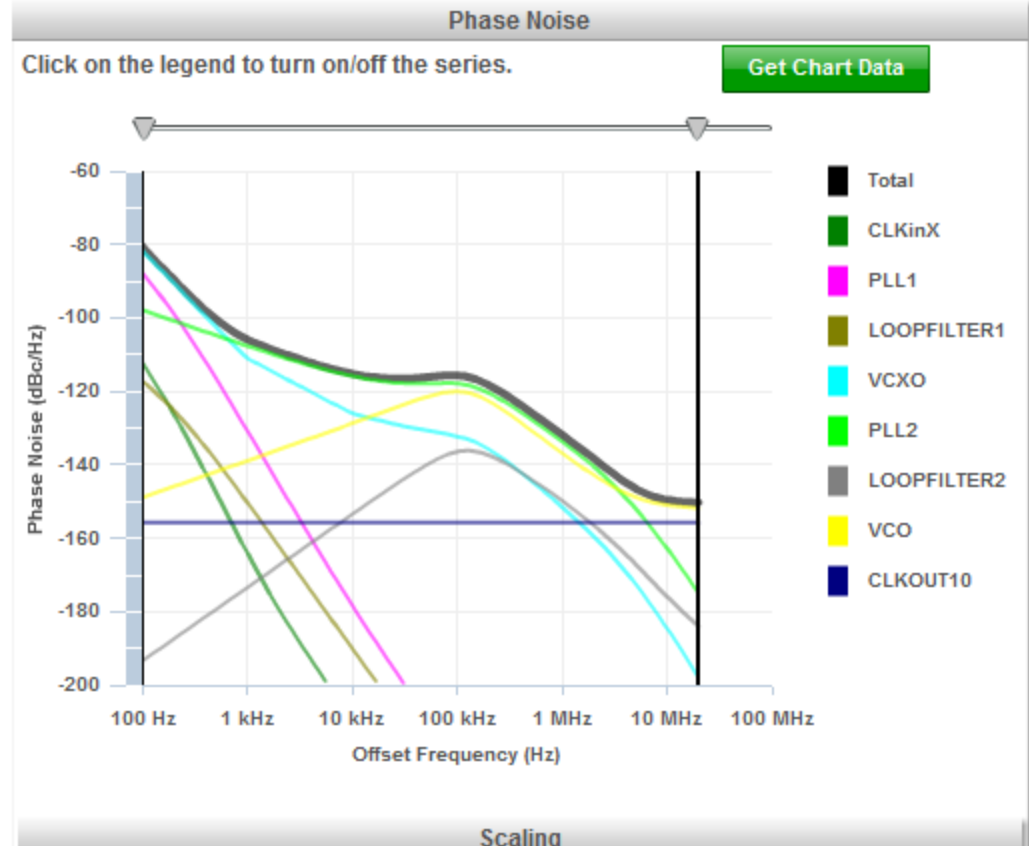


Note 12 kHz to 20 MHz integration = **102.8 fs rms**

# Final note

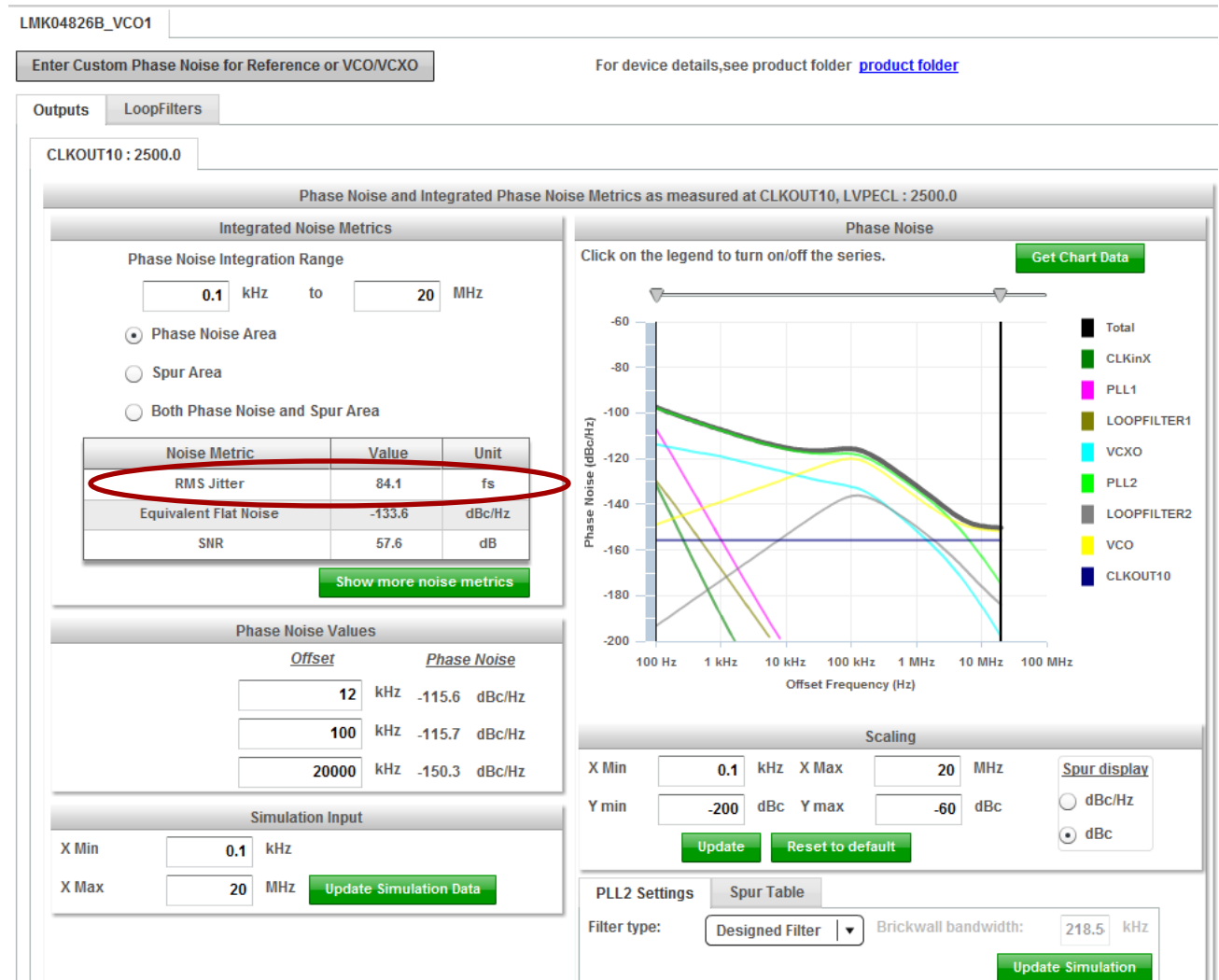
- The VCXO in this design is still limiting performance, as illustrated by the cyan line. VCXO is impacting below 1 kHz.
- Also PLL1 would be limiting performance below 1 kHz. Increase charge pump current to improve PLL1 noise or decreasing PLL1 loop bandwidth (more effective) will filter this noise out.
  - Updating from 40 Hz to 10 Hz loop bandwidth places PLL1 noise about 10 dB below PLL2 noise.

se Metrics as measured at CLKOUT10, LVPECL : 2500.0



# LMK0482x phase noise show case

- With a VCXO that doesn't limit phase noise performance and a loop filter designed such that PLL1 noise does not impact final output, jitter performance is improved in the 100 Hz to 20 MHz integration range. By simulation best case performance is:
  - 84.1 fs rms





# Other Notes

- LMK0482x simulations do not include support for the SYSREF divider. So entering low SYSREF frequencies into the design will cause the LMK0482x to not show as a solution.