Using LMK04828 as JESD204B Fan-out

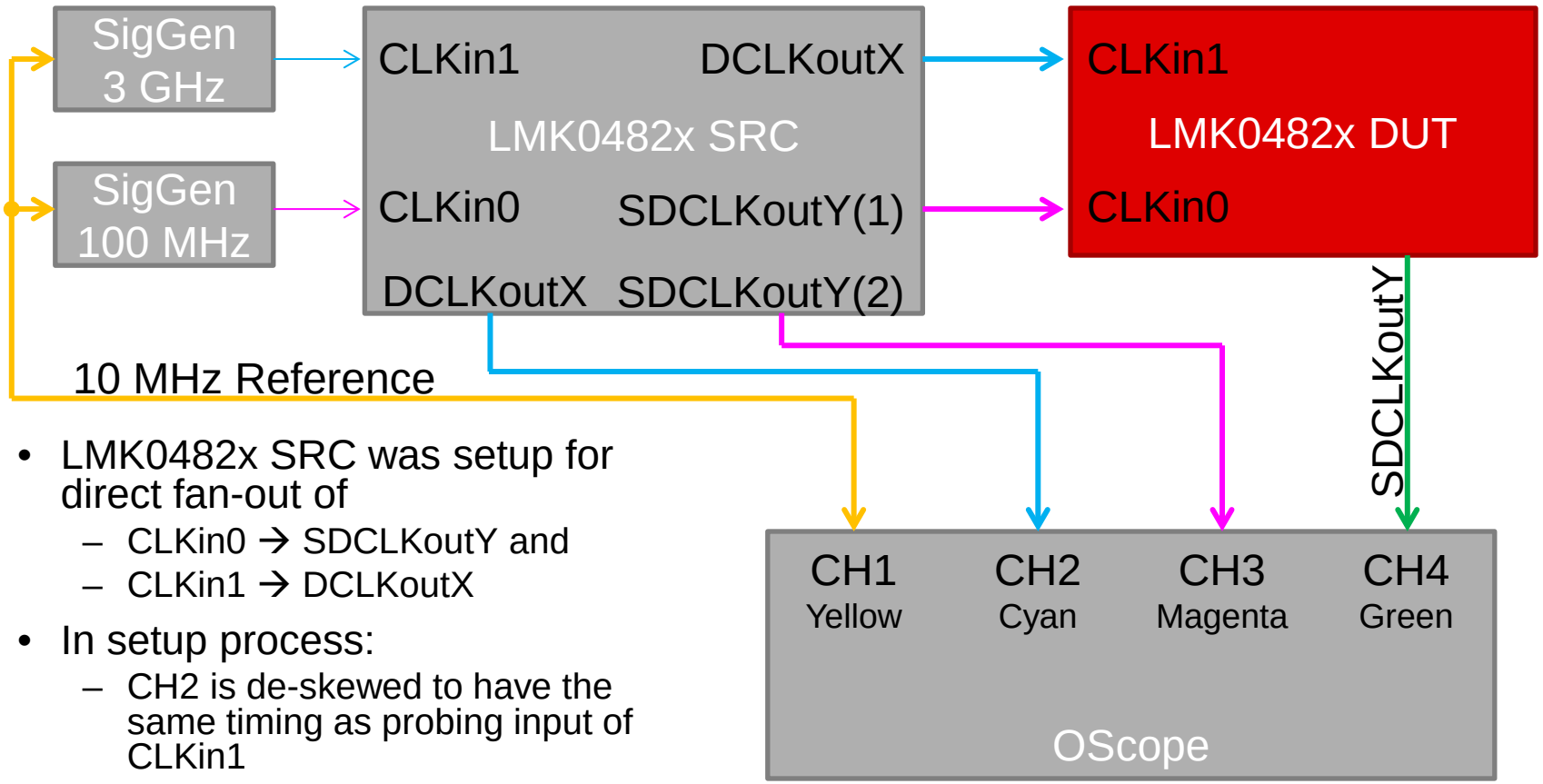
2016-01-08

Quick summary of setup time measurements. Setup time from CLKin0 (SYSREF in) to CLKin1 (Device Clock in).

Description of Traces

- CH1 – Yellow – Is a 10 MHz reference
  - Triggered clock.
- CH2 – Cyan – Is CLKin1 at 3 GHz
- CH3 – Magenta – Input from SYSREF
  - This signal timing is adjusted using the phase delay option on the signal generator.
- CH4 – Green – Output from SYSREF of DUT LMK0482x.
  - When this signal jumps one 3 GHz device clock cycle, the LMK04828 timing has slipped and moved to the next ‘valid window.’

Test Setup



- LMK0482x SRC was setup for direct fan-out of
  - CLKin0 → SDCLKoutY and
  - CLKin1 → DCLKoutX
- In setup process:
  - CH2 is de-skewed to have the same timing as probing input of CLKin1
  - Phase of CH3 is de-skewed to have the same timing as probing input of CLKin0

Data Summary of room temp data

	Absolute Time	Timing Window
Before start of window	6327.0 ps	
Invalid timing window **(setup/hold time)**		16.2 ps
At start of window	6343.2 ps	
VALID timing window		**314.1 ps**
At end of window	6657.3 ps	
Invalid timing window **(setup/hold time)**		19.9 ps
At beginning of next window	6677.2 ps	

At 3 GHz, clock period is 333 + 1/3 ps.
333.3 ps – 314.1 ps = 19.2 ps invalid window (setup/hold time).

Conclusion, about a 20 ps setup/hold time was measured at 3 GHz.
This setup/hold time should not be impacted by frequency but should be increased for PVT variation.
Centering rising edge of SYNC on falling edge of 3 GHz clock appears to be optimum.

Before start of window, 6.3269916 ns

	Value	Mean	Min	Max	St Dev	Count	Info
C1C2 Dely	-613.8ps	-638.79398p	-667.4p	-602.3p	12.44p	289.0	
C1C3 Dely	5.72ns	5.6881976n	5.659n	5.72n	12.17p	289.0	
C1C4 Dely	4.345ns	4.3355565n	4.295n	4.367n	13.02p	289.0	
C2 Period	326.1ps	334.32773p	313.3p	355.4p	7.541p	289.0	
C4 Mean	-1.978mV	-2.8328145m	-6.209m	2.546m	1.418m	289.0	
C4 Ampl	700.0mV	714.72266m	680.0m	760.0m	13.55m	289.0	
C2C3 Dely*	6.333ns	6.3269916n	6.307n	6.345n	6.445p	289.0	

At start of window, 6.3432361 ns

Note constant phase output of SYSREF to next slide

At end of window, 6.6573149 ns

Note constant phase output of SYSREF to prior slide

	Value	Mean	Min	Max	St Dev	Count	Info
C1C2 Dely	-644.0ps	-636.63132p	-673.4p	-605.1p	11.13p	634.0	
C1C3 Dely	6.017ns	6.0206836n	5.985n	6.056n	11.96p	634.0	
C1C4 Dely	4.654ns	4.6684057n	4.626n	4.709n	15.17p	634.0	
C2 Period	331.1ps	332.67384p	306.5p	355.4p	8.666p	634.0	
C4 Mean	-4.222mV	-2.0604957m	-6.316m	2.079m	1.502m	634.0	
C4 Ampl	698.8mV	714.86861m	680.0m	761.3m	14.85m	634.0	
C2C3 Dely*	6.661ns	6.6573149n	6.632n	6.681n	6.938p	634.0	

At beginning of next window, 6.6771549 ns

	Value	Mean	Min	Max	St Dev	Count	Info
C1C2 Dely	-621.9ps	-633.48558p	-674.4p	-602.7p	10.83p	427.0	
C1C3 Dely	6.059ns	6.0436693n	6.013n	6.073n	11.37p	427.0	
C1C4 Dely	5.01ns	5.0035202n	4.972n	5.035n	13.19p	427.0	
C2 Period	336.0ps	333.07535p	312.1p	352.4p	7.266p	427.0	
C4 Mean	-1.329mV	-1.5168246m	-6.197m	2.749m	1.468m	427.0	
C4 Ampl	720.0mV	732.17663m	700.0m	761.3m	13.38m	427.0	
C2C3 Dely*	6.681ns	6.6771549n	6.657n	6.699n	6.463p	427.0	