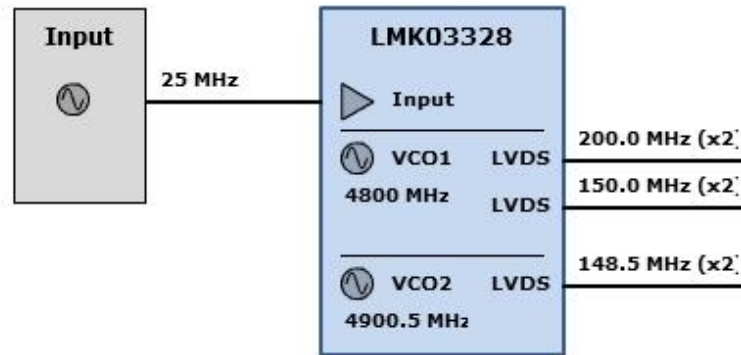


WEBENCH[®] Clock Architect

Project Report

Project: 3456224/53 Project 53 - [LMK03328]
Created: 5/29/17 5:24:13 AM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	200	LVDS	1
fixed1	150	LVDS	1
fixed2	148.5	LVDS	1
fixed_0	200	LVDS	1
fixed_1	150	LVDS	1
fixed_2	148.5	LVDS	1

Options

Name	Design Value
Automatically Select	No
Input Frequencies	
Part Filter	LMK03328

Properties

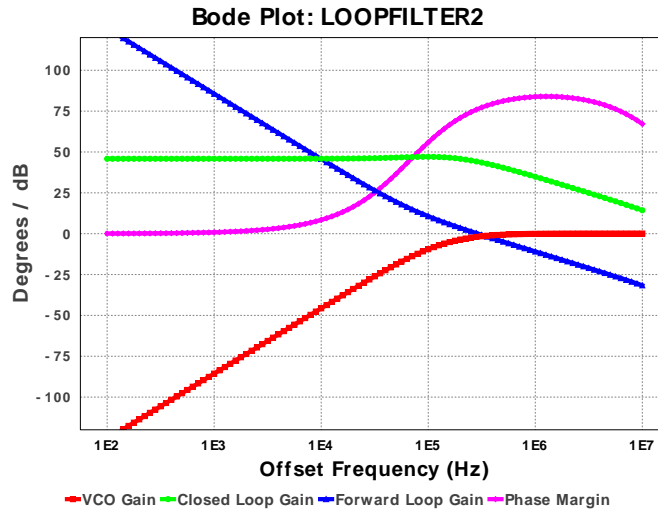
Name	Design Value
External Sources	none
Total BOM Cost	\$10.0
Total Current	605.0 mA
Total Footprint	49.0 mm ²



User ID = 3456224
 Design Id = 1817
 Device = LMK03328
 Created = 5/29/17 5:24:13 AM

WEBENCH® Clock Design Report

Loop Filter: LMK03328 LOOPFILTER2



Preferences

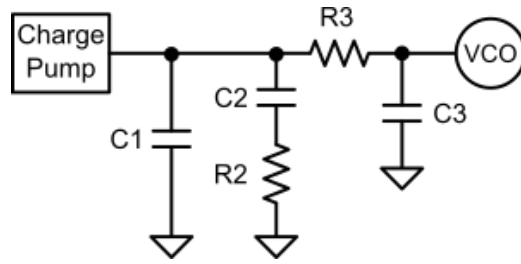
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	45.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4900.50 MHz
Phase Det. Frequency	25.00 MHz
Filter type	designed
Brickwall Bandwidth	291.8260213171288 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	196
PLL Numerator	1.0
PLL Denominator	50.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

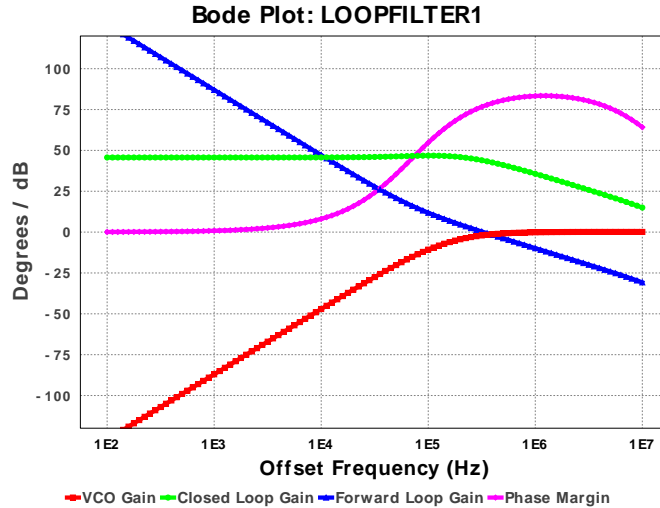
Name	Design Value	Forced	Actual Value
Loop Bandwidth	228.019 kHz	N	291.826 kHz
Phase Margin	70.00 deg	N	76.354 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.052

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	1.80 nF	N	N
C3	Open	Y	N
C4	Open	N	N
R2	1.317 kohms	Y	N
R3	6.299 kohms	Y	N



Loop Filter: LMK03328 LOOPFILTER1



Preferences

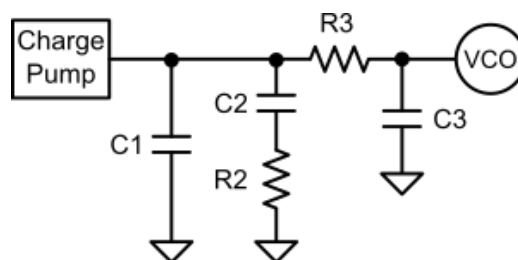
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	45.00 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	4800.00 MHz
Phase Det. Frequency	25.00 MHz
Filter type	designed
Brickwall Bandwidth	328.02080631613217 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	192
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	228.019 kHz	N	328.021 kHz
Phase Margin	70.00 deg	N	77.071 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.073

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	1.50 nF	N	N
C3	Open	Y	N
C4	Open	N	N
R2	1.517 kohms	Y	N
R3	6.299 kohms	Y	N



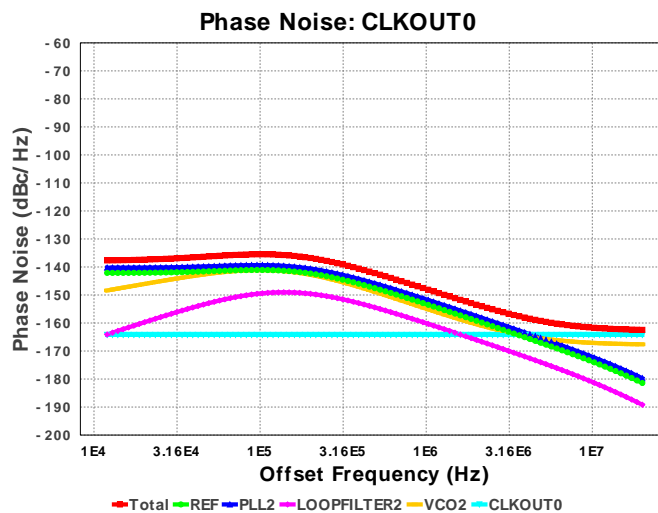
Output Block: LMK03328 LMK03328 : CLKOUT0 as LVDS output, 148.5 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-152.151 dBc/Hz
RMS Jitter	167.276 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.156 mrad
EVM	0.016%
SNR	76.133 dB
Spur	-79.133 dBc
Jitter (Pk-Pk)	1192.764 fs
Jitter (Cycle to Cycle Pk)	2385.528 fs
Jitter (Cycle to Cycle RMS)	236.565 fs
A/D ENOB	12.361 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-137.65	-135.47	-162.44
REF	-142.11	-141.06	-181.4
PLL2	-140.23	-139.34	-179.71
LOOPFILTER2	-164.09	-149.48	-189.17
VCO2	-148.38	-141.11	-167.61
CLKOUT0	-164.23	-164.23	-164.23



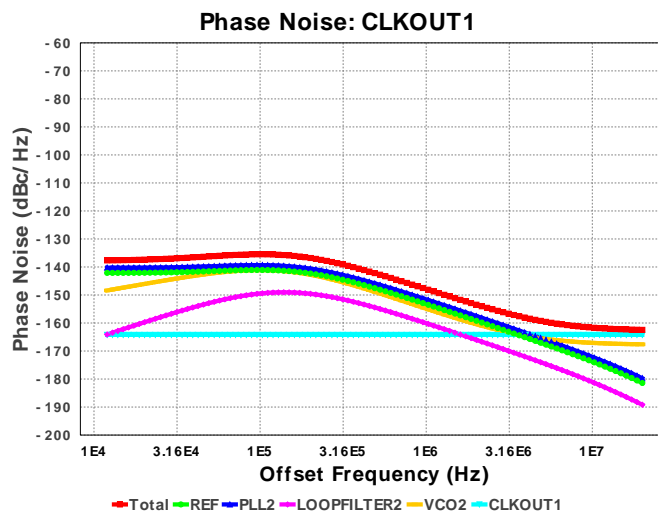
Output Block: LMK03328 LMK03328 : CLKOUT1 as LVDS output, 148.5 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-152.151 dBc/Hz
RMS Jitter	167.276 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.156 mrad
EVM	0.016%
SNR	76.133 dB
Spur	-79.133 dBc
Jitter (Pk-Pk)	1192.764 fs
Jitter (Cycle to Cycle Pk)	2385.528 fs
Jitter (Cycle to Cycle RMS)	236.565 fs
A/D ENOB	12.361 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-137.65	-135.47	-162.44
REF	-142.11	-141.06	-181.4
PLL2	-140.23	-139.34	-179.71
LOOPFILTER2	-164.09	-149.48	-189.17
VCO2	-148.38	-141.11	-167.61
CLKOUT1	-164.23	-164.23	-164.23



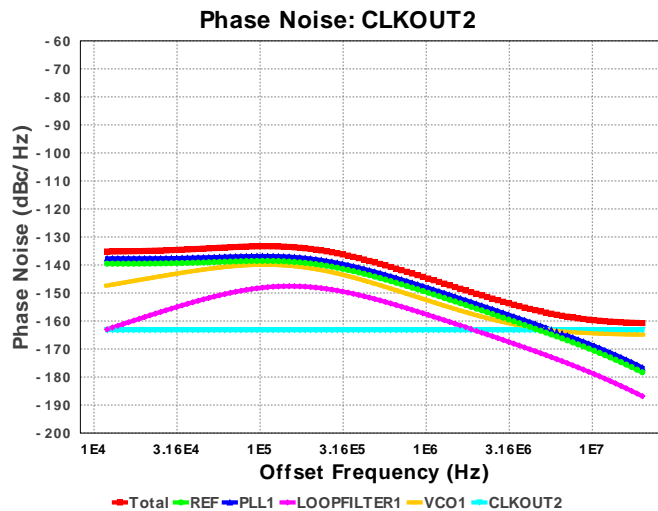
Output Block: LMK03328 LMK03328 : CLKOUT2 as LVDS output, 200.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-149.50 dBc/Hz
RMS Jitter	168.528 fs
RMS Phase Error (deg)	0.012 deg
RMS Phase Error	0.212 mrad
EVM	0.021%
SNR	73.482 dB
Spur	-76.482 dBc
Jitter (Pk-Pk)	1201.691 fs
Jitter (Cycle to Cycle Pk)	2403.381 fs
Jitter (Cycle to Cycle RMS)	238.335 fs
A/D ENOB	11.921 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-135.2	-133.33	-160.75
REF	-139.53	-138.55	-178.3
PLL1	-137.66	-136.83	-176.61
LOOPFILTER1	-162.97	-148.19	-186.82
VCO1	-147.35	-139.92	-164.85
CLKOUT2	-163.22	-163.22	-163.22



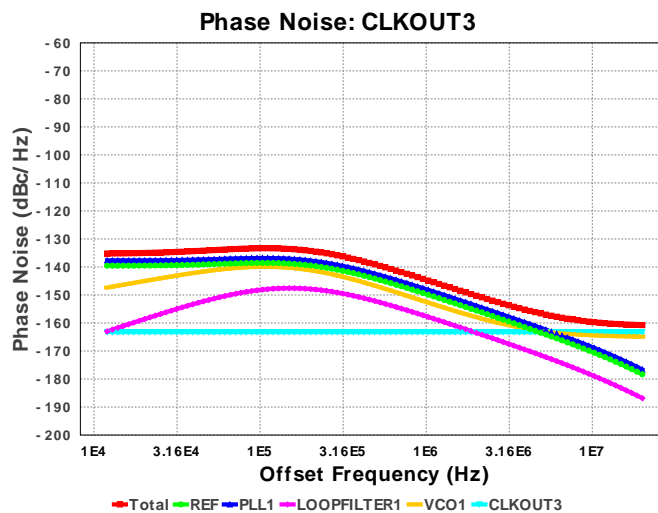
Output Block: LMK03328 LMK03328 : CLKOUT3 as LVDS output, 200.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-149.50 dBc/Hz
RMS Jitter	168.528 fs
RMS Phase Error (deg)	0.012 deg
RMS Phase Error	0.212 mrad
EVM	0.021%
SNR	73.482 dB
Spur	-76.482 dBc
Jitter (Pk-Pk)	1201.691 fs
Jitter (Cycle to Cycle Pk)	2403.381 fs
Jitter (Cycle to Cycle RMS)	238.335 fs
A/D ENOB	11.921 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-135.2	-133.33	-160.75
REF	-139.53	-138.55	-178.3
PLL1	-137.66	-136.83	-176.61
LOOPFILTER1	-162.97	-148.19	-186.82
VCO1	-147.35	-139.92	-164.85
CLKOUT3	-163.22	-163.22	-163.22



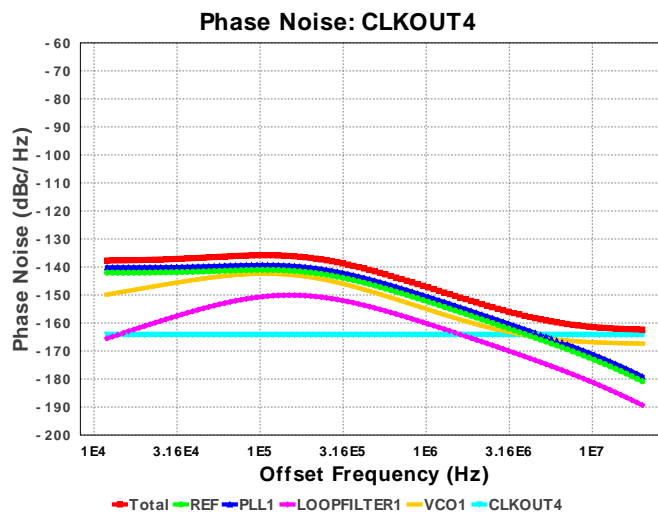
Output Block: LMK03328 LMK03328 : CLKOUT4 as LVDS output, 150.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-151.922 dBc/Hz
RMS Jitter	170.027 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.16 mrad
EVM	0.016%
SNR	75.904 dB
Spur	-78.904 dBc
Jitter (Pk-Pk)	1212.377 fs
Jitter (Cycle to Cycle Pk)	2424.753 fs
Jitter (Cycle to Cycle RMS)	240.454 fs
A/D ENOB	12.323 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-137.69	-135.82	-162.32
REF	-142.03	-141.05	-180.8
PLL1	-140.16	-139.32	-179.11
LOOPFILTER1	-165.47	-150.69	-189.32
VCO1	-149.85	-142.41	-167.35
CLKOUT4	-164.2	-164.2	-164.2



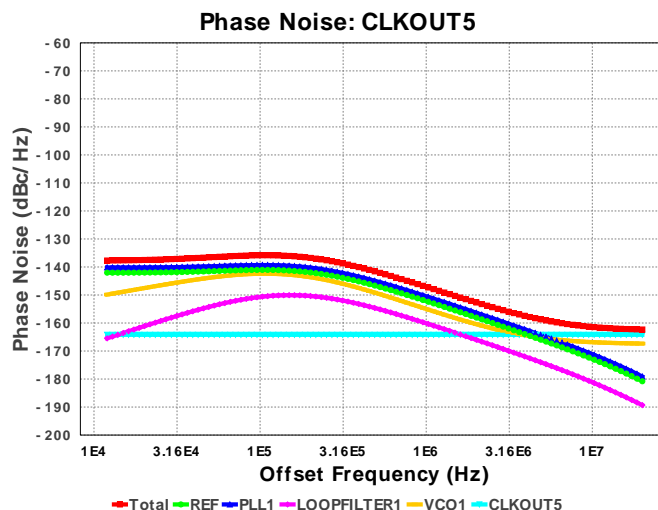
Output Block: LMK03328 LMK03328 : CLKOUT5 as LVDS output, 150.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-151.922 dBc/Hz
RMS Jitter	170.027 fs
RMS Phase Error (deg)	0.009 deg
RMS Phase Error	0.16 mrad
EVM	0.016%
SNR	75.904 dB
Spur	-78.904 dBc
Jitter (Pk-Pk)	1212.377 fs
Jitter (Cycle to Cycle Pk)	2424.753 fs
Jitter (Cycle to Cycle RMS)	240.454 fs
A/D ENOB	12.323 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-137.69	-135.82	-162.32
REF	-142.03	-141.05	-180.8
PLL1	-140.16	-139.32	-179.11
LOOPFILTER1	-165.47	-150.69	-189.32
VCO1	-149.85	-142.41	-167.35
CLKOUT5	-164.2	-164.2	-164.2



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