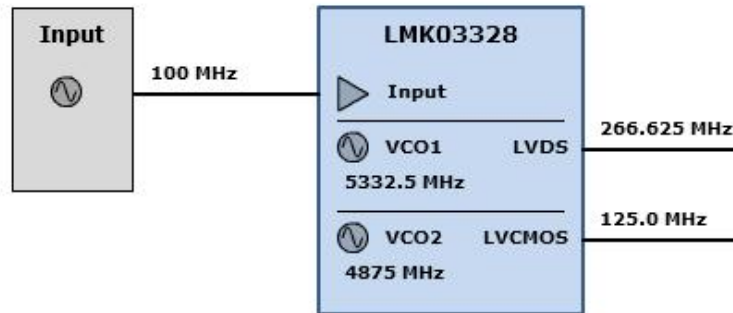


WEBENCH[®] Clock Architect

Project Report

Project: 4291614/51 Project 51 - [LMK03328]
Created: 7/24/18 11:07:10 PM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	125	Any	1
fixed1	266.625	Any	1

Options

Name	Design Value
Automatically Select	No
Input Frequencies	
Part Filter	LMK03328

Properties

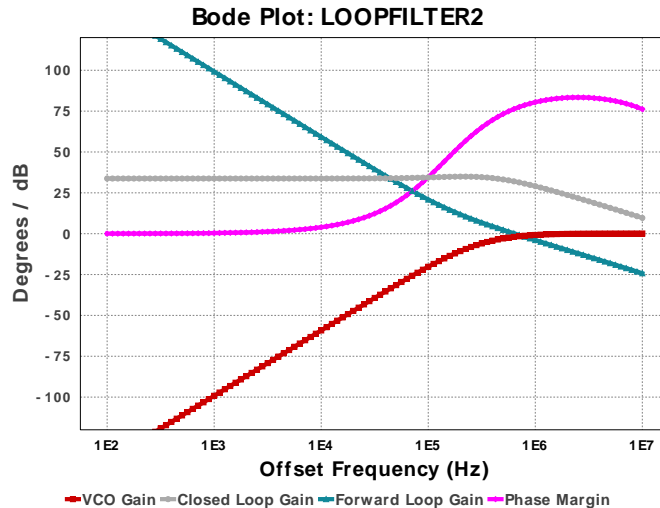
Name	Design Value
External Sources	none
Total BOM Cost	\$10.0
Total Current	402.5 mA
Total Footprint	49.0 mm ²



User ID = 4291614
 Design Id = 179
 Device = LMK03328
 Created = 7/24/18 11:07:10 PM

WEBENCH® Clock Design Report

Loop Filter: LMK03328 LOOPFILTER2



Preferences

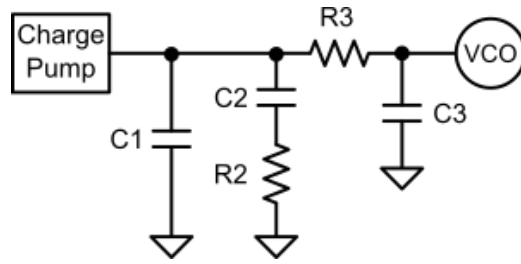
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	43.333 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	5000.00 MHz
Phase Det. Frequency	100.00 MHz
Filter type	designed
Brickwall Bandwidth	620.0939474768744 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	50
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

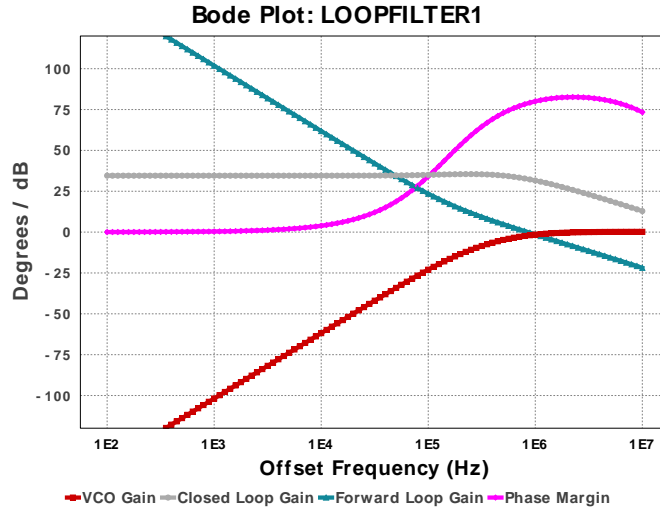
Name	Design Value	Forced	Actual Value
Loop Bandwidth	479.495 kHz	N	620.094 kHz
Phase Margin	70.00 deg	N	83.14 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.135

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	3.30 nF	N	Y
C3	Open	Y	N
C4	Open	N	N
R2	0.735 kohms	Y	N
R3	0.518 kohms	Y	Y



Loop Filter: LMK03328 LOOPFILTER1



Preferences

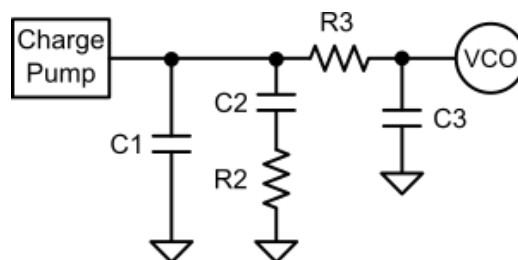
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	1.60 mA
VCO Gain	48.875 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	5332.50 MHz
Phase Det. Frequency	100.00 MHz
Filter type	designed
Brickwall Bandwidth	219.48357625822518 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	53
PLL Numerator	13.0
PLL Denominator	40.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	542.733 kHz	N	219.484 kHz
Phase Margin	70.00 deg	N	63.528 deg
T3/T1Ratio	50.00 %	N	11.411 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	21.629

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.255 nF	Y	Y
C2	33.00 nF	N	Y
C3	0.035 nF	Y	Y
R2	1.028 kohms	Y	Y
R3	1.136 kohms	Y	Y



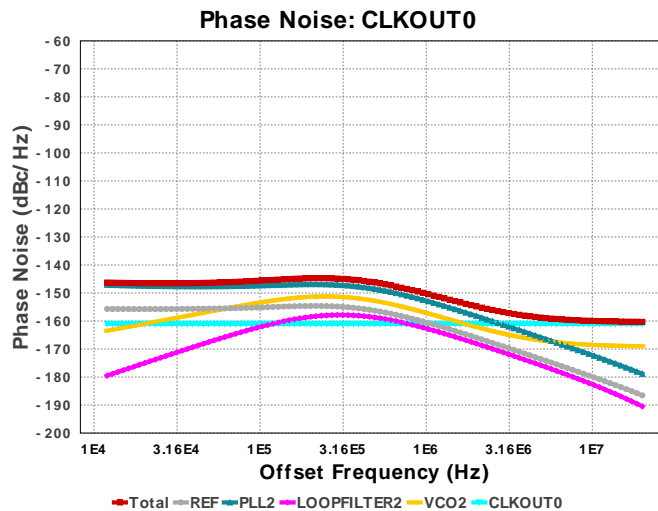
Output Block: LMK03328 LMK03328 : CLKOUT0 as LVCMOS output, 125.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-156.347 dBc/Hz
RMS Jitter	122.591 fs
RMS Phase Error (deg)	0.006 deg
RMS Phase Error	0.096 mrad
EVM	0.01%
SNR	80.329 dB
Spur	-83.329 dBc
Jitter (Pk-Pk)	874.137 fs
Jitter (Cycle to Cycle Pk)	1748.275 fs
Jitter (Cycle to Cycle RMS)	173.37 fs
A/D ENOB	13.058 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-145.7	-144.58	-160.29
REF	-155.46	-154.97	-186.54
PLL2	-146.83	-147.13	-178.83
LOOPFILTER2	-180.03	-166.11	-196.13
VCO2	-156.06	-149.49	-169.01
CLKOUT0	-161.01	-161.01	-161.01



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

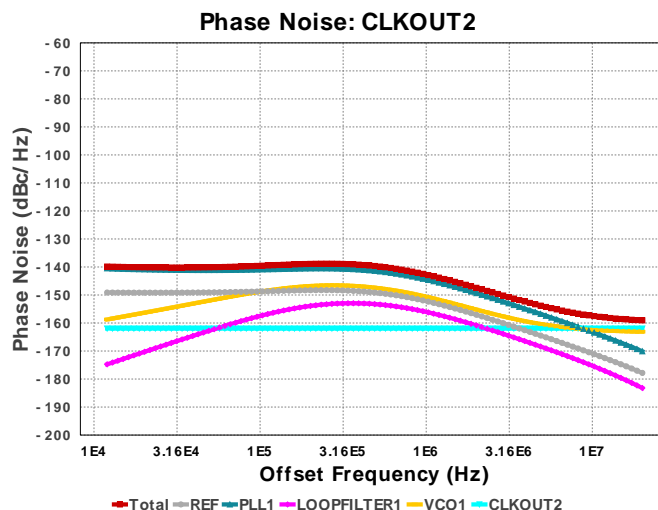
Output Block: LMK03328 LMK03328 : CLKOUT2 as LVDS output, 266.625 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-148.383 dBc/Hz
RMS Jitter	143.771 fs
RMS Phase Error (deg)	0.014 deg
RMS Phase Error	0.241 mrad
EVM	0.024%
SNR	72.365 dB
Spur	-75.365 dBc
Jitter (Pk-Pk)	1025.155 fs
Jitter (Cycle to Cycle Pk)	2050.311 fs
Jitter (Cycle to Cycle RMS)	203.322 fs
A/D ENOB	11.735 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-126.14	-131.89	-159.55
REF	-148.98	-149.08	-232.2
PLL1	-138.3	-139.19	-222.45
LOOPFILTER1	-147.74	-147.07	-202.84
VCO1	-126.47	-133.06	-163.25
CLKOUT2	-161.97	-161.97	-161.97



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

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