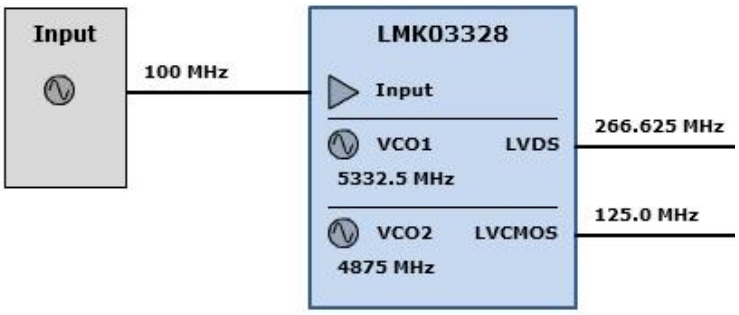
WEBENCH® Clock Architect

Project Report

Project: 4291614/53 Project 53 - [LMK03328]
Created: 7/24/18 11:35:56 PM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	125	Any	1
fixed1	266.625	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	No
Part Filter	LMK03328

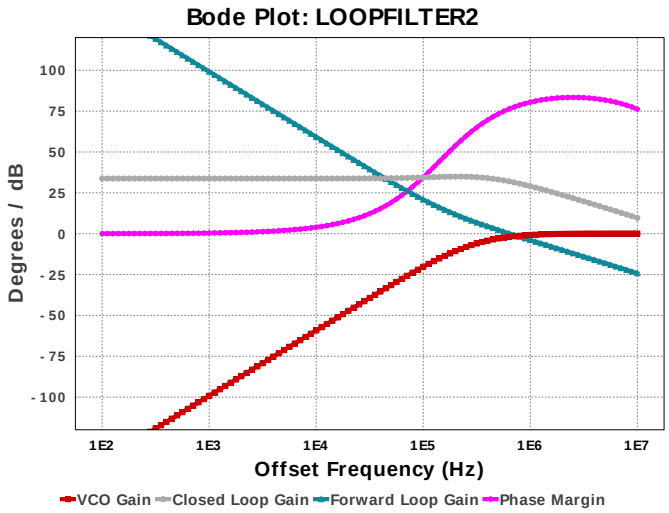
Properties

Name	Design Value
External Sources	none
Total BOM Cost	$10.0
Total Current	402.5 mA
Total Footprint	49.0 mm^2

User ID = 4291614
Design Id = 181
Device = LMK03328
Created = 7/24/18 11:35:56 PM

WEBENCH ® Clock Design Report

Loop Filter: LMK03328 LOOPFILTER2



Preferences

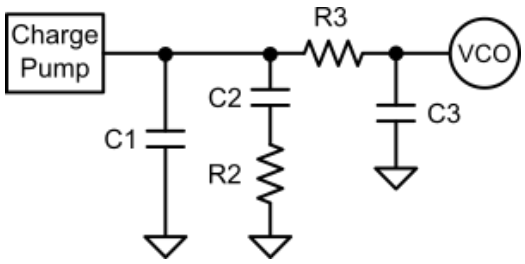
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	43.333 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	5000.00 MHz
Phase Det. Frequency	100.00 MHz
Filter type	designed
Brickwall Bandwidth	620.0939474768744 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	50
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

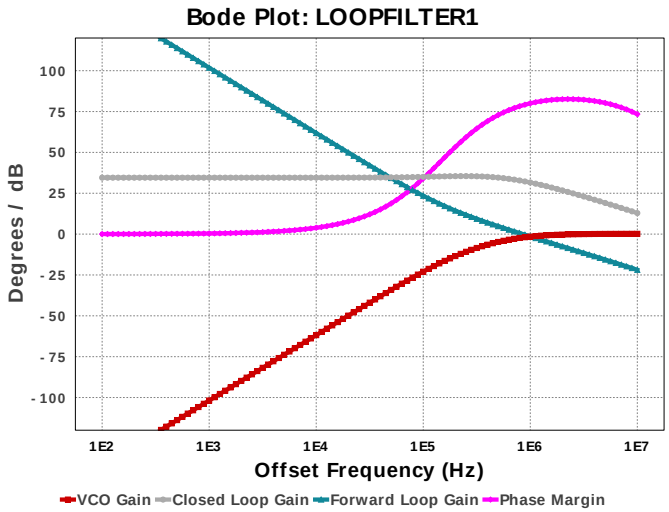
Name	Design Value	Forced	Actual Value
Loop Bandwidth	479.495 kHz	N	620.094 kHz
Phase Margin	70.00 deg	N	83.14 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	0.135

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	3.30 nF	N	Y
C3	Open	Y	N
C4	Open	N	N
R2	0.735 kohms	Y	N
R3	6.299 kohms	Y	N



Loop Filter: LMK03328 LOOPFILTER1



Preferences

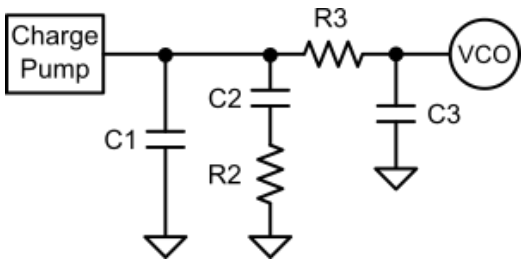
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	6.40 mA
VCO Gain	48.875 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	5332.50 MHz
Phase Det. Frequency	100.00 MHz
Filter type	designed
Brickwall Bandwidth	842.6799594430812 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	53
PLL Numerator	13.0
PLL Denominator	40.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	542.733 kHz	N	842.68 kHz
Phase Margin	70.00 deg	N	88.268 deg
T3/T1Ratio	50.00 %	N	0.00 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	3.771

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.005 nF	Y	N
C2	33.00 nF	N	Y
C3	Open	Y	N
C4	Open	N	N
R2	0.903 kohms	Y	N
R3	6.299 kohms	Y	N



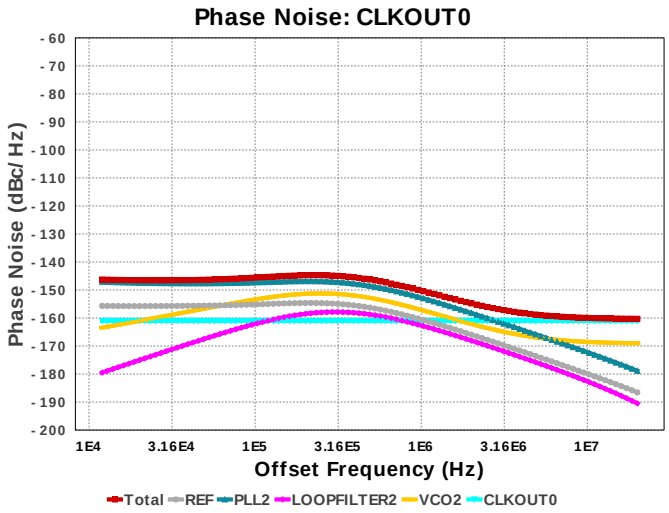
Output Block: LMK03328 LMK03328 : CLKOUT0 as LVCMOS output, 125.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-156.223 dBc/Hz
RMS Jitter	124.348 fs
RMS Phase Error (deg)	0.006 deg
RMS Phase Error	0.098 mrad
EVM	0.01%
SNR	80.205 dB
Spur	-83.205 dBc
Jitter (Pk-Pk)	886.663 fs
Jitter (Cycle to Cycle Pk)	1773.327 fs
Jitter (Cycle to Cycle RMS)	175.855 fs
A/D ENOB	13.037 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-145.7	-144.44	-160.29
REF	-155.46	-154.97	-186.54
PLL2	-146.83	-147.13	-178.83
LOOPFILTER2	-172.53	-158.61	-190.47
VCO2	-156.06	-149.49	-169.01
CLKOUT0	-161.01	-161.01	-161.01



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.

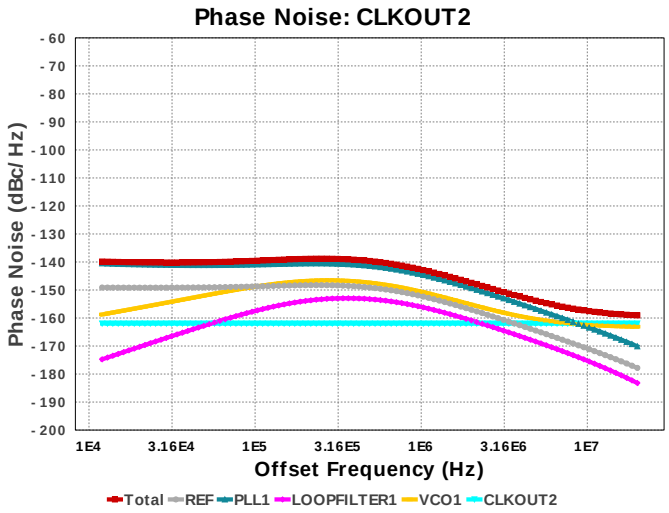
Output Block: LMK03328 LMK03328 : CLKOUT2 as LVDS output, 266.625 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-150.825 dBc/Hz
RMS Jitter	108.536 fs
RMS Phase Error (deg)	0.01 deg
RMS Phase Error	0.182 mrad
EVM	0.018%
SNR	74.807 dB
Spur	-77.807 dBc
Jitter (Pk-Pk)	773.914 fs
Jitter (Cycle to Cycle Pk)	1547.827 fs
Jitter (Cycle to Cycle RMS)	153.493 fs
A/D ENOB	12.141 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	12	100	20000
Total	-135.6	-138.96	-159.05
REF	-149.08	-149.23	-177.79
PLL1	-140.45	-141.38	-170.07
LOOPFILTER1	-153.74	-153.01	-183.2
VCO1	-137.74	-144.36	-163.1
CLKOUT2	-161.97	-161.97	-161.97



Spurs are not displayed in this PDF version of the phase noise graph. See the simulation page in Clock Architect to view the spurs in the phase noise graph.