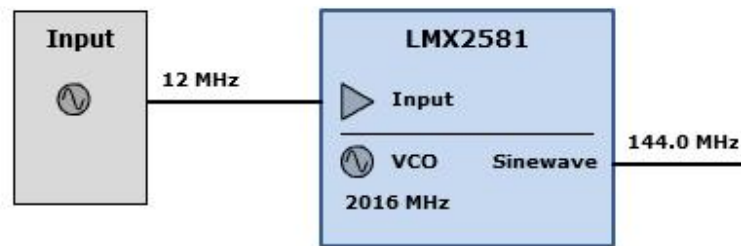


WEBENCH[®] Clock Architect

Project Report

Project: 4249703/5 Project 5 - [LMX2581]
Created: 1/9/17 10:27:07 PM



Block Diagram

My Comments

No comments

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	144	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	No

Properties

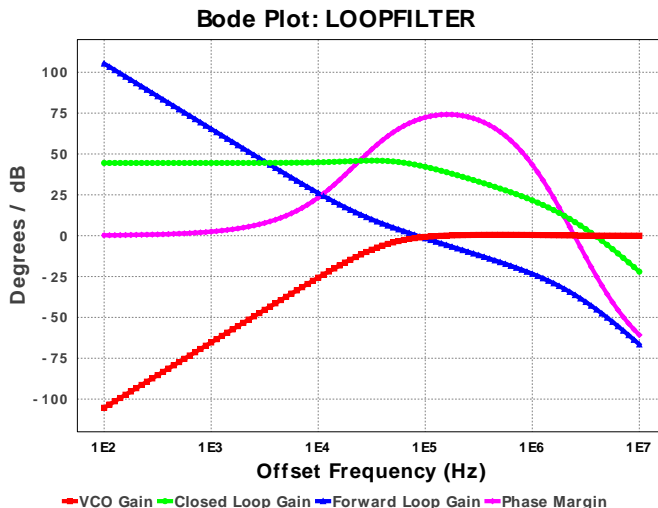
Name	Design Value
External Sources	none
Total BOM Cost	\$7.0
Total Current	198.0 mA
Total Footprint	32.0 mm ²



User ID = 4249703
 Design Id = 5
 Device = LMX2581
 Created = 1/9/17 10:27:07 PM

WEBENCH® Clock Design Report

Loop Filter: LMX2581 LOOPFILTER



Preferences

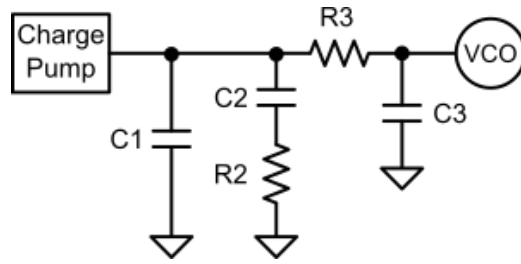
Name	Design Value
Filter Type	Passive
Filter Order	3rd Order
Op Amp Gain	1.00
Charge Pump Gain	2.64 mA
VCO Gain	18.279 MHz/V
VCO Input Capacitance	0.00 pF
VCO Frequency	2016.00 MHz
Phase Det. Frequency	12.00 MHz
Filter type	designed
Brickwall Bandwidth	253.32076974612337 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	168
PLL Numerator	0.0
PLL Denominator	1.0
Reference spurs	enabled
Fractional spurs	enabled
Subfractional spurs	enabled
Other spurs	enabled

Parameters

Name	Design Value	Forced	Actual Value
Loop Bandwidth	84.636 kHz	N	253.321 kHz
Phase Margin	70.00 deg	N	60.866 deg
T3/T1Ratio	50.00 %	N	19.54 %
T4/T3Ratio	0.00 %	N	0.00 %
Gamma	0.24	N	19.123

Loop Filter Components

Name	Target Value	Fixed	Forced
C1	0.039 nF	N	N
C2	3.90 nF	N	N
C3	0.004 nF	N	N
C4	Open	N	N
R2	6.10 kohms	N	Y
R3	15.00 kohms	N	N



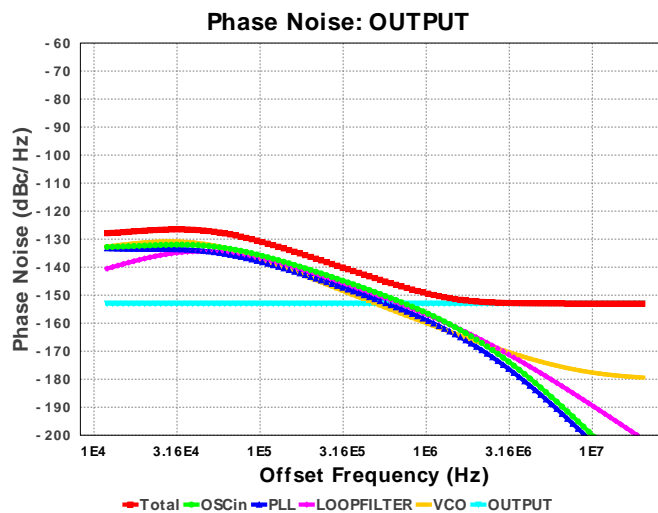
Output Block: LMX2581 LMX2581 : OUTPUT as SINEWAVE output, 144.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-146.194 dBc/Hz
RMS Jitter	342.487 fs
RMS Phase Error (deg)	0.018 deg
RMS Phase Error	0.31 mrad
EVM	0.031%
SNR	70.176 dB
Spur	-73.176 dBc
Jitter (Pk-Pk)	2442.10 fs
Jitter (Cycle to Cycle Pk)	4884.20 fs
Jitter (Cycle to Cycle RMS)	484.349 fs
A/D ENOB	11.371 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

Offset	Total	OSCin	PLL	LOOPFILTER	VCO	OUTPUT
12 kHz	-129.59	-133.17	-133.64	-145.12	-138.25	-153
100 kHz	-130.7	-133.16	-135.42	-143.81	-144.68	-153
20000 kHz	-152.99	-217.47	-220.07	-201.22	-179.39	-153



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You should completely validate and test your design implementation to confirm the system functionality for your application prior to production.

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