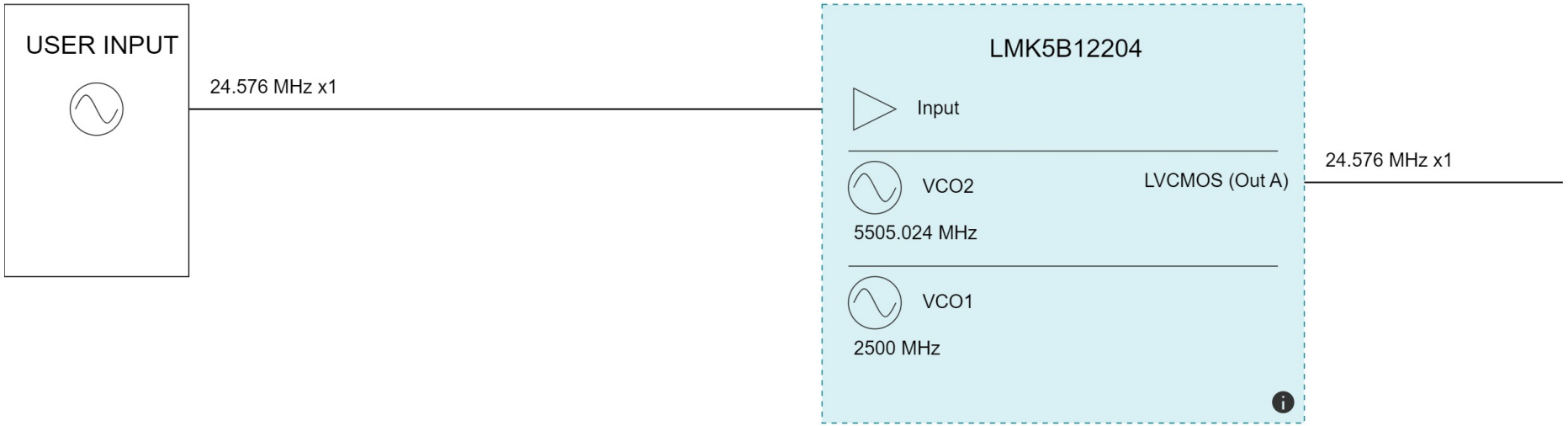
Clock tree architect design report

1. Selected solution details:

1.a. Block diagram:



https://webench.ti.com/clock-tree-architect

1.b. Solution details:

Devices	Area (mm²)	BOM price estimate ($)	Jitter (fs rms)	Power (mW)
LMK5B12204	49.00	6.500	125 Out A: 125	1056

1.c. Device details:

Devices	Area (mm²)	BOM price estimate ($)	Current (mA)	Power (mW)
LMK5B12204	49.00	6.500	320	1056

1.d. Output details:

Devices	Output	Frequency	Format	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Deterministic phase
LMK5B12204	Out A	24.576 MHz	LVCMOS	1	125	-160	Yes [1]

[1] Requires some settings at device level. Kindly, refer the datasheet.

2. Other solutions:

Devices	Area (mm²)	BOM price estimate ($)	Jitter (fs rms)	Power (mW)
LMK05318	49.00	8.760	125	1030
LMK05028	81.00	14.960	160	713
LMK61E08 and CDC3RL02	36.28	12.650	1156	520
LMK04133	229.00	23.700	150	498
LMK04208	261.00	25.710	100	561
LMK04906B	261.00	25.710	100	561
LMK04816B	261.00	26.430	100	561
LMK04033B	229.00	30.030	150	498
LMK04832	261.00	34.960	50	746
LMK04000B	229.00	31.060	150	498

3. Required system specifications and parameters:

3.a. Required output details:

Name	Format	Frequency	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Additional specs
Out A	LVCMOS	24.576 MHz	1	100000	-50	Internal VCO

3.b. Input details:

One or more of the below inputs or TI oscillators may be used.

Name	Frequency	Clock count	Jitter (fs rms)	Noise floor (dBc/Hz)	Additional specs
Input A	24.576 MHz	1	4000000	-60	-

3.c. System configuration options:

Application: Not specified
Jitter integration bandwidth: 12 kHz to 20 MHz
Max. number of stages: 5
Solution scoring:
Jitter: Very important, Power: Less important, Price: Important, Area: Important

3.d. External VCO and VCXO computation parameters:

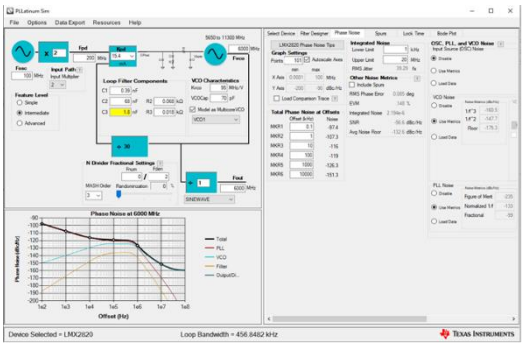
VCO attribute	Value	VCXO attribute	Value
Price ($)	30	Price ($)	20
Area (mm²)	140	Area (mm²)	180
Current (mA)	15	Current (mA)	15
Noise floor (dBc/Hz)	-156	Noise floor (dBc/Hz)	-168
Jitter (fs rms)	50	Jitter (fs rms)	50
Min frequency (MHz)	1	Frequency (MHz)	500
Max frequency (MHz)	10000	Auto pick VCXO frequency	true

Featured clocks & timing tools

Clock tree architect design tool helps you select the right clocks & timing products to design a clock tree based on user entered output, input and system specifications. Along with the clock tree structure – it provides an approximate metric for power, area, jitter and other system parameters. Users are recommended to use the below tools to help with more accurate in-depth simulations, device programming, loop filter design and configuration.

PLLatinum Simulator Tool (PLLATINUMSIM-SW)

The PLLATINUMSIM-SW simulator tool lets you create detailed designs and simulations of our PLLATINUM™ integrated circuits which include the LMX series of PLLs and synthesizers. Users can design active and passive filters, do detailed simulations of phase noise, purs, lock time and bode plots.



TICS Pro Software (TICSPRO-SW)

The TICS Pro software is used to program the evaluation modules (EVMs) for device numbers with these prefixes: CDC, LMK and LMX. These devices include PLLs and voltage-controlled oscillators (PLL+VCO), synthesizers and clocking devices. Users can program EVMs through USB2ANY interface adaptor or onboard USB interface and export the programming configurations for use in end application. Even without an EVM, TICS Pro is very useful tool in determining and validating register configurations and how to set up the device.

Clocks & timing product portfolio and additional resources

Visit Clocks & timing home page to explore the full product portfolio and additional resources to help you with your designs. Also, checkout TI Precision Labs - Clocks and timing videos to learn more about clocks and timing basics, phase lock loop fundamentals, noise, network synchronizers and design tips.

Technical support

TI E2E™ support forums

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