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LV5609LP

Bi-CMOS LSI

Vertical Clock Driver for CCD

Overview

The LV5609LP is vertical clock driver for CCD.

Functions

- Ternary output ×2ch
- Binary output ×2ch
- SHT output ×1ch
- Output ON resistance : 30Ω typ

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = V_M = 0\text{V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		6	V
	VH max		20	V
	VL max		-10	V
	VH-VL max		24	V
Allowable power dissipation	P_d max	with specified substrate *	0.8	W
Operating temperature	T_{opr}		-20 to +80	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

* : Specified substrate : 40×50×0.8mm³, glass epoxy four-layer (2S2P) board

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = V_M = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.0	3.3	5.5	V
	VH			15	17	V
	VL		-8.5	-7.5	-4	V
	VH-VL				23.5	V
CMOS input High voltage	V_{INH}		$0.8V_{DD}$		V_{DD}	V
CMOS input Low voltage	V_{INL}		-0.1		0.4	V

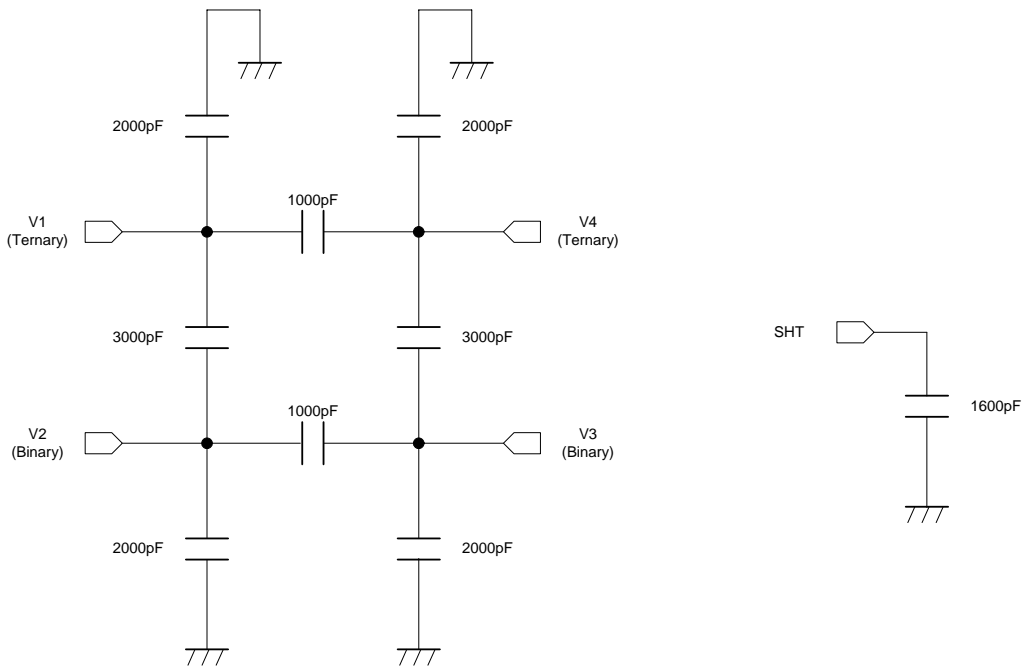
LV5609LP

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, $V_{SS} = 0\text{V}$, $V_H = 15\text{V}$, $V_L = -7.5\text{V}$, $V_M = 0\text{V}$,
Unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Static current drain	I_{DD}	V_{DD} pin			1	μA
	I_H	V_H pin			10	μA
	I_L	V_L pin			1	μA
Dynamic current drain	I_{DD}	V_{DD} pin See *1 and *2.			1	mA
	I_H	V_H pin See *1 and *2.		2.4	4.5	mA
	I_L	V_L pin See *1 and *2.		3	5	mA
Output ON resistance	R_L	$I_O = +10\text{mA}$		20	30	Ω
	R_M	$I_O = \pm 10\text{mA}$		30	45	Ω
	R_H	$I_O = -10\text{mA}$		30	40	Ω
	R_{SHT}	$I_O = -10\text{mA}$		30	40	Ω
Propagation delay time	TPLM	No load			200	ns
	TPMH	No load			200	ns
	TPLH	No load			200	ns
	TPML	No load			200	ns
	TPHM	No load			200	ns
	TPHL	No load			200	ns
Rise time	TTLM	$V_L \rightarrow V_M$ V1, V3 See *1.			800	ns
		$V_L \rightarrow V_M$ V2, V4 See *1.			800	ns
	TTMH	$V_M \rightarrow V_L$ V1, V3 See *1.			800	ns
	TTLH	$V_L \rightarrow V_H$ SHT See *1.			200	ns
Fall time	TTML	$V_M \rightarrow V_L$ V1, V3 See *1.			800	ns
		$V_M \rightarrow V_L$ V2, V4 See *1.			800	ns
	TTHM	$V_H \rightarrow V_M$ V1, V3 See *1.			800	ns
	TTHL	$V_H \rightarrow V_L$ SHT See *1.			200	ns

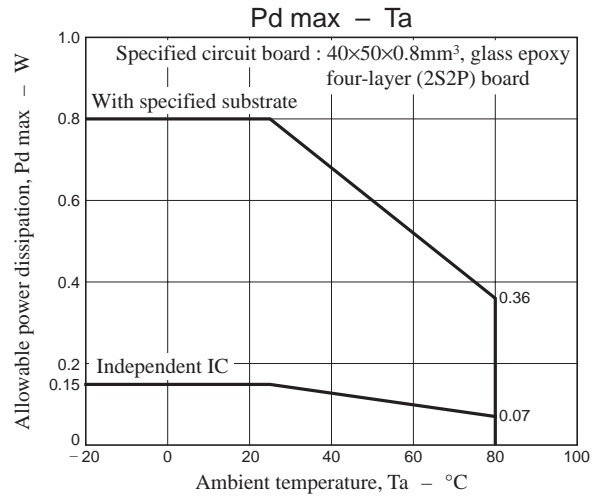
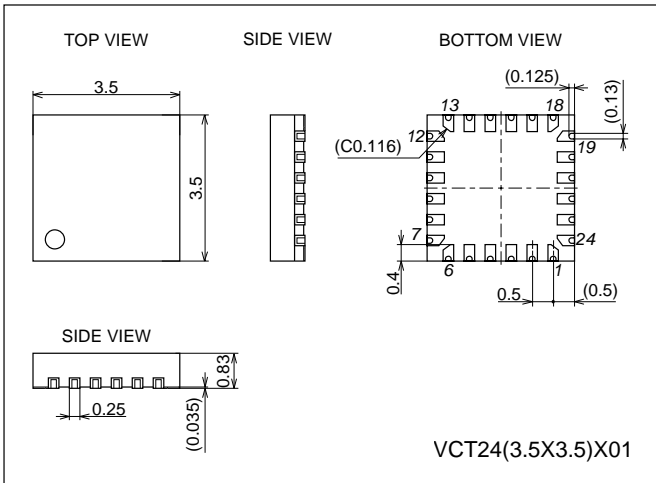
*1 : Refer to the CCD equivalent load shown below.

*2 : Refer to the timing waveform on Page 7.



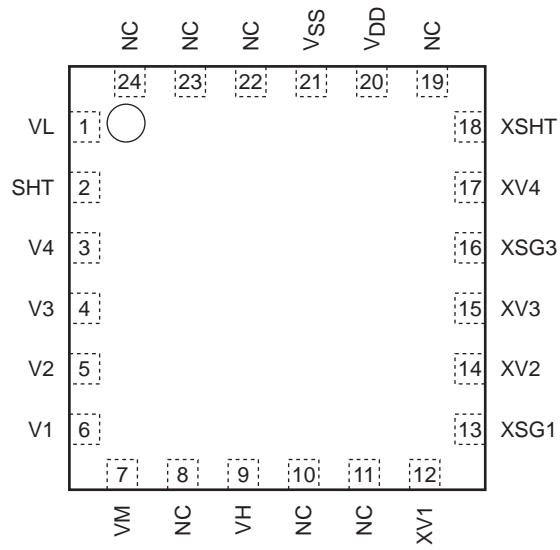
Package Dimensions

unit : mm (typ)
3322



LV5609LP

Pin Assignment



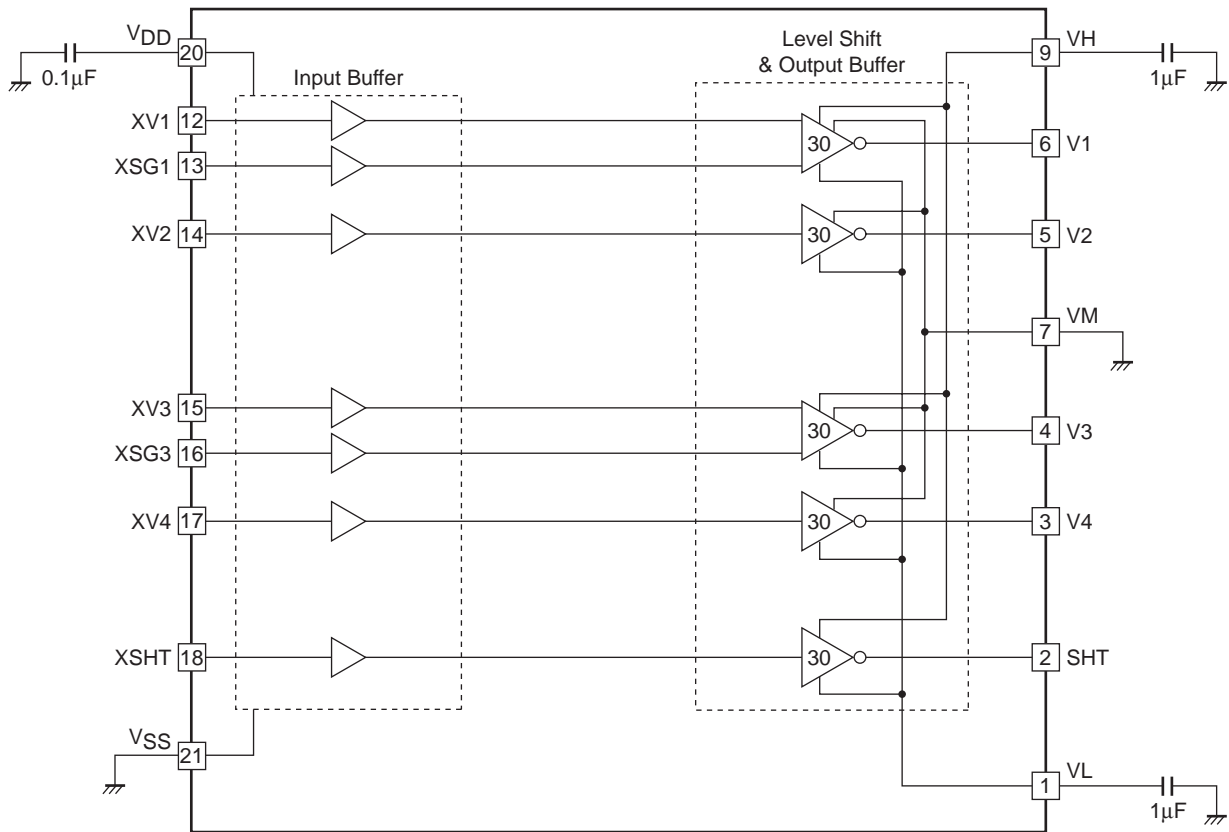
Top view

Pin Function

Pin No.	Name	Mode
1	VL	Lo power for output (-7.5V system)
2	SHT	Level shift output (binary VH, VL)
3	V4	Level shift output (binary VM, VL)
4	V3	Level shift output (ternary VH, VM, VL)
5	V2	Level shift output (binary VM, VL)
6	V1	Level shift output (ternary VH, VM, VL)
7	VM	GND for output
8	NC	
9	VH	Hi power supply for output (15V system)
10	NC	
11	NC	
12	XV1	V1 transfer pulse input
13	XSG1	V1 read pulse input
14	XV2	V2 transfer pulse input
15	XV3	V3 transfer pulse input
16	XSG3	V3 read pulse input
17	XV4	V4 transfer pulse input
18	XSHT	SHT pulse input
19	NC	
20	V _{DD}	Power supply for input buffer (3.3V system)
21	V _{SS}	GND for input buffer
22	NC	
23	NC	
24	NC	

LV5609LP

Block Diagram

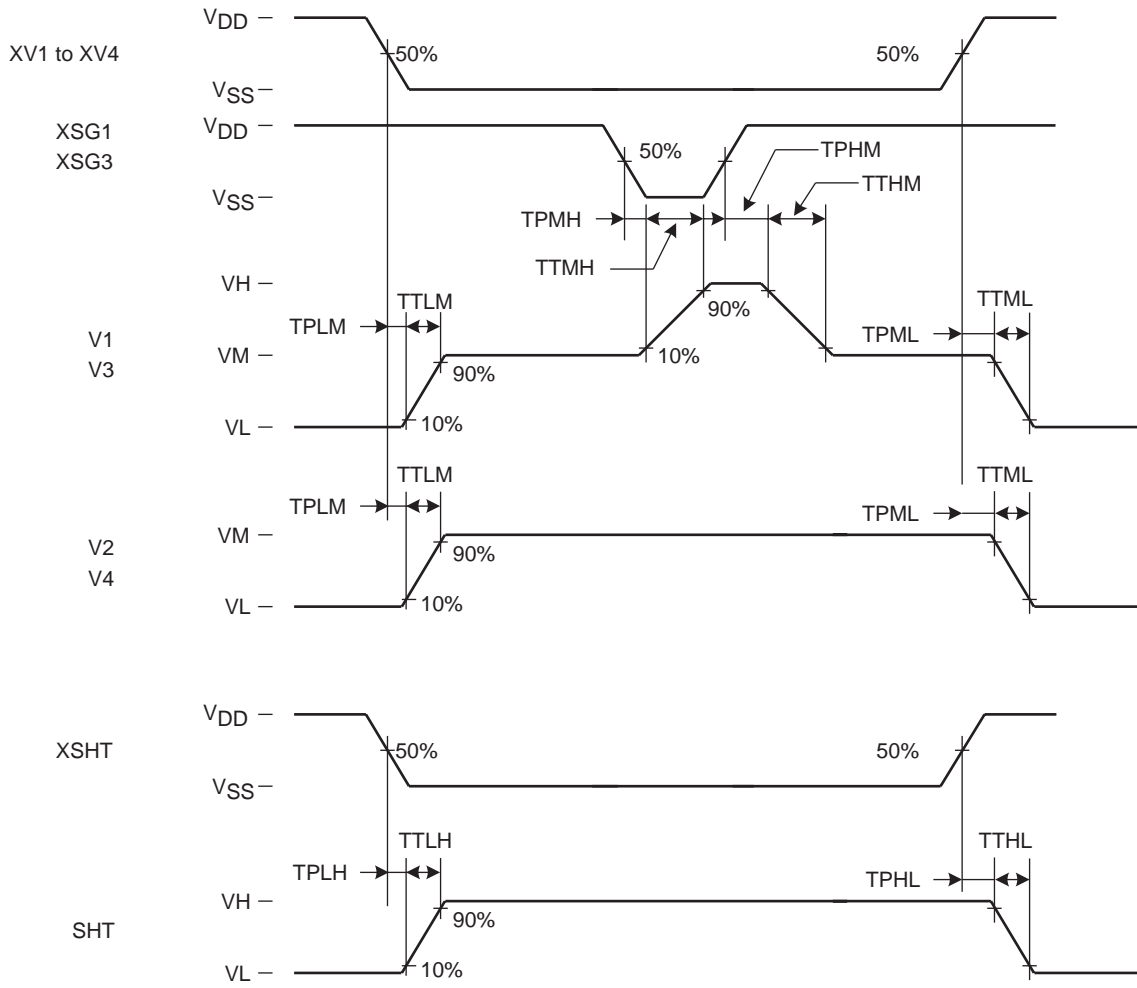


Logical Function Table

Input				Output		
XV1 XV3	XSG1 XSG3	XV2 XV4	XSHT	V1 V3	V2 V4	SHT
L	L	X	X	VH	X	X
L	H	X	X	VM	X	X
H	L	X	X	VL	X	X
H	H	X	X	VL	X	X
X	X	L	X	X	VM	X
X	X	H	X	X	VL	X
X	X	X	L	X	X	VH
X	X	X	H	X	X	VL

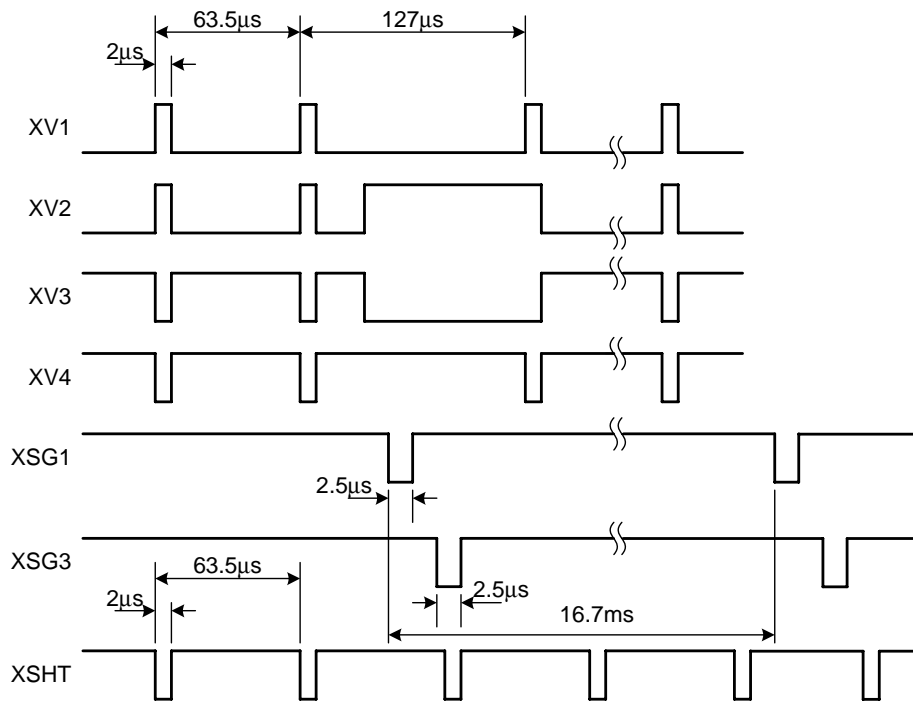
LV5609LP

Timing Chart

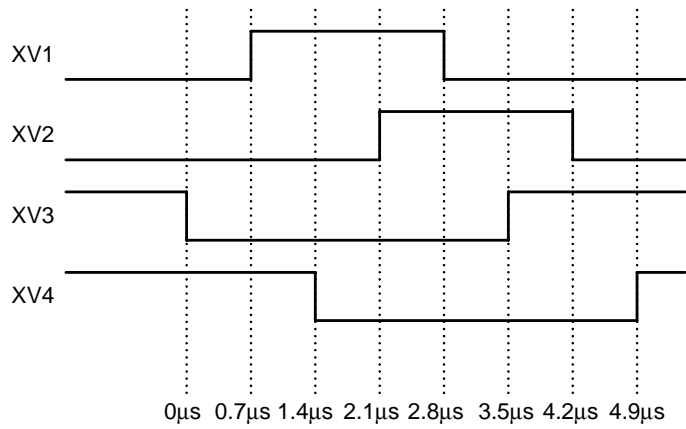


LV5609LP

CCD Equivalent Load Measurement Timing Waveform



Enlarged View of overlapped portion



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