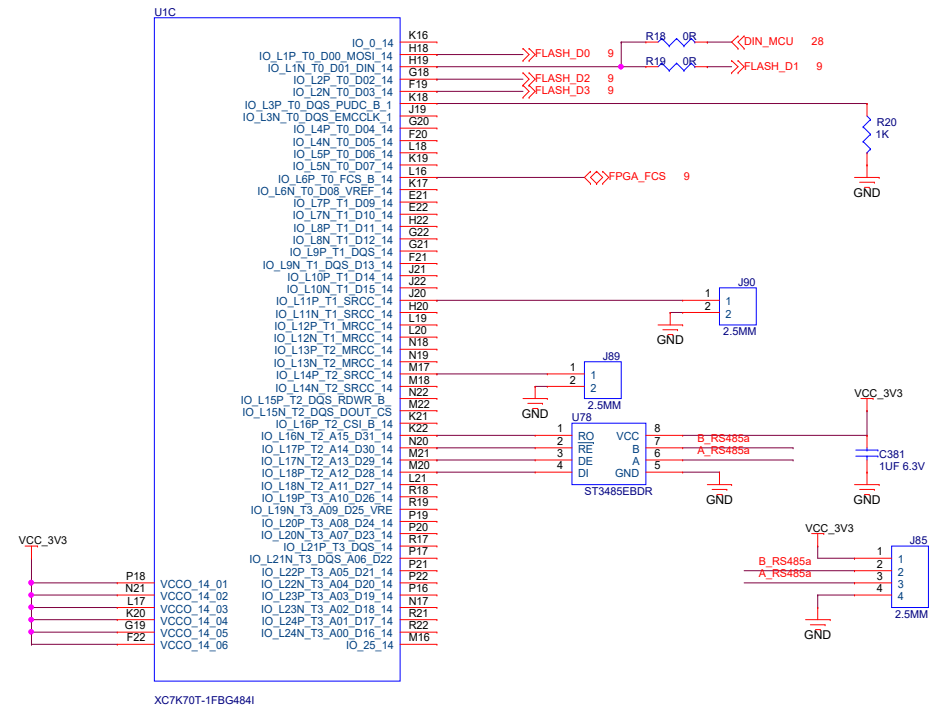
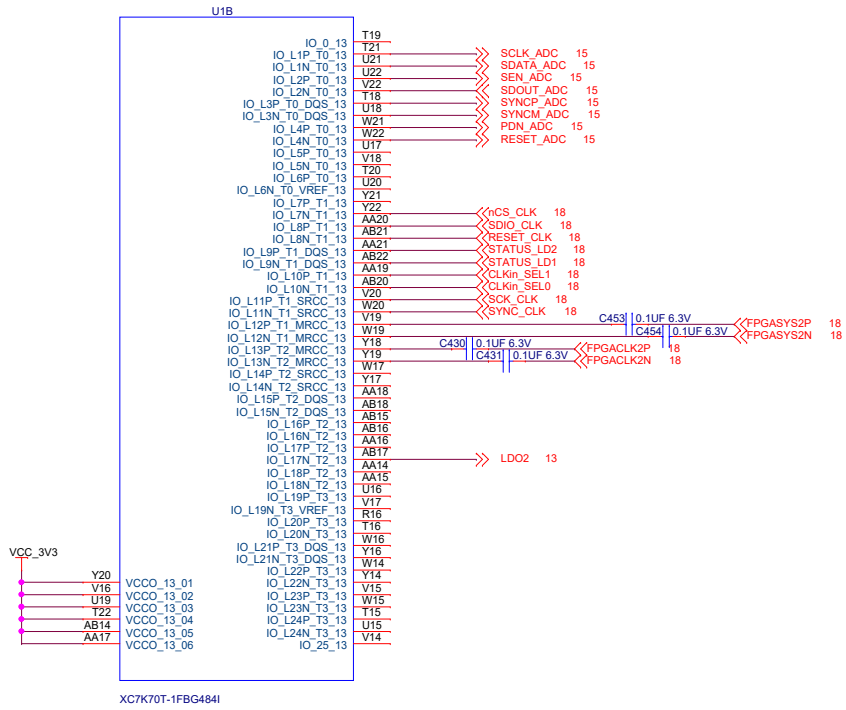
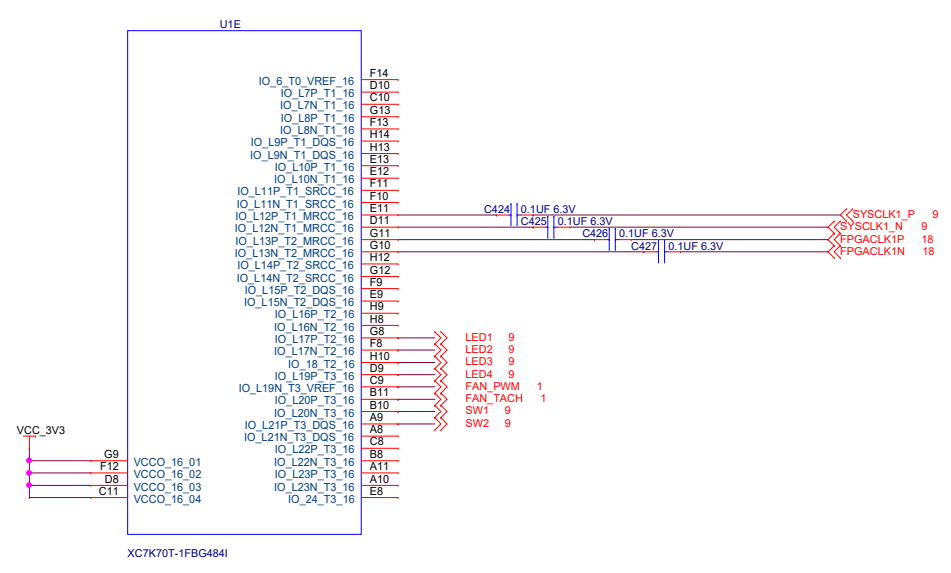
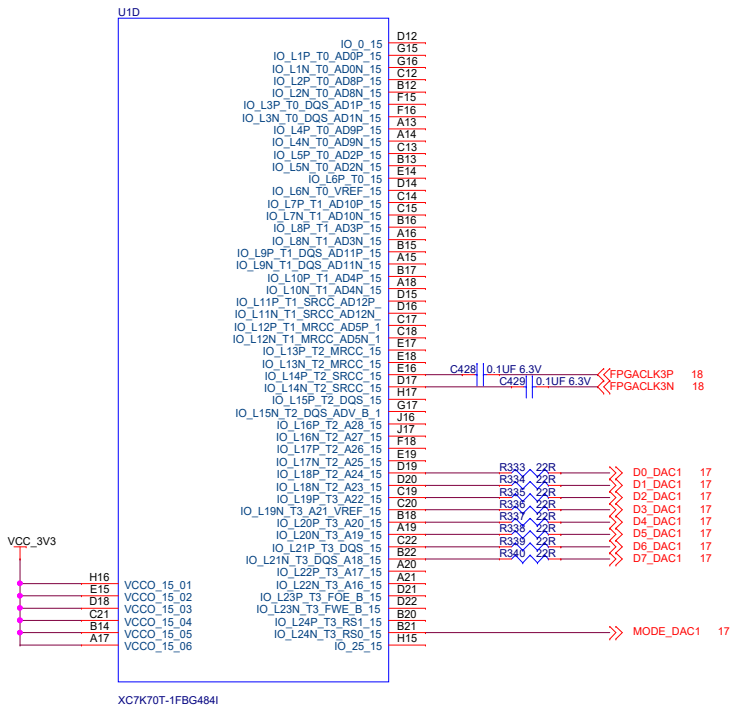


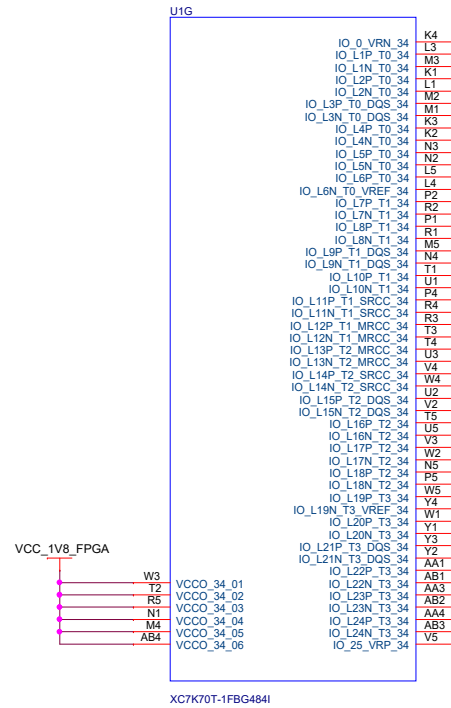
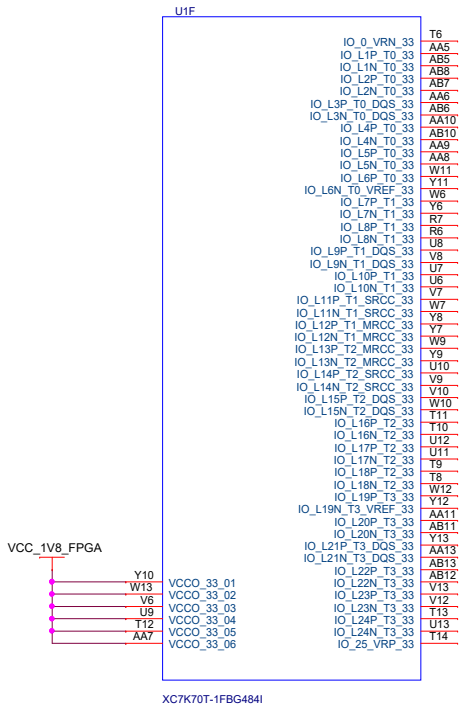
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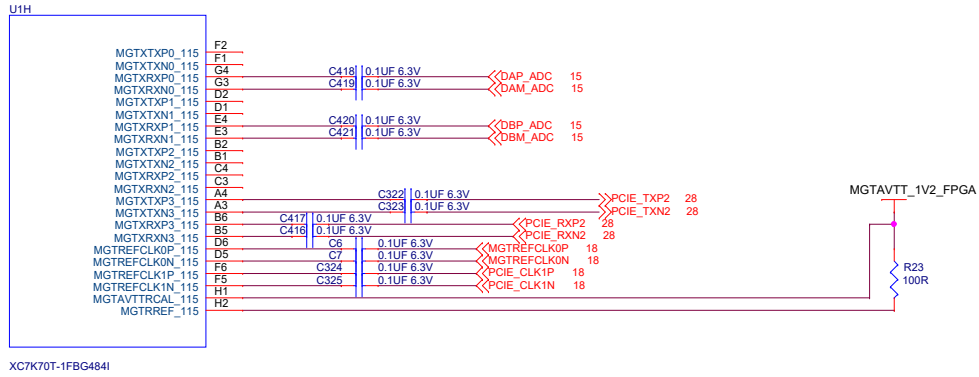
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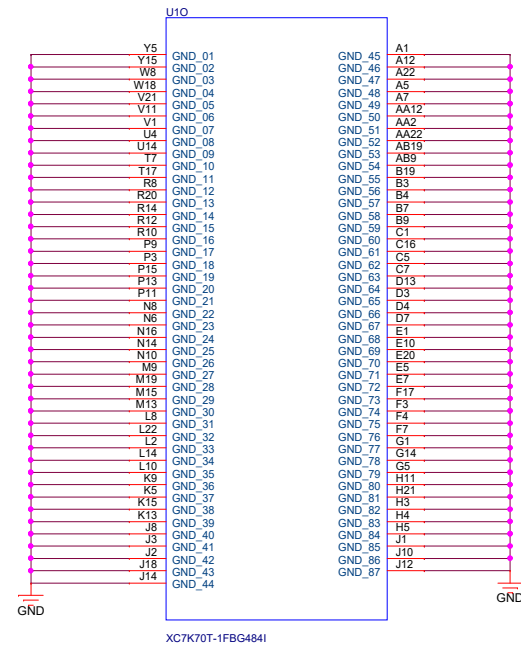
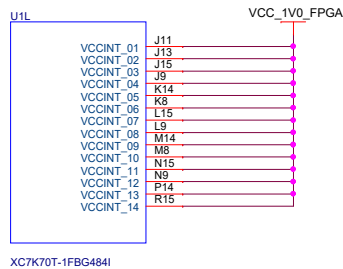
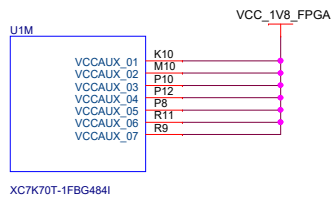
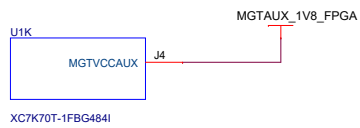
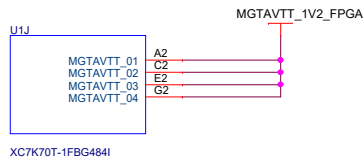
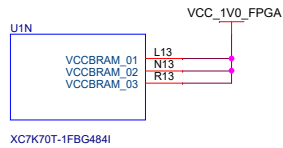
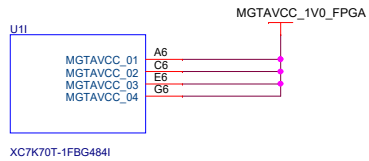
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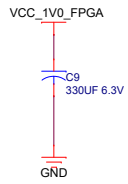
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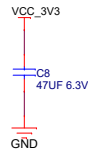
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BYPASS CAPACITORS

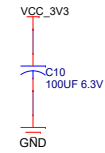
VCCINT 330uF (2)



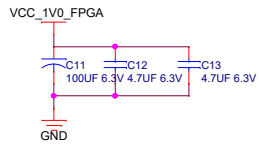
Bank 0 1.5V VCCO



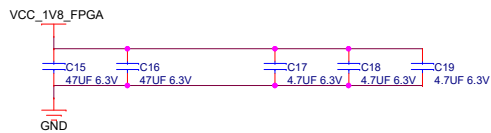
Bank 13/14/15 1.5V VCCO



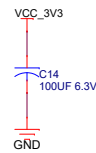
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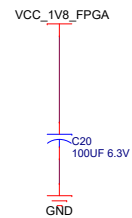
VCCAUX 47uF



Banks 16 3.3V VCCO



Banks 33, 34 1.5V VCCO

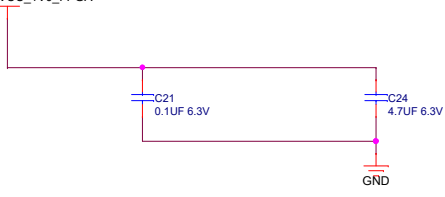


FPGA Bypass Capacitors

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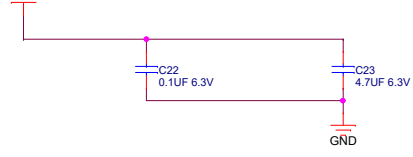
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MGTAVCC_1V0_FPGA



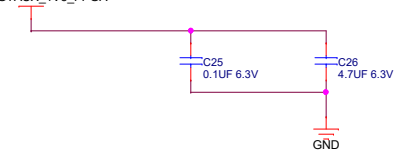
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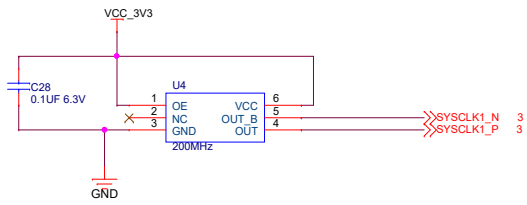
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MGTAUX_1V8_FPGA

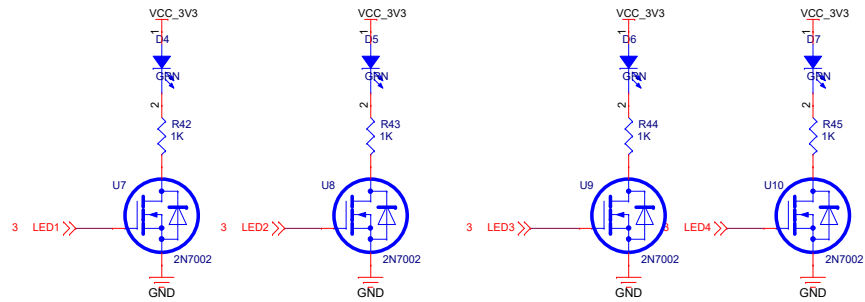
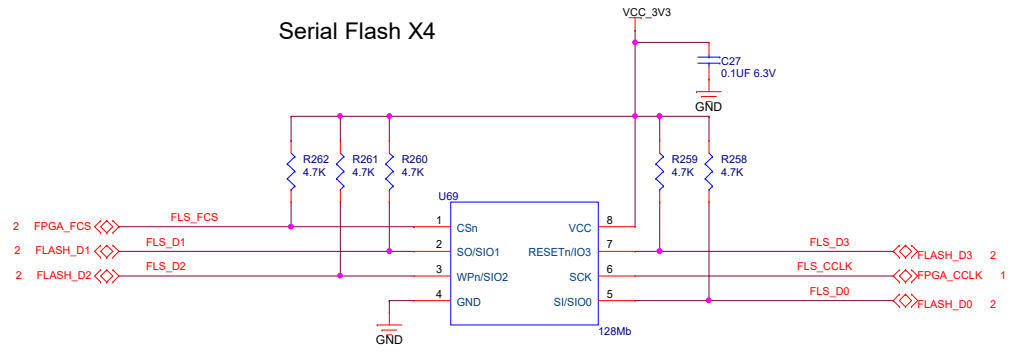


FPGA MGT Bypass Capacitors

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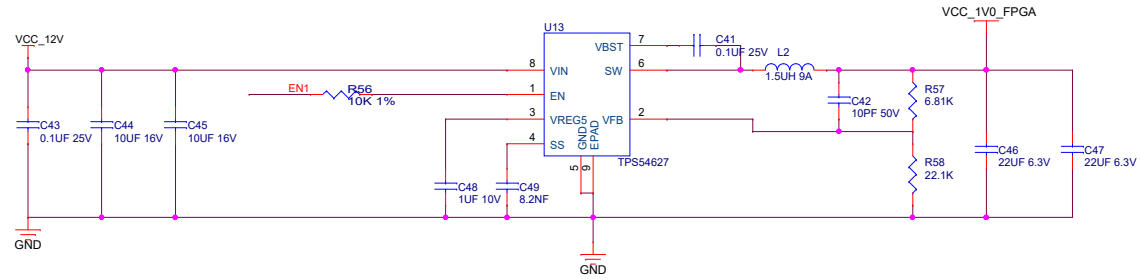
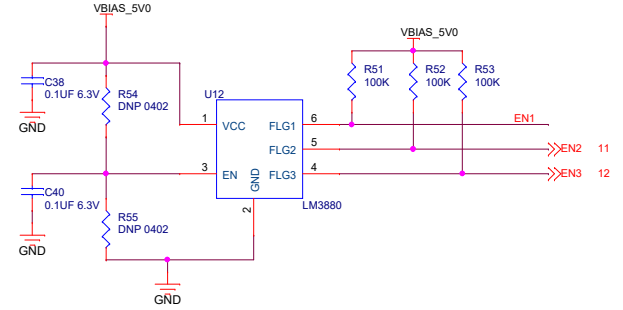
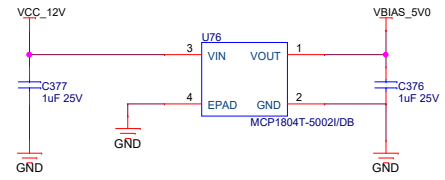
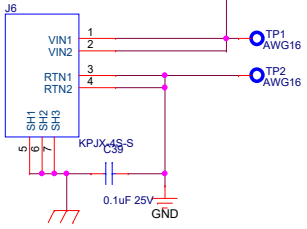
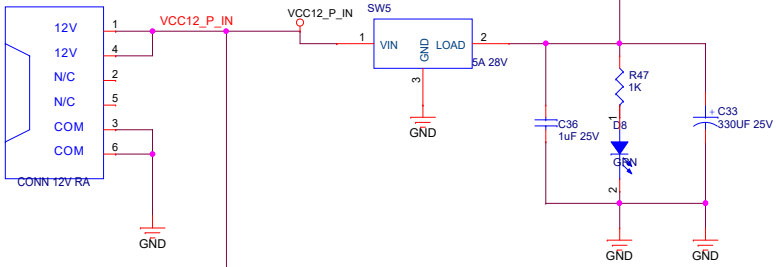
Serial Flash X4



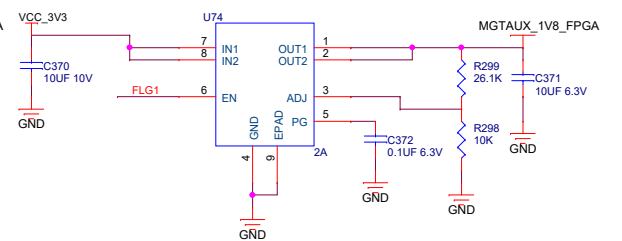
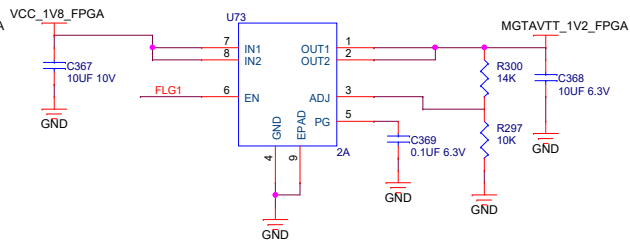
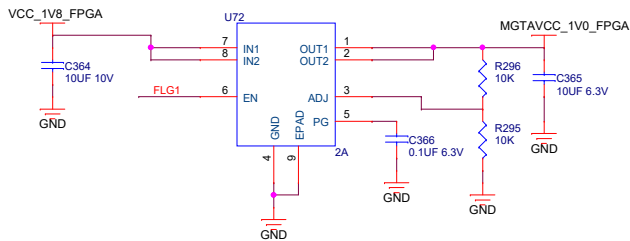
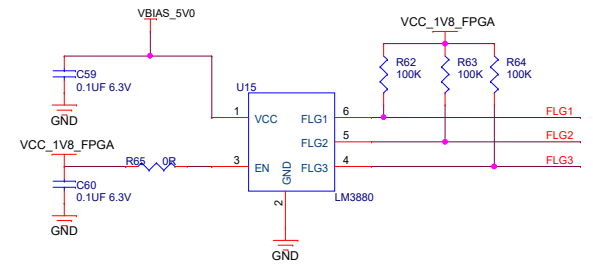
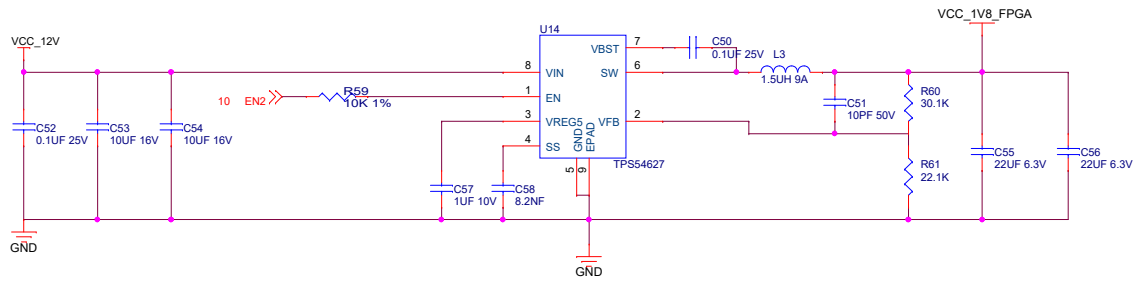
FPGA JTAG, Clock, Flash, Buttons

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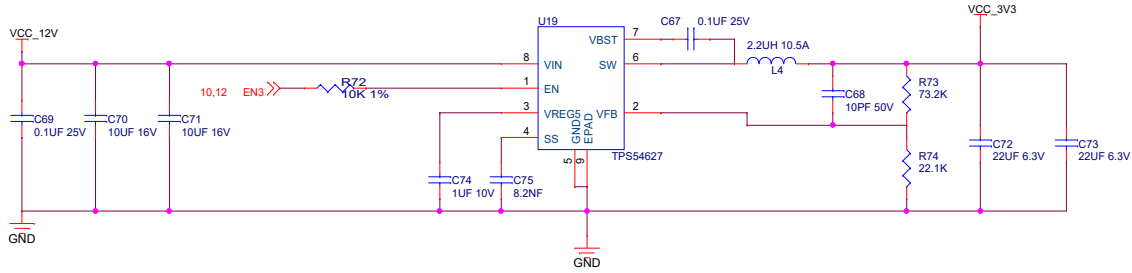
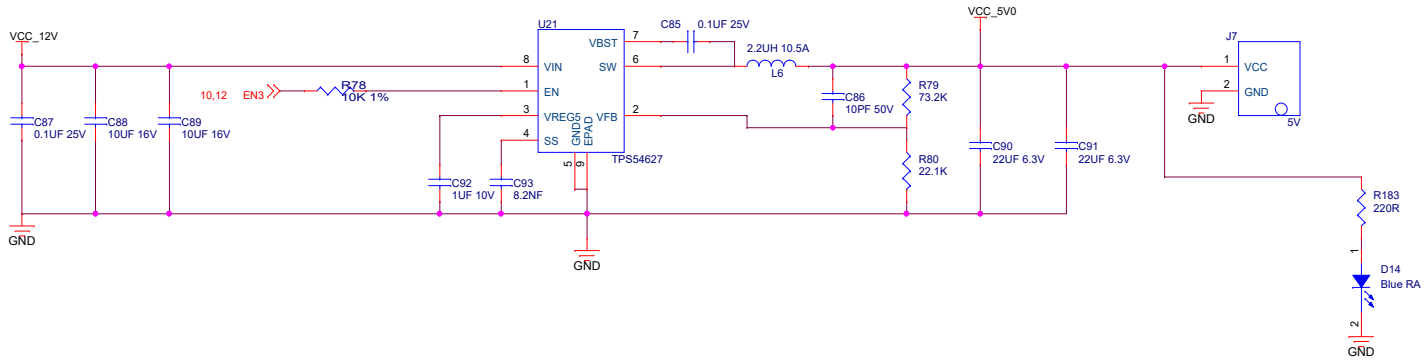
J5



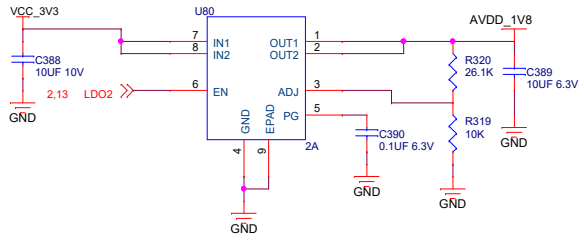
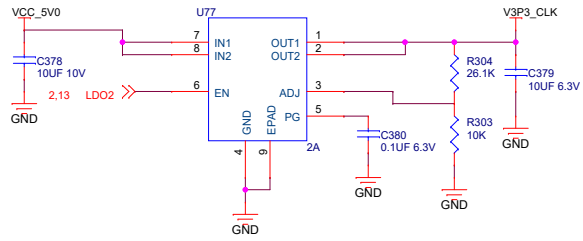
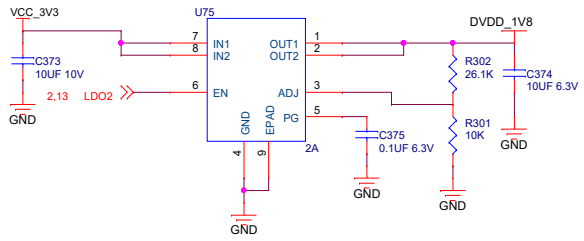
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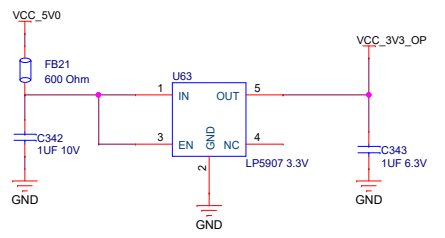
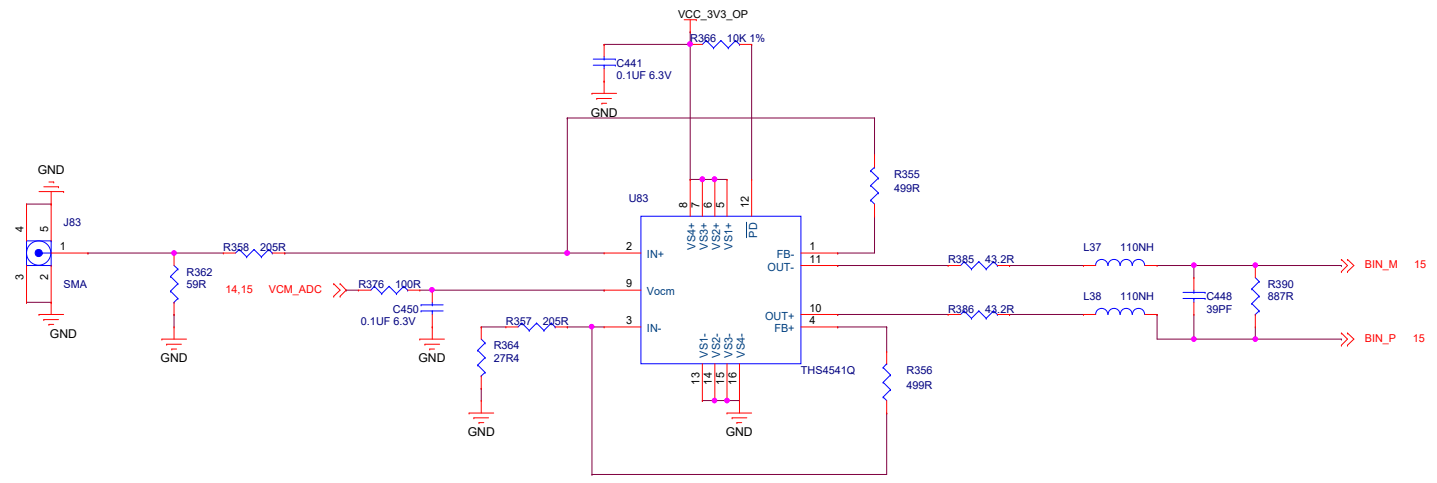
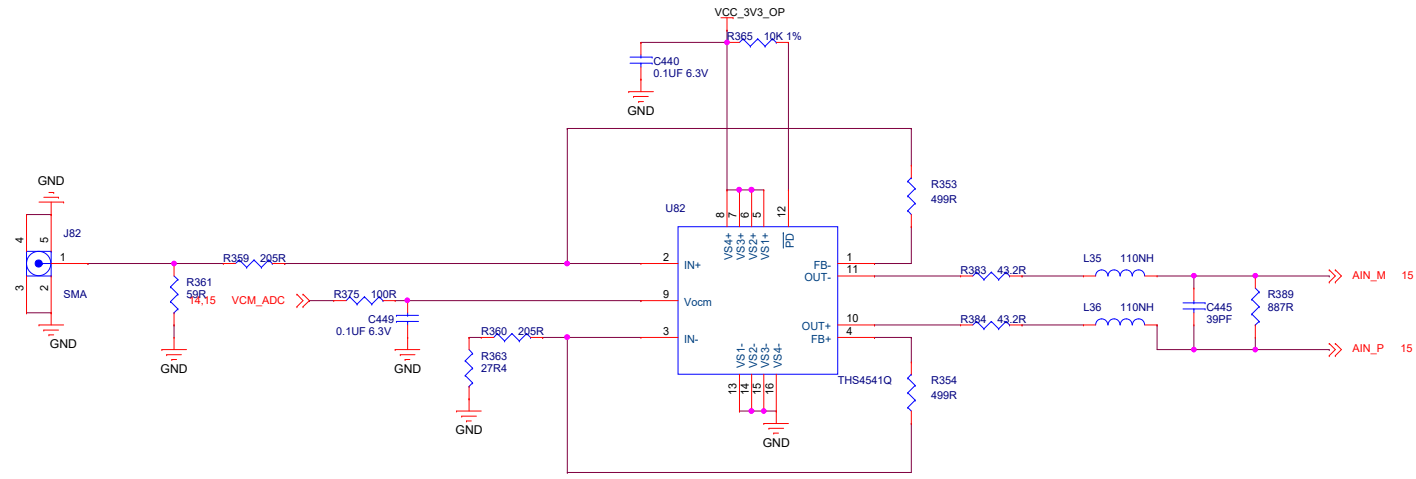
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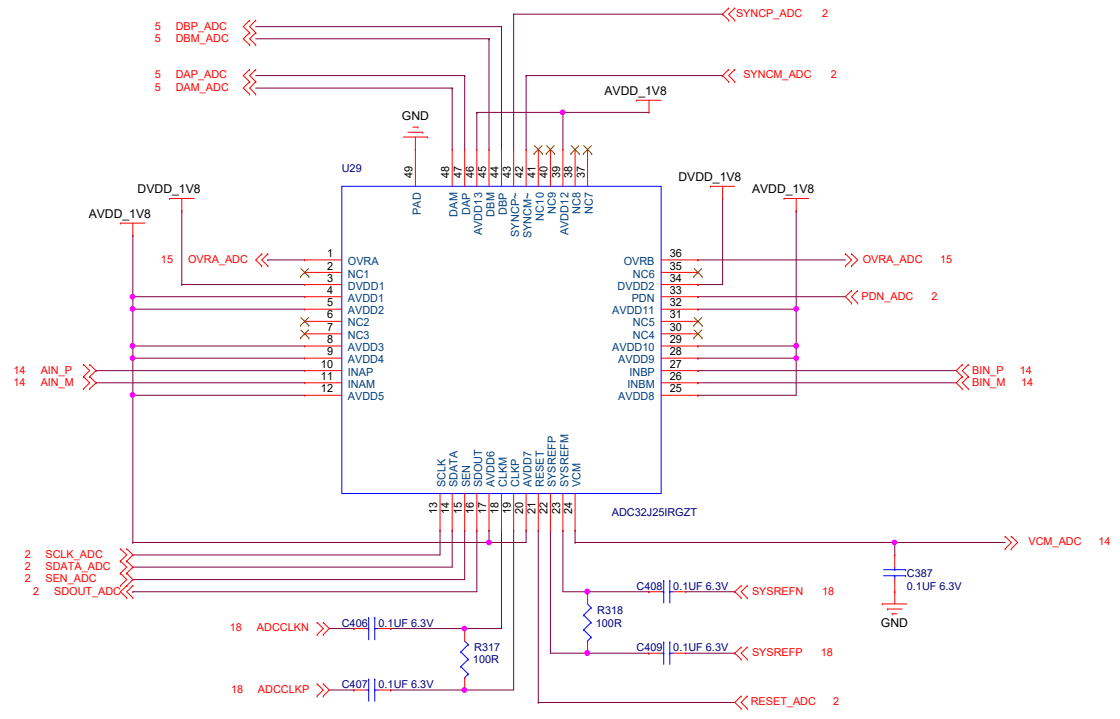
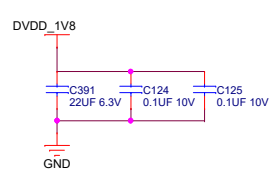
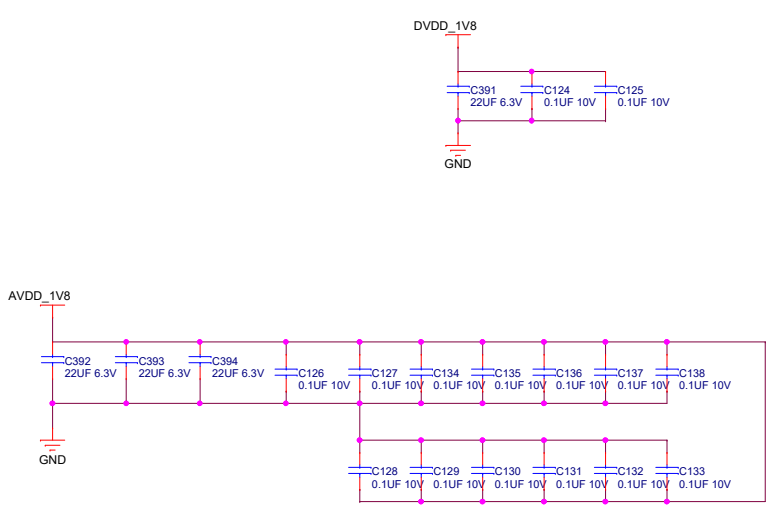
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5

4

3

2

1

D

D

C

C

B

B

A

A

5

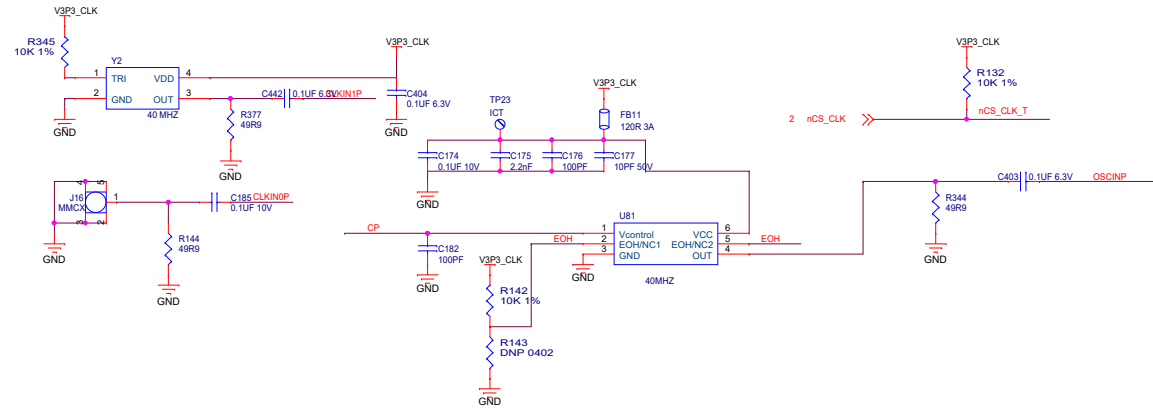
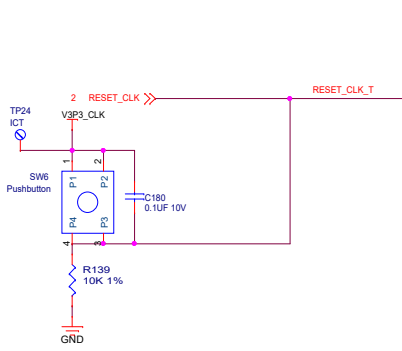
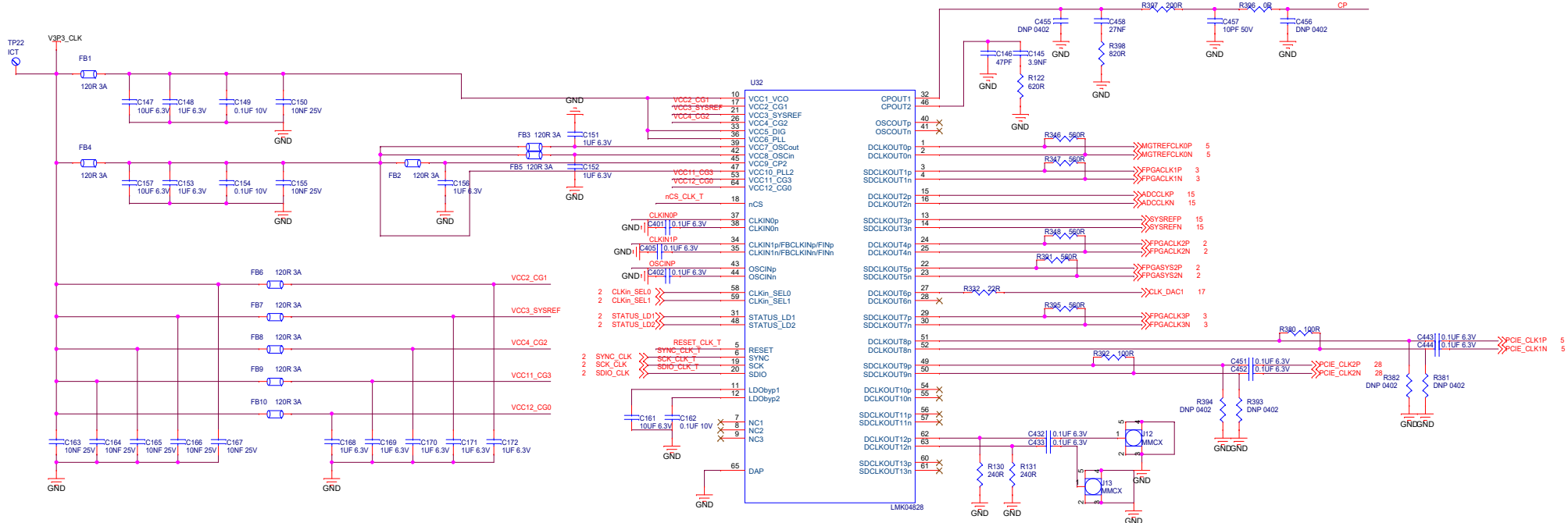
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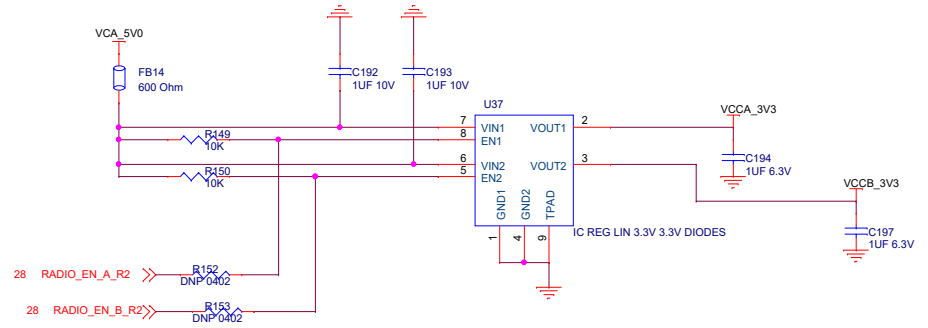
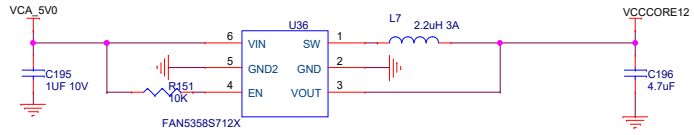
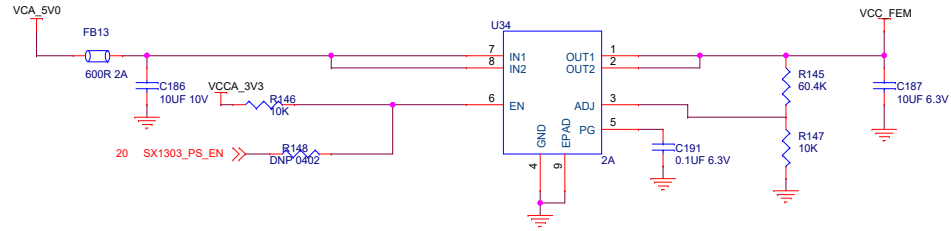
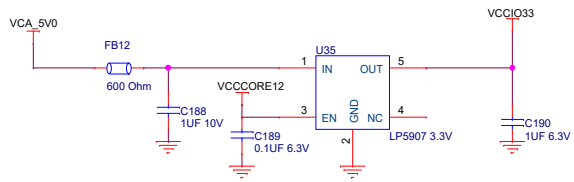
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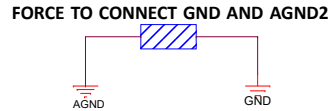
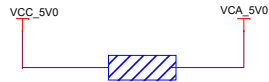
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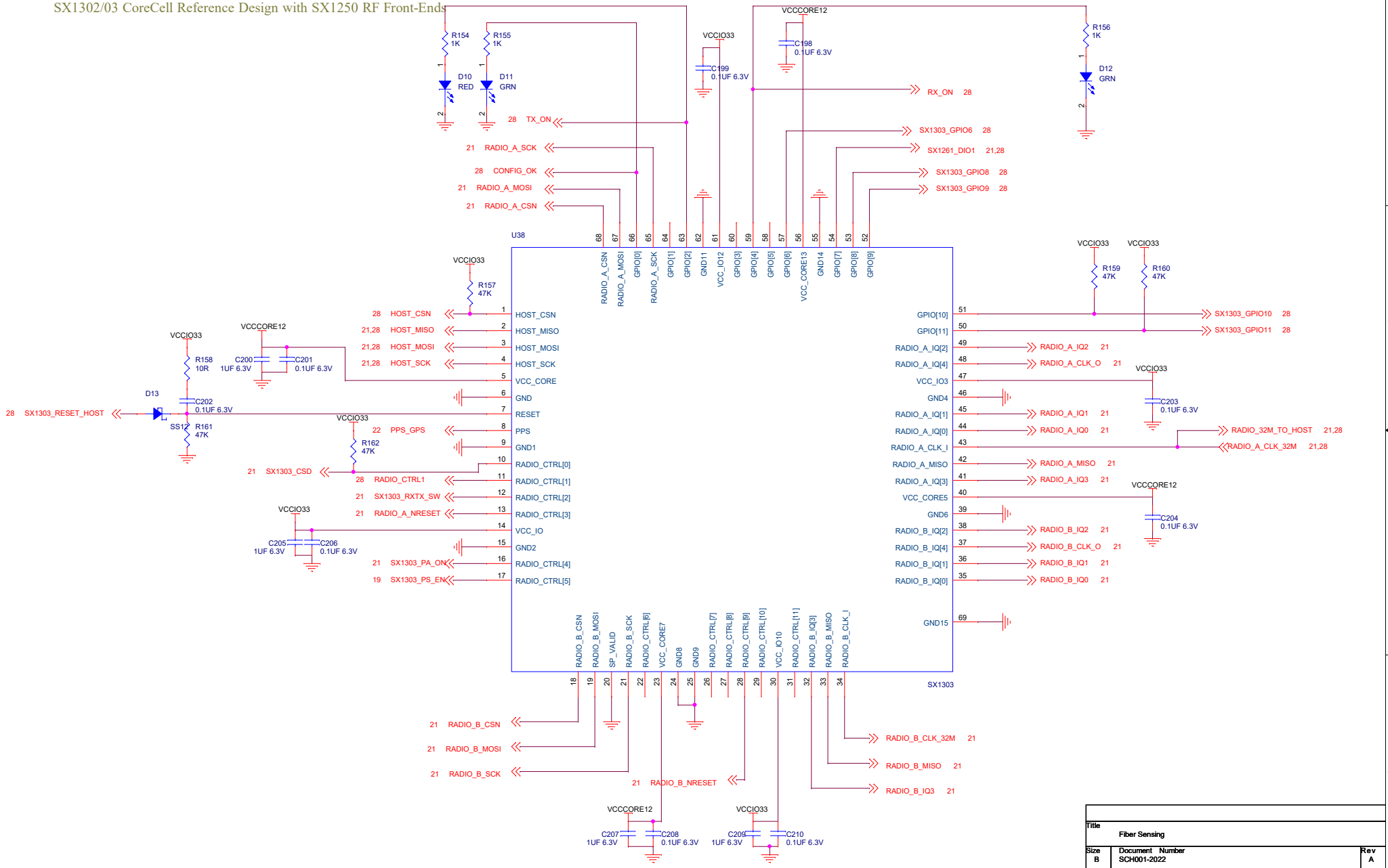


**HOW TO CONNECT gnd TO AGND2?
VIA STICING?
CONNECT POWER PLANE?**



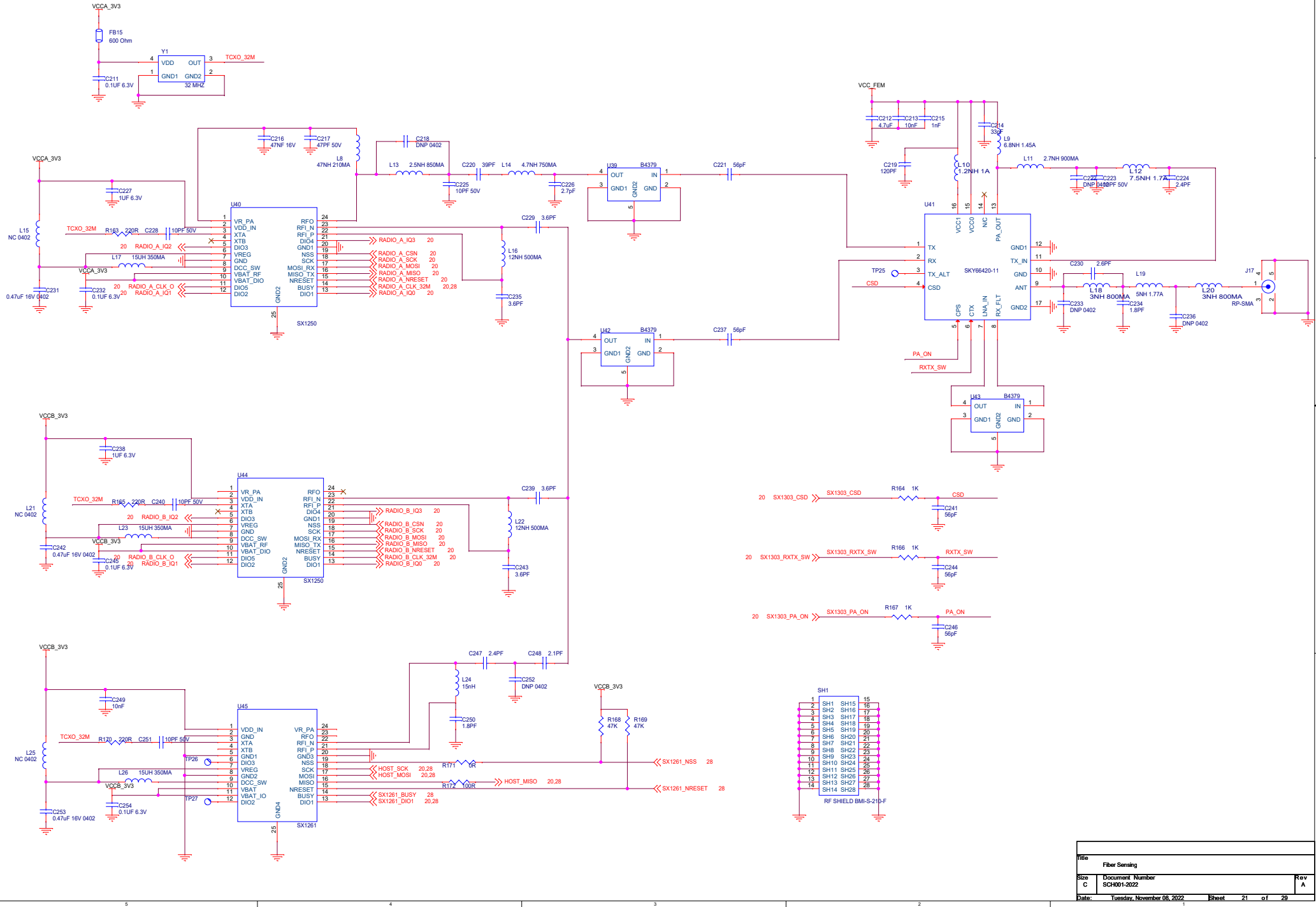
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SX1302/03 CoreCell Reference Design with SX1250 RF Front-Ends

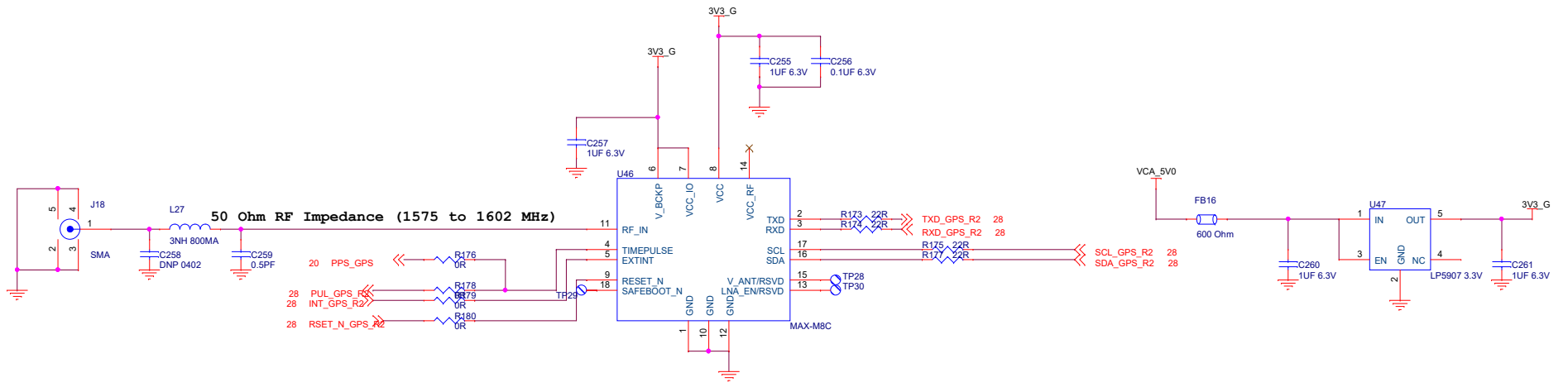


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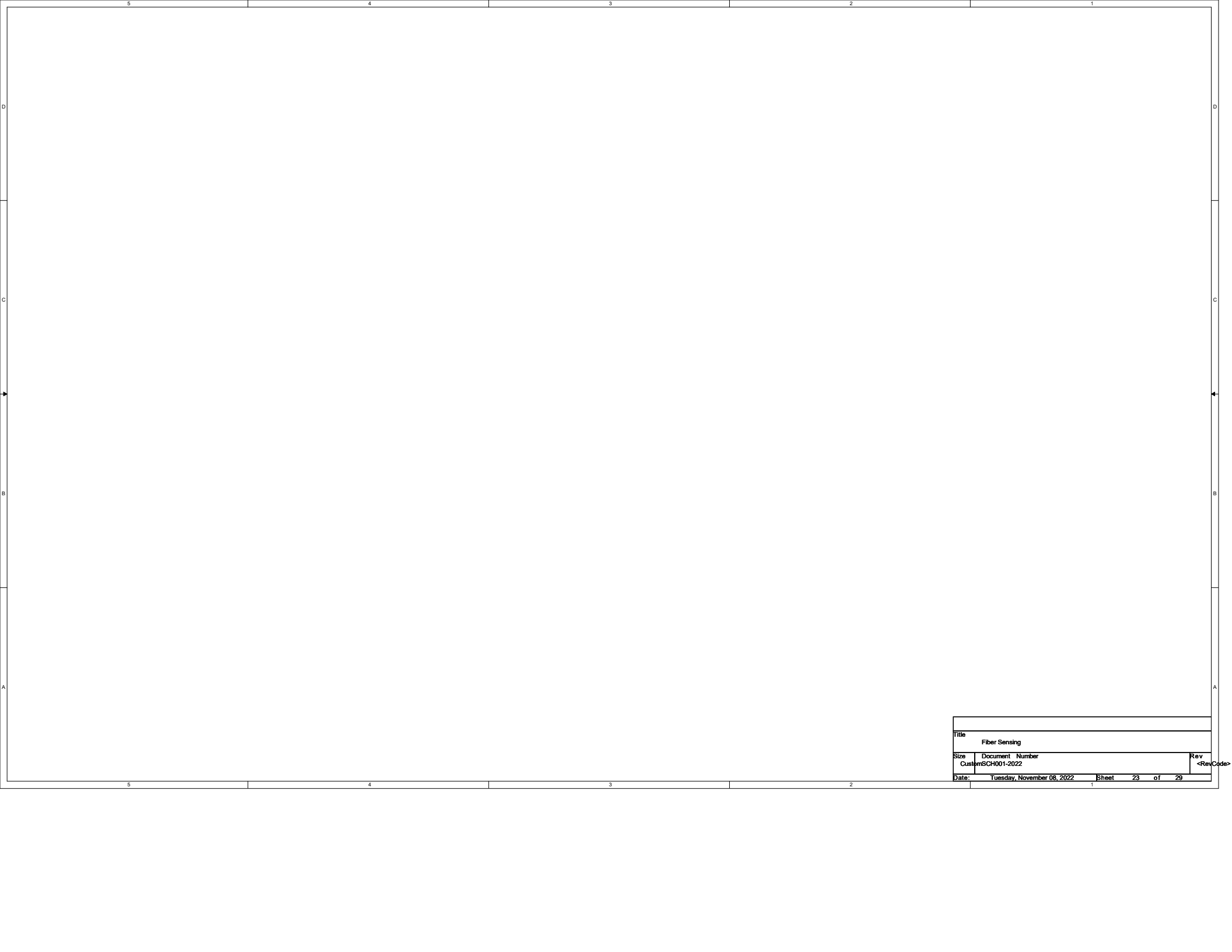
SX130x CoreCell Reference Design - RF Part with 2x SX1250 RF Front-Ends:



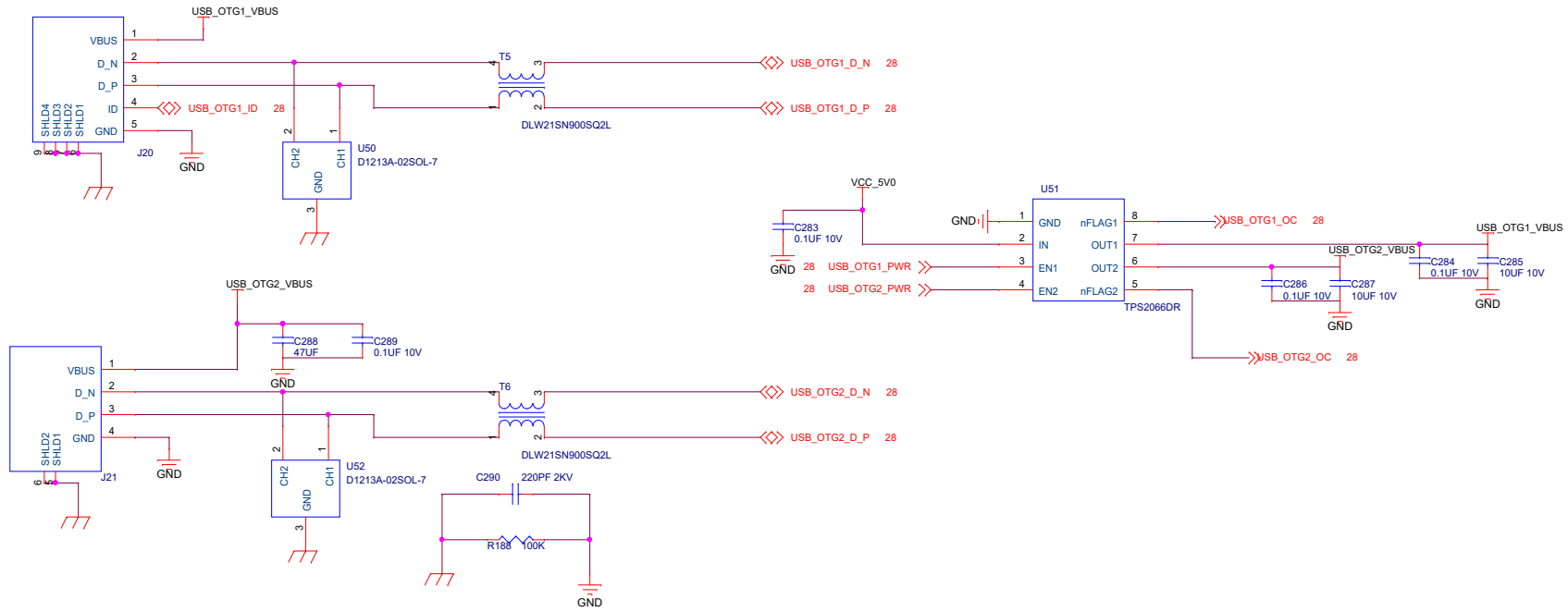
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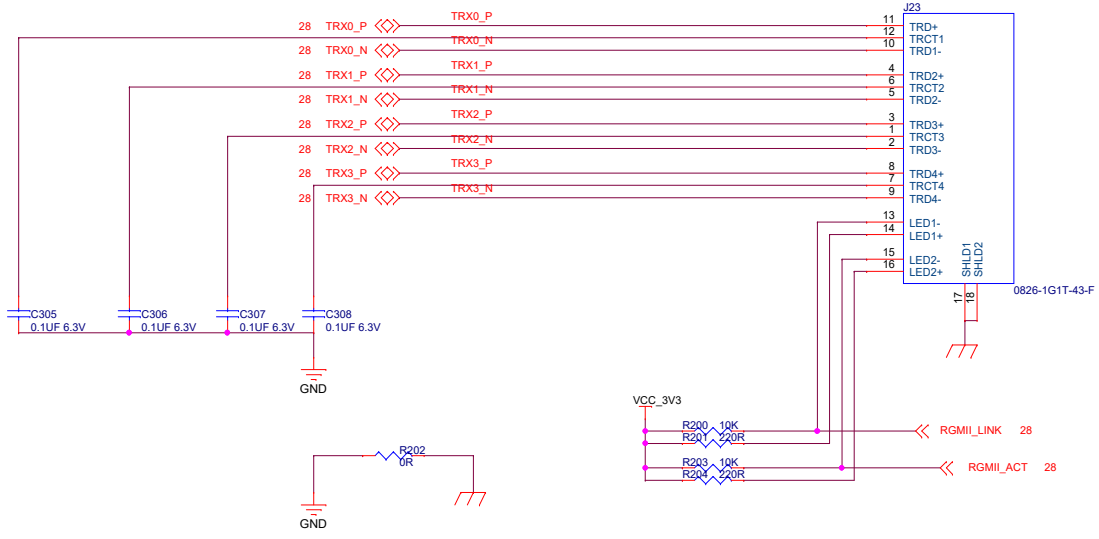
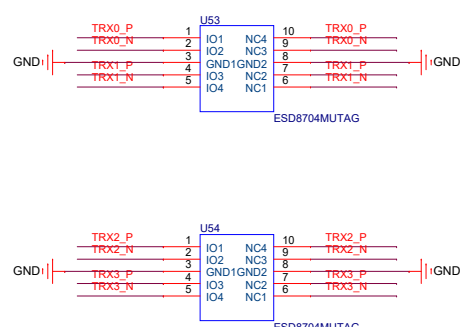
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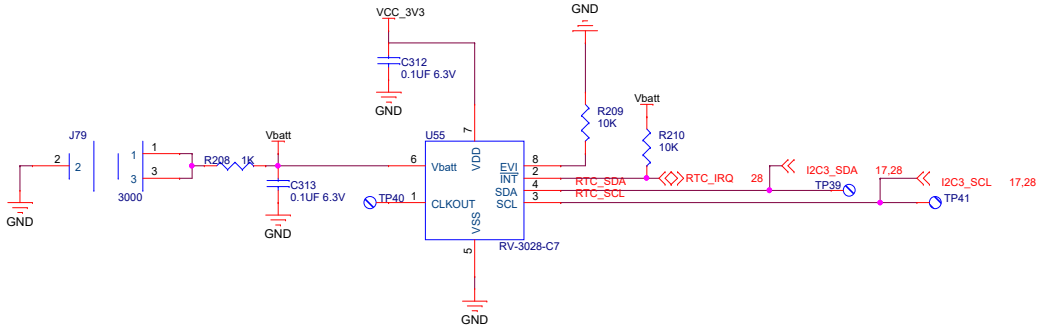
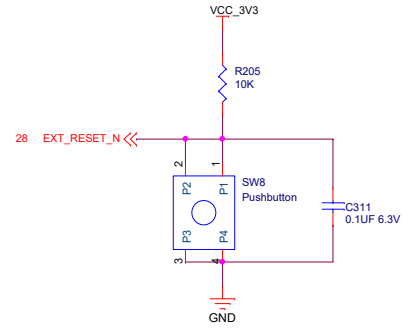
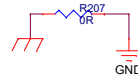
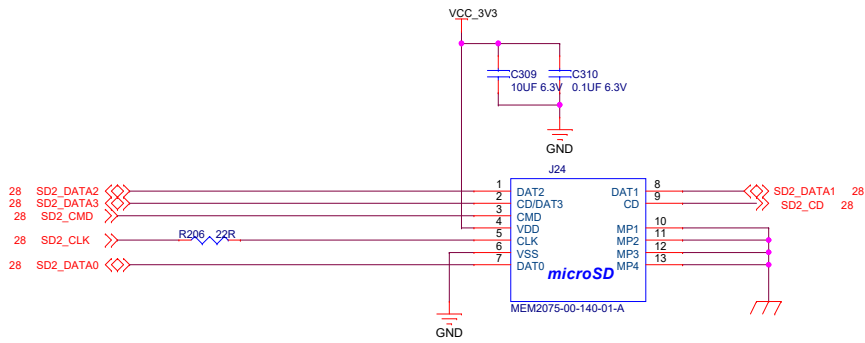
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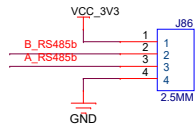
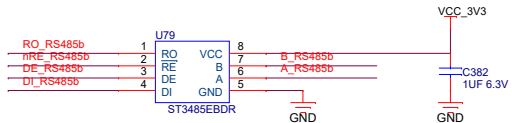
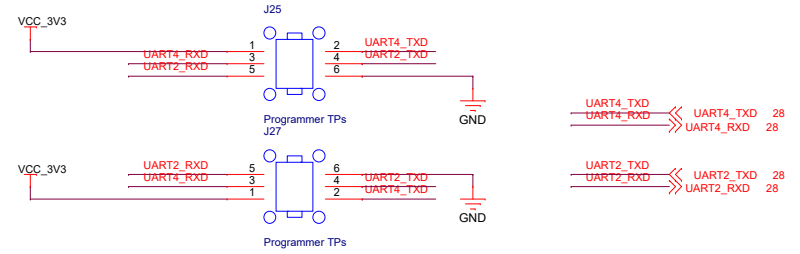
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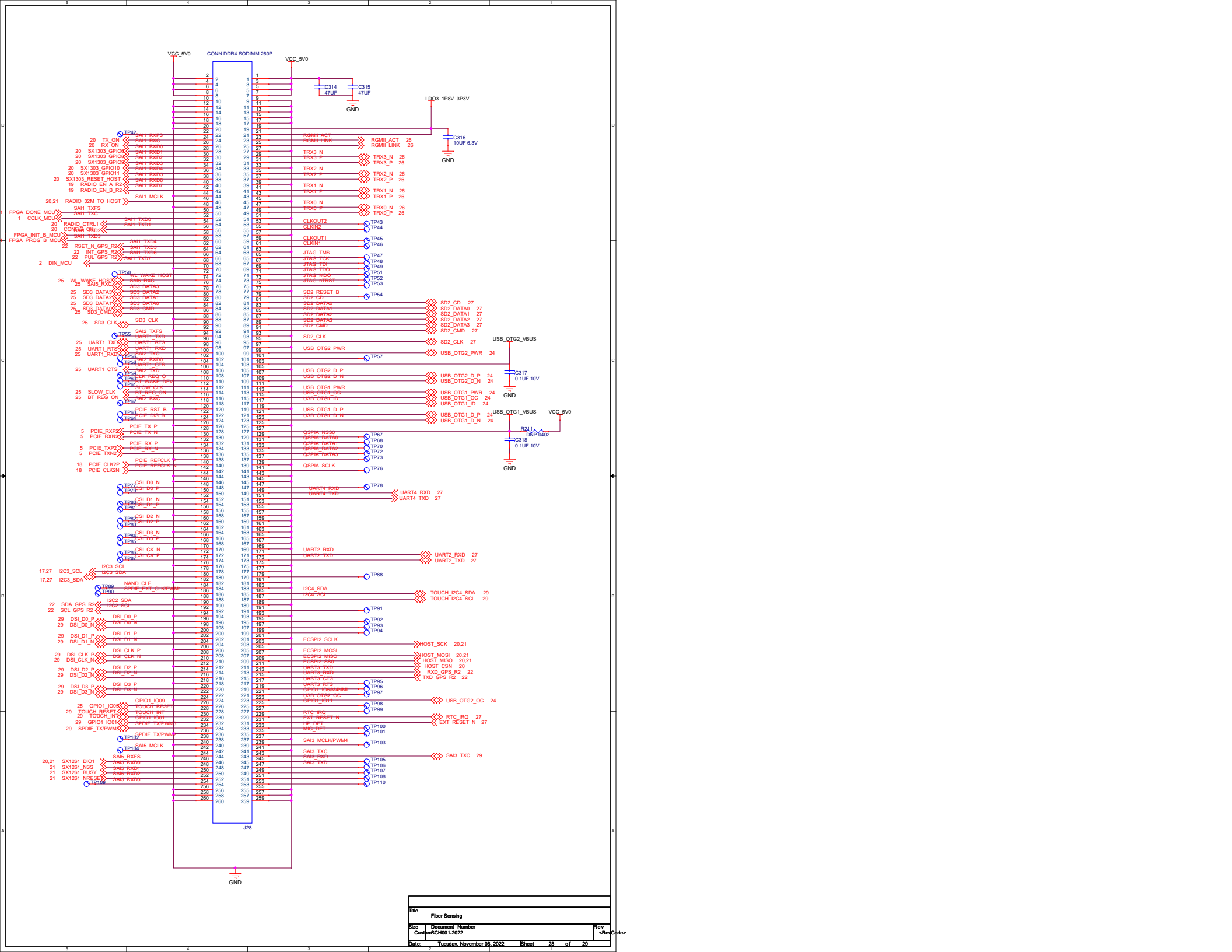
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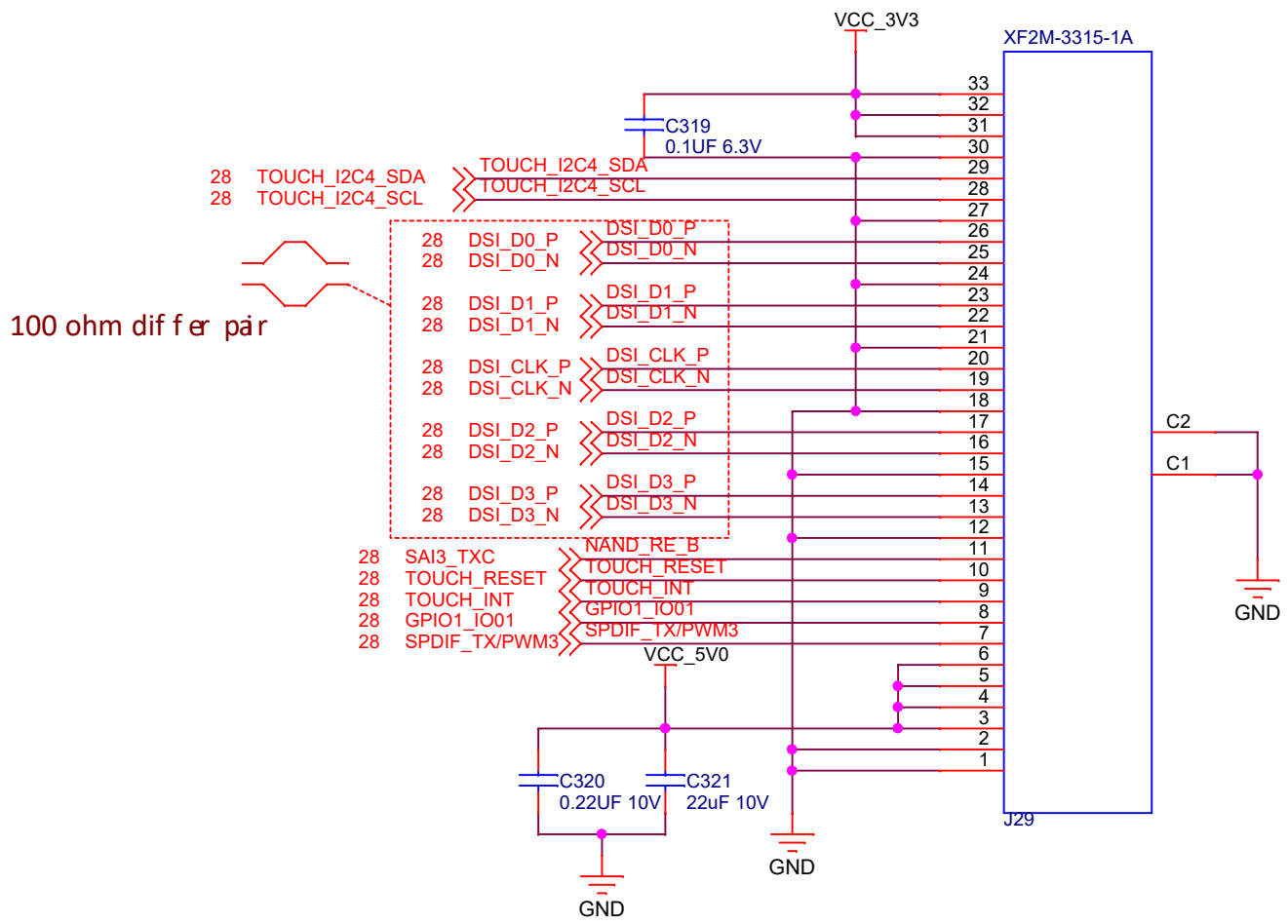


J5 is a flip of J4



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