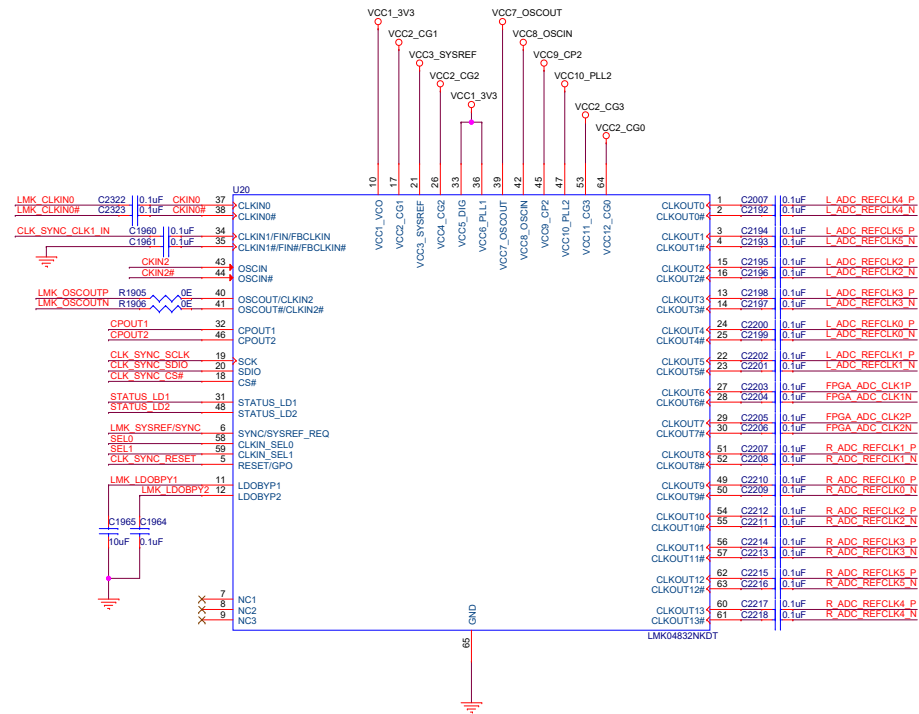
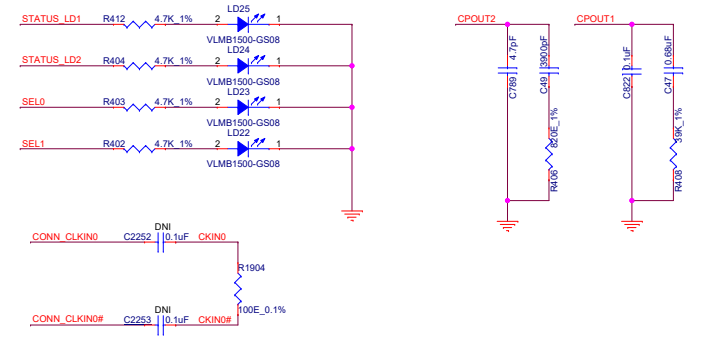


LMK04832 - ADC CLOCK GENERATION

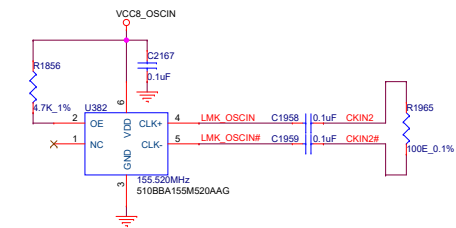


STATUS LEDS & LOOP FILTER



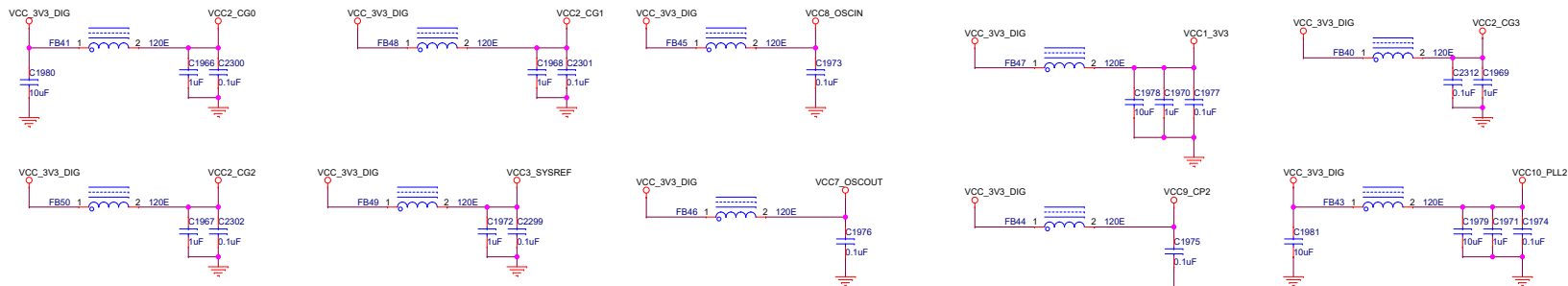
Cad Note: Tripad C2322 & C2252, Tripad C2323 & C2253

OFF PAGE CONNECTIONS



- | | | |
|------------------|--------------------|------|
| L ADC REFCLK0_N | << ADC_REFCLK0_N | [20] |
| L ADC_REFCLK0_P | << ADC_REFCLK0_P | [20] |
| L ADC REFCLK1_N | << ADC_REFCLK1_P | [20] |
| L ADC_REFCLK1_P | << ADC_REFCLK1_N | [20] |
| L ADC REFCLK2_P | << ADC_REFCLK2_P | [20] |
| L ADC_REFCLK2_N | << ADC_REFCLK2_N | [20] |
| L ADC REFCLK3_P | << ADC_REFCLK3_P | [20] |
| L ADC_REFCLK3_N | << ADC_REFCLK3_N | [20] |
| L ADC REFCLK4_P | << ADC_REFCLK4_P | [20] |
| L ADC_REFCLK4_N | << ADC_REFCLK4_N | [20] |
| L ADC REFCLK5_P | << ADC_REFCLK5_P | [20] |
| L ADC_REFCLK5_N | << ADC_REFCLK5_N | [20] |
| R ADC REFCLK0_N | <<R ADC_REFCLK0_P | [20] |
| R ADC_REFCLK0_P | <<R ADC_REFCLK0_N | [20] |
| R ADC REFCLK1_P | <<R ADC_REFCLK1_P | [20] |
| R ADC_REFCLK1_N | <<R ADC_REFCLK1_N | [20] |
| R ADC REFCLK2_P | <<R ADC_REFCLK2_P | [20] |
| R ADC_REFCLK2_N | <<R ADC_REFCLK2_N | [20] |
| R ADC REFCLK3_P | <<R ADC_REFCLK3_P | [20] |
| R ADC_REFCLK3_N | <<R ADC_REFCLK3_N | [20] |
| R ADC REFCLK4_P | <<R ADC_REFCLK4_P | [20] |
| R ADC_REFCLK4_N | <<R ADC_REFCLK4_N | [20] |
| R ADC REFCLK5_P | <<R ADC_REFCLK5_P | [20] |
| R ADC_REFCLK5_N | <<R ADC_REFCLK5_N | [20] |
| FPGA ADC CLK1P | <<FPGA_ADC_CLK1P | [12] |
| FPGA_ADC_CLK1N | <<FPGA_ADC_CLK1N | [12] |
| FPGA_ADC_CLK2P | <<FPGA_ADC_CLK2P | [12] |
| FPGA_ADC_CLK2N | <<FPGA_ADC_CLK2N | [12] |
| CLK_SYNC CLK1_IN | <<CLK_SYNC_CLK1_IN | [6] |
| CLK_SYNC SDIO | <<CLK_SYNC_SDIO | [13] |
| CLK_SYNC CS# | <<CLK_SYNC_CS# | [13] |
| CLK_SYNC SCLK | <<CLK_SYNC_SCLK | [13] |
| CLK_SYNC RESET | <<CLK_SYNC_RESET | [13] |
| LMK OSCOUTP | <<LMK_OSCOUTP | [13] |
| LMK OSCOUTN | <<LMK_OSCOUTN | [13] |
| LMK SYSREF/SYNC | <<LMK_SYSREF/SYNC | [13] |
- R18B3 100K 1% CLK_SYNC RESET
- | | | |
|--------------|----------------|------|
| CONN_CLKINO | <<CONN_CLKINO | [20] |
| CONN_CLKING# | <<CONN_CLKING# | [20] |
| STATUS_LD1 | <<STATUS_LD1 | [6] |
| STATUS_LD2 | <<STATUS_LD2 | [6] |
| LMK_CLKINO | <<LMK_CLKINO | [12] |
| LMK_CLKING# | <<LMK_CLKING# | [12] |

DECAPS



Cad Note: Place the Decaps close to each power pins

Variant Name															LMK_CLKIN0# [12]	
REV NO.	NATURE OF CHANGE			APPROVED BY	DATE	 Mistral Solutions [P] Ltd. #60 Adarsh regent,100 Feet Ring Road, Domlur Extension Bangalore 560 071, Ph : +91-80-2535 6400, Fax :+91-80-25356444		Title		LMK04832 - ADC CLK GEN.						
								Size	Document Number	MS_HFFES_FEC_SCH_REVA					Rev	
								C							A	
						Drawn by: ARUJEET Date: Monday, January 02, 2012		Approved by: SRIDHAR TS Date: Tuesday, November 21, 2023								
						Design file path:										
								Date: Tuesday, November 21, 2023		Sheet	17	of	25			