

PCIE CLOCK BUFFER

The diagram illustrates the PCIE Clock Buffer circuit, centered around the LMK00334RTVT clock buffer. The circuit is divided into several functional blocks:

- Power Input and Decoupling:** VPP3_OUT is connected to the buffer's power pins (10, 28, 30) through a 160 OHM, 6A resistor (FB19). Decoupling capacitors C10576, C10577, C10578, and C10579 (0.1uF, 50V) are placed across the power pins.
- Signal Input and Decoupling:** VPP3_OUT is connected to the buffer's signal pins (1, 2) through a 160 OHM, 6A resistor (FB20). Decoupling capacitors C10580 and C10581 (0.1uF, 50V) are placed across the signal pins.
- Signal Output and Decoupling:** VPP3_OUT is connected to the buffer's signal pins (1, 2) through a 160 OHM, 6A resistor (FB21). Decoupling capacitors C10582 and C10583 (0.1uF, 50V) are placed across the signal pins.
- Signal Traces:** The buffer's output pins (CLKOUTA0, CLKOUTA1, CLKOUTB0, CLKOUTB1) are connected to the signal traces (CLKOUTA0, CLKOUTA1, CLKOUTB0, CLKOUTB1) through 0 OHM resistors (R11025, R11026, R11027, R11028).
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The LMK00334RTVT clock buffer is shown with its pins (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31) and its internal components (R11025, R11026, R11027, R11028).

Legend:

- PCIE_OPS_REFLCK_P
- PCIE_OPS_REFLCK_M
- PCIE_AF50T_REFLCK_P
- PCIE_AF50T_REFLCK_M
- PCIE_NVMa_REFLCK_P
- PCIE_NVMa_REFLCK_M

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Legend:

- PCIE_OPS_REFCLK_P
- PCIE_OPS_REFCLK_M
- PCIE_AF50T_REFCLK_P
- PCIE_AF50T_REFCLK_M
- PCIE_NVMa_REFCLK_P
- PCIE_NVMa_REFCLK_M

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```
ERROR: undefined: lename
OFFENDING COMMAND: reviewresult.txt
STACK:
```