4.5.1 Case 1a/b/c: Synchronization of multiple LMK0482x in Distribution mode

4.5.1.1 Overview

The LMK0482x configured to operate in distribution mode uses the external VCO path (CLKin1) for PLL2 to provide a clock to the dividers and outputs. Follow the yellow path in Figure 17 and Figure 19 to see how the distribution clock is delivered to the output clocks (e.g. DCLKout0) and how the distribution clock optionally re-clocks an incoming SYNC/SYSREF pulse on CLKin0.

By providing a SYNC pulse to the CLKin0 pin which meets a setup and hold time to CLKin1, it is possible to reset dividers of the LMK0482x deterministically.

After synchronization of device clock and SYSREF dividers the device may generate SYSREF locally (case 1a), re-clock the CLKin0 or SYNC input (case 1b), or directly analog bypass the CLKin0 to the outputs (case 1c).

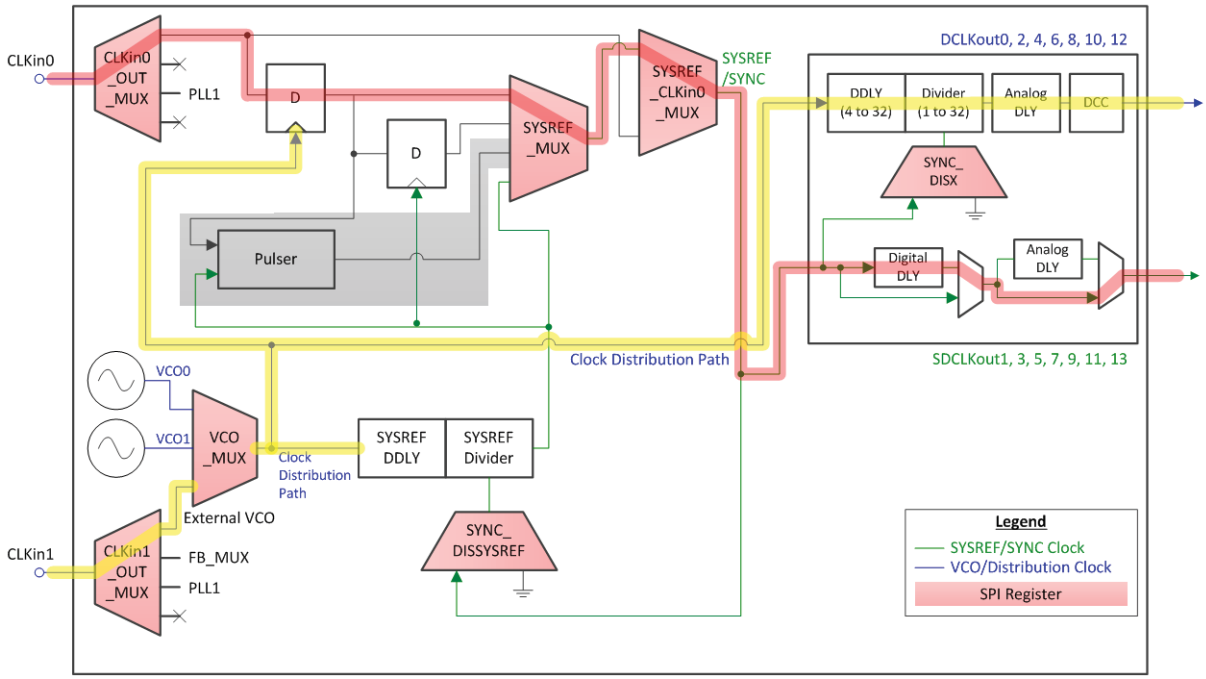

Figure 17 - CLKin0 and CLKin1 clocking paths highlighted for clock distribution mode

4.5.1.2 Procedure to Synchronize

4.5.1.2.1 Prepare to Synchronize LMK0482x dividers (was Basics) (??)

The slave LMK0482x is programmed as illustrated in Figure 17 to allow CLKin0 to reset all dividers. Follow recommended programming sequence from datasheet.

It is possible to synchronize the SYSREF and/or clock output dividers of the slave LMK0482x device in clock distribution mode using the CMOS SYNC pin. However, it is recommended to use the high speed CLKin0 path as illustrated in red highlight in Figure 17 for the SYNC/SYSREF clock. This path minimizes setup and hold times as compared to using the SYNC pin.

To allow the incoming SYSREF/SYNC signal to reset the dividers, the SYNC_DISX/SYNC_DISSYSREF bits must be clear for desired dividers. To reset on the rising edge, set SYNC_1SHOT_EN = 1. Only a single pulse is required reset the DCLKoutX and/or SYSREF dividers.

If the SDCLKoutY is powered up and selecting SYSREF with SYSREF_CLR = 0, then the same SYNC/SYSREF pulses which reset the dividers of the LMK0482x will also propagate to outside the chip. Powering down the output individually or with SYSREF_GBL_PD and appropriate SDCLKoutY_DIS_MODE, or setting SYSREF_CLR = 1 will prevent this from occurring.

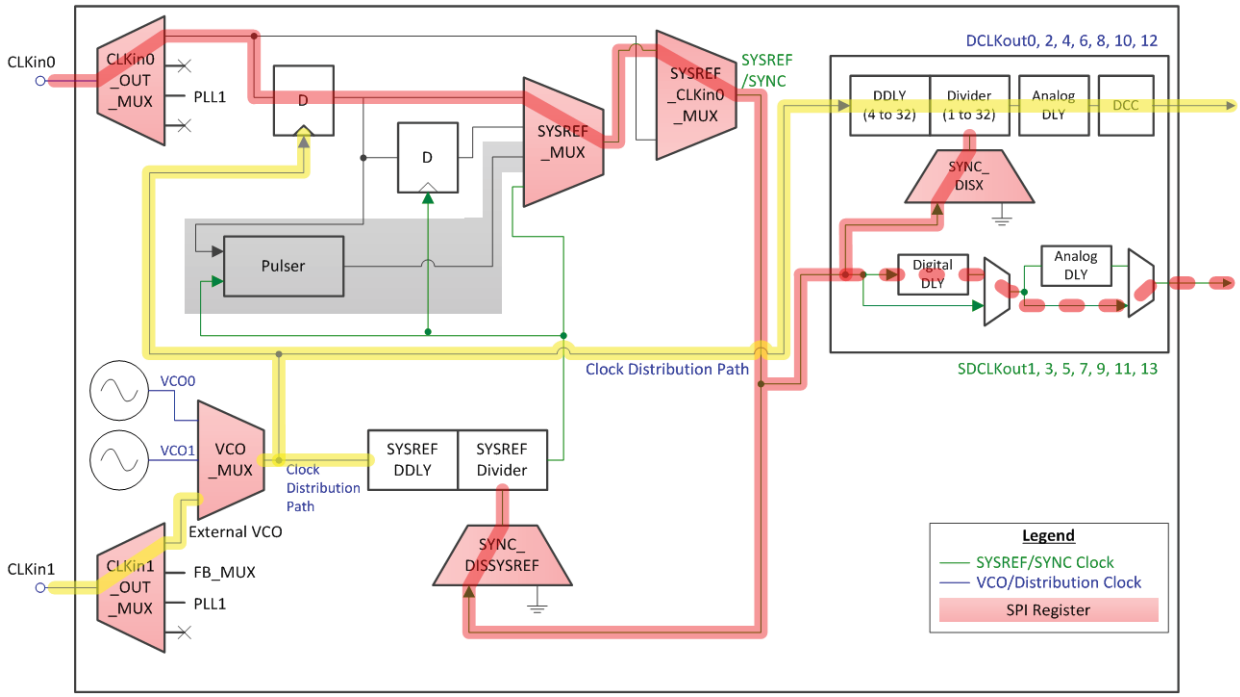

Figure 18 - Resetting dividers in distribution mode

To synchronize dividers, the key registers are:

Table 6 - Fundamental registers to setup slave in distribution mode

Address	Field	Value	Definition
Synchronization and clock routing path specific registers			
0x147[1:0]	CLKin0_OUT_MUX	0	Route CLKin0 to SYSREF_MUX
R313[0:1]	SYSREF_MUX	0	Route CLKin0 to SYSREF_CLKin0_MUX
R313[2]	SYSREF_CLKin0_MUX	0	Route SYSREF_MUX to SYSREF/SYNC Path
R324[0,1,2, 3,4,5,6,7]	SYNC_DISX, SYNC_DISSYSREF	0	Allow SYSREF/SYNC path to reset dividers as desired
R320[1]	SYSREF_DDLY_PD	0	Enable SYSREF DDLY
R316[0:4] & R317[0:7]	SYSREF_DDLY	?	As desired for global SYSREF DDLY
R262[7], … (Multiple)	DCLKoutX_DDLY_PD	0	Enable DCLKoutX_DDLY_PD
R257[0:3],[4:7], … (Multiple)	DCLKoutX_DDLY_CNTL DCLKoutX_DDLY_CNTH	? ?	As desired for device clock DDLY

	SYNC_MODE	0	Disables possibility of CMOS SYNC pin6 from causing a SYNC event. If desired, set to 1 to enable this path.
	SYSREF_PD	0	SYSREF Divider and circuitry powered up.

4.5.1.2.2 Synchronize DCLKoutX and SYSREF Dividers

Once the slave device is programmed to accept SYNC/SYSREF to reset its dividers, the SYNC event occurs. Now reconfigure the slave device as desired.

It is recommended for the external SYNC to arrive on DC coupled CLKin0. However the SYNC pin may also be used lower input frequencies.

4.5.1.2.3 Output of SYSREF

After the dividers are reset using the above configuration, the device may be reconfigured to generate SYSREF signals for downstream devices as illustrated in Figure 19. Here the SYNC_DISX/SYNC_DISSYSREF bits are re-programmed to prevent the SYSREF/SYNC signal from resetting the dividers, and the SYSREF_MUX is now selecting the pulser as the source for SYSREF signals. Note that other options would also be valid such as continuous mode (SYSREF_MUX = 3), re-clocked SYNC from CLKin0/SYNC pin (SYSREF_MUX = 1), or direct analog bypass of CLKin0 to SDCLKoutY (SYSREF_CLKin0_MUX = 1).

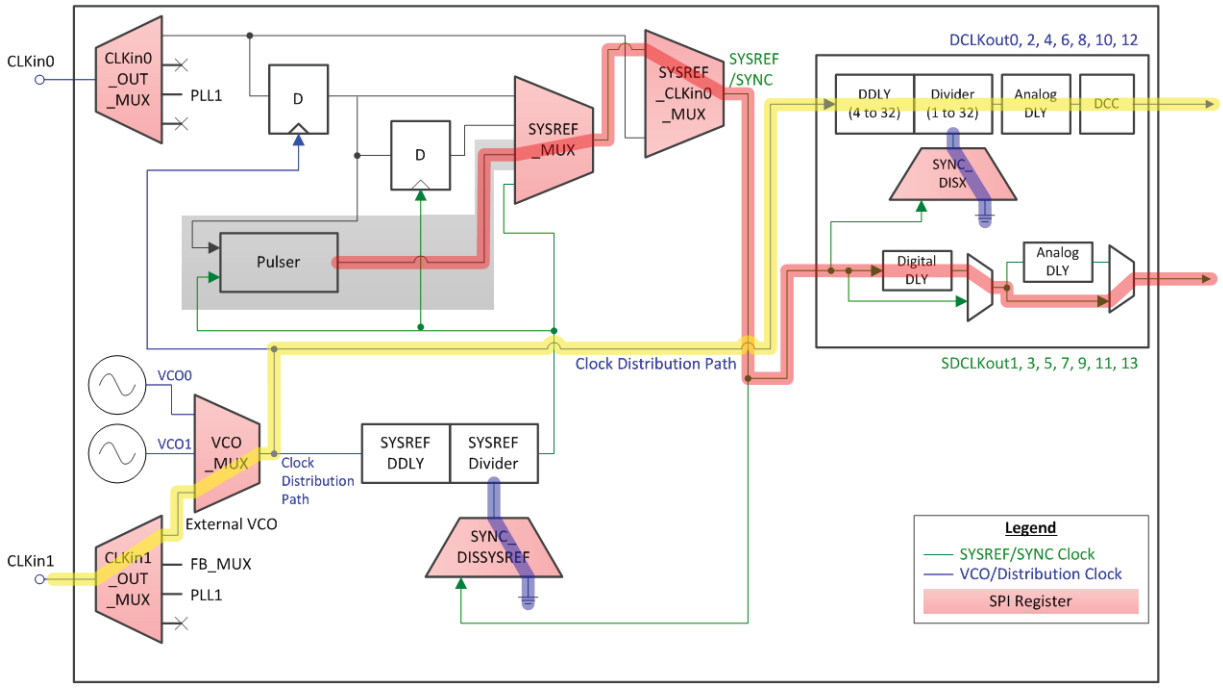

Figure 19 - Distribution with local SYSREF generation (simplified from Figure 10)

For this step, key registers are:

Address	Field	Value	Definition
	SYNC_DISX/ SYNC_DISSYSREF	1	Disable all SYNC

	SYNC_MODE	2 or 3	Select pin or SPI pulser trigger
	SYSREF_MUX	3	Select pulser
	SYSREF_CLR	0	SYSREF CLR must be 0 for operation

4.5.1.3 Example

This example will use two LMK04828 boards as illustrated in Figure 20. The master will be configured in a PLL2 mode with the VCXO of the master being hold at Vcc/2 by forcing holdover and using a manual DAC voltage setting. It is allowable to configure the master as dual loop and lock PLL1 if a signal generator is available.

is configured to generate a 983.04 MHz clock output from both DCLKout0 and DCLKout2. The master output's SDCLKout1 and SDCLKout3 will be configured to generate a single SYSREF pulse used to reset the dividers in the slave device in distribution mode. The phase of the slave's DCLKout0/SDCLKout1 can be compared against the master's DCLKout2 and SDCLKout3 to confirm the determinism. Naturally the clock outputs of the slave device will be deterministic and this can be measured on DCLKout0/2, SDCLKout1/3.

When connecting the boards together, take care to connect same polarity inputs and outputs. Unless an extra SMA is populated on the LMK04828 Slave board, DCLKout0* (inverting) will connect to CLKin1* (inverting).

4.5.1.3.1 Overview

The basic settings for master and slave are outlined in Table 7.

Table 7 – Case 1a/1b Demo Configuration

Setting	**Master**	**Slave**
Default Mode	Multi SYNC Master, Reference Free, 983.04 MHz, pulser	Multi SYNC Slave – Case 4b, 0-Delay SYSREF re-clocking; Sync from Master
OSCin Frequency	122.88 MHz	122.88 MHz
VCO Frequency	2949.12 MHz	2949.12 MHz
DCLKout0	983.04 MHz (/3)	122.88 MHz (/24)
DCLKout2	983.04 MHz (/3)	245.76 MHz (/12)
SYSREF Divider Frequency	12.288 MHz (/240)	122.88 MHz (/24)
SYSREF Mode	Pulser	Re-Clocked
FORCE_HOLDOVER	1	0
MAN_DAC	512 (Vcc/2)	N/A

4.5.1.3.2 Modify EVMs

Because this example uses the pulser for SYNC/SYSREF from master, it is necessary to modify the master for DC coupled SDCLKout1 output and the slave for DC coupled CLKin0 input. Refer to *APPENDIX B – Instructions for Modifying EVMs*, for detailed instructions.

4.5.1.3.3 Connecting EVMs together

When connecting the boards together, take care to connect same polarity inputs and outputs. Unless an extra SMA is populated on the LMK04828 Slave board, DCLKout0* (inverting) will connect to CLKin1* (inverting).

To connect the EVMs together, refer to the diagram in Figure 20. While the SDCLKout1 of the master must be DC coupled to differentially to CLKin0 of the slave for timing reasons, the outputs of the LMK04828 connected to the oscilloscope may be configured to AC or DC coupled as desired. If it is chosen to connect both the non-inverting and inverting output of an SDCLKout to the oscilloscope, it is recommended to use DC coupling so that the signals will not need time to bias to result in a proper, steady state, differential waveform.

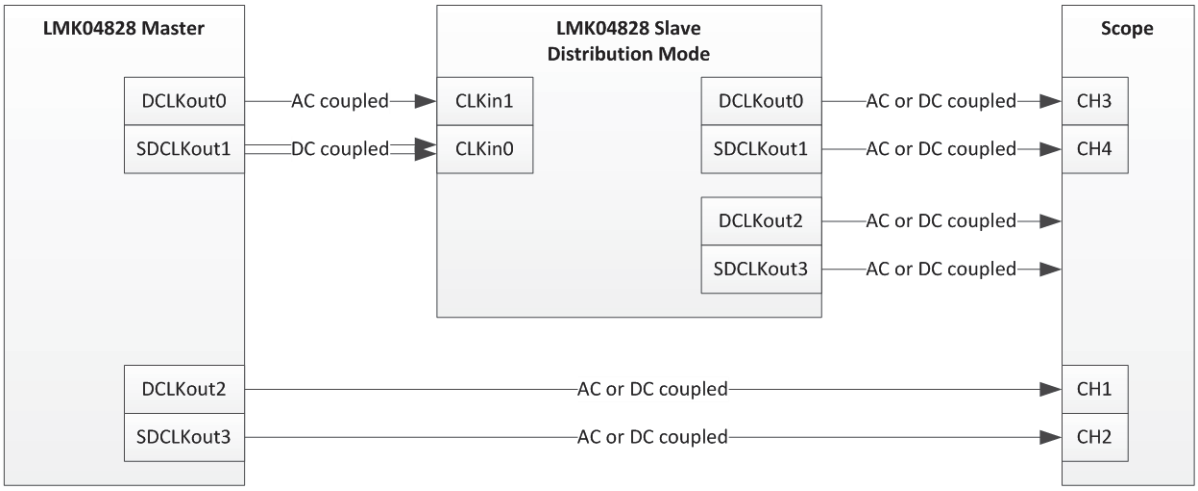

Figure 20 - Synchronization of Distribution LMK04828. PCB and test equipment connection diagram

4.5.1.3.4 Software Setup

Once the EVMs are modified and the connected together, connect the USB2ANYs from the PC to the EVMs. Start two copies of TICS Pro and load the LMK04828B profile for each device. To identify which EVM is being controlled by which TICS Pro instance select “USB communications” on the menu bar, and select “Interface” to open the Communication Setup window. Click the “Identify” button to flash the green LED on the USB2ANY controlled by the specific instance of TICS Pro.

On the TICS Pro controlling the master EVM

- click “Default configurations” on the menu bar, and
- select “Multi-sync demo, master, dual loop, cascaded 0-delay, without reference, 983.04 MHz”
    - This will load the LMK04828B EVM to be in dual loop mode, but will force holdover with a fixed voltage on the 122.88 MHz VCXO so that PLL2 will lock to reliable reference. Frequency may not be exactly 122.88 MHz.
        - When in holdover, output phase noise/jitter at offsets below 12 kHz may be impacted from holdover mode. Different VCXOs will have different sensitivity and offsets at which phase noise may degrade from a locked condition.
    - If it is desired to lock to answer external reference, connect a reference at 122.88 MHz to CLKin1 and uncheck FORCE_HOLDOVER on the User Controls page.

- Click “Write All Registers” button on the toolbar or press “Ctrl-L” to program the master LMK04828.
- Then press the “SYNC Dividers” button to synchronize all the dividers of the master.
- Confirm that the PLL2 DLD LED is lit next to the VCXO.

With the TICS Pro program controlling the slave EVM,

- click “Default configurations” on the menu bar, and
- select “Multi-sync demo, slave, distribution.”
    - This will load the LMK04828B EVM to have both PLLs powered down, route CLKin1 to distribution, and prepare the device to receive a SYNC/SYSREF pulse on CLKin0.
- Click “Write All Registers” button on the toolbar or press “Ctrl-L” to program the master LMK04828.

Now using the TICS Pro for master,

- on the SYSREF Page, click the “Send Pulses” button to launch a SYSREF pulse into the slave’s CLKin0 input. This will synchronize the dividers on the slave.

On the slave device

- on the “Set Modes” tab, click “Disable SYNC on all Dividers” button to prevent the dividers from responding to SYNC/SYSREF now that they’ve been aligned.
- Then select the desired JESD204B mode, “Continuous,” “Pulser,” or “SYSREF Request.”
    - For this example, selection “Continuous” so a continuous stream of SYSREF pulses are output which can be compared with the master.
    - **However in a real application**, “Pulser” would be the normal selection as it is undesirable to send continuous SYSREF pulses because of noise and power consumption.
        - In this real application, pulses would then be sent by programming SYSREF_PULSE_CNT or toggling the SYNC pin.

This concludes then necessary steps to get a system operational.

4.5.1.3.5 Further visualization, testing, and optimization

In a normal application, the system would now be operational, however to assist in visualization, on the master TICS Pro.

- set “Continuous” JESD204B mode to generate continuous SYSREF pulses which may be observed with respect to the slave.

It is also possible to observe the reset of the slave device dividers by observing the impact of reset timing on the device clocks. To do this, with the master in continuous SYSREF mode, on the slave

- On the “Set Modes” page click the “Receive SYNC/SYSREF on CLKin0” button.
    - Now the reset of the device clock maybe observed from slave device.
- On the “Clock Outputs” page uncheck
    - DDLY_PD for CLKout0
    - Change the digital delay value by adjusting the two comboboxes immediately below the DDLY_PD. Half Step may also be checked.

To determine the position in the valid window for the slave to properly receive the SYNC/SYSREF signal with respect to its device clock, on the master refer to APPENDIX C – Adjusting Timing from a Master Device for maximum setup and Hold Time.

4.5.1.4 General Usage of TICS Pro

For any given setup, to get to a device in clock distribution mode to sync, on the Set Modes page, click…

- "Set Distribution" to put the device into distribution mode.
- "Reclocked CLKin0" to set CLKin0 to reset dividers.
- "Enable SYNC for SYSREF" and "Enable SYNC for CLKout Dividers"

Once SYNC occurs, click "Disable SYNC for all Dividers"

Naturally all device clock and SYSREF clock outputs need to be configured as desired.