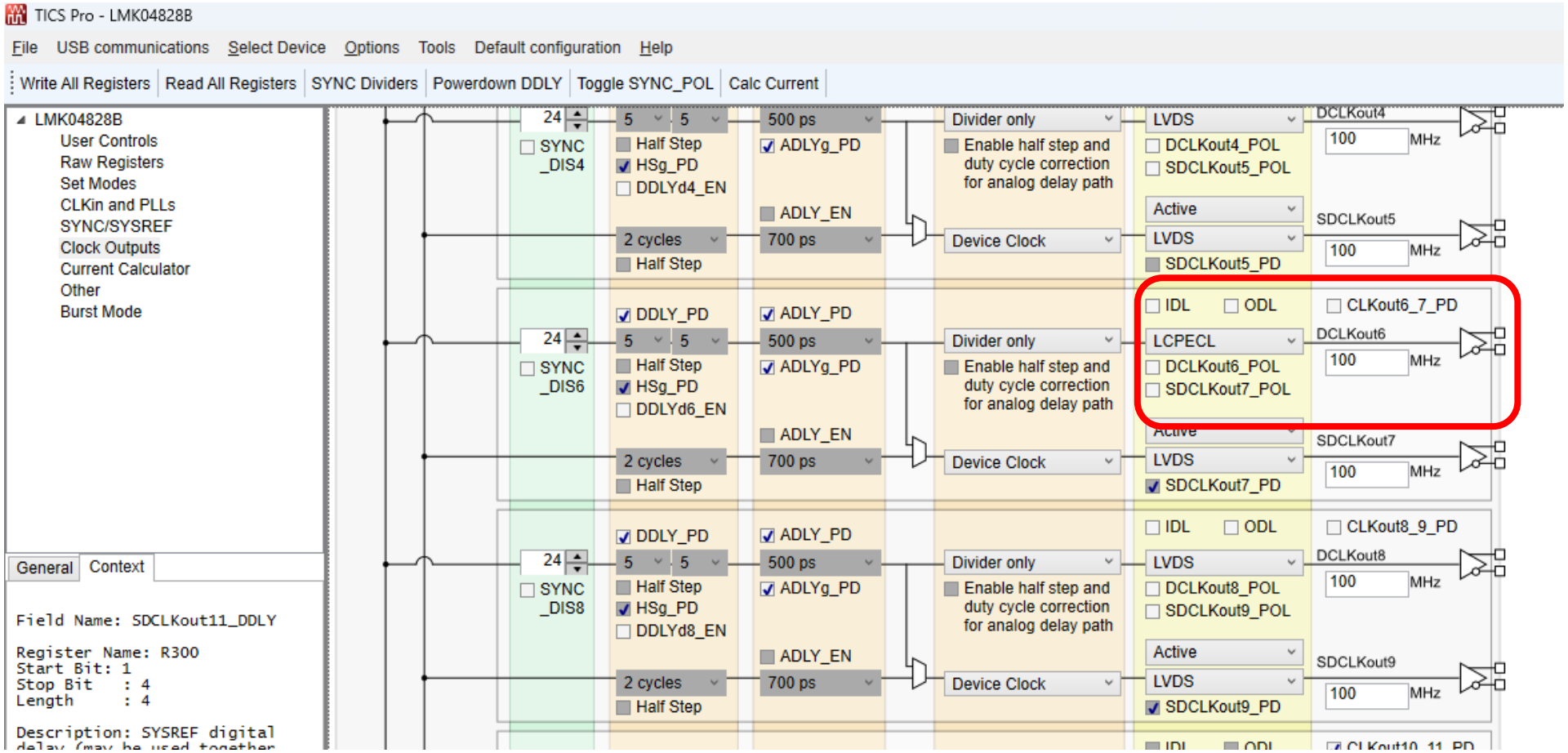
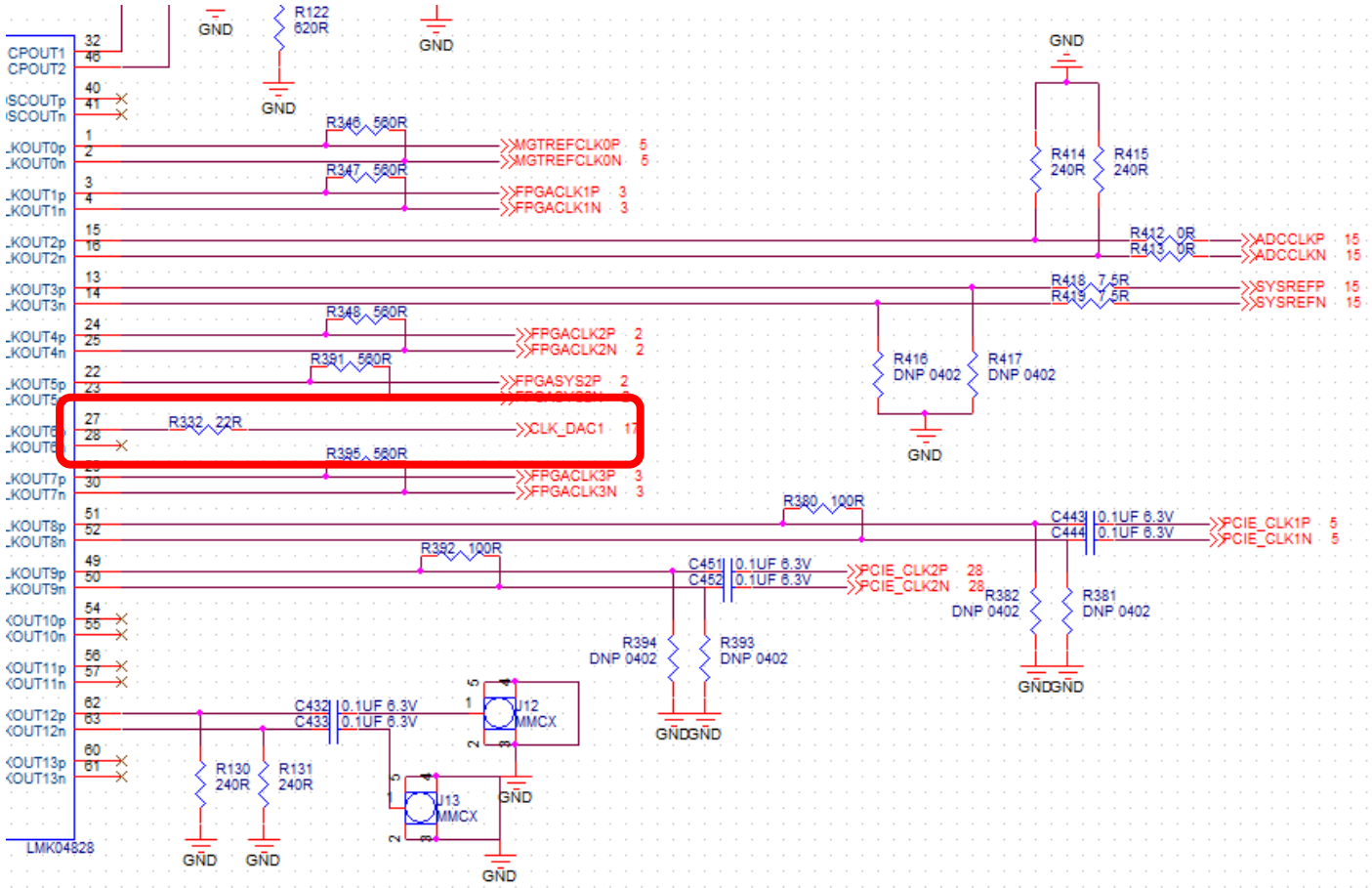
Notes

LMK04828: TICS Pro



Schematic


LMK04828
CPOUT1
CPOUT2
SCOUTp
SCOUTn
KOUT0p
KOUT0n
KOUT1p
KOUT1n
KOUT2p
KOUT2n
KOUT3p
KOUT3n
KOUT4p
KOUT4n
KOUT5p
KOUT7p
KOUT7n
KOUT8p
KOUT8n
KOUT9p
KOUT9n
OUT10p
OUT10n
OUT11p
OUT11n
OUT12p
OUT12n
OUT13p
OUT13n
GND
R122 620R
R346 560R
R347 560R
R348 560R
R391 560R
R332 22R
R395 560R
R380 100R
R392 100R
MGTREFCLK0P 5
MGTREFCLK0N 5
FPGACLK1P 3
FPGACLK1N 3
FPGACLK2P 2
FPGACLK2N 2
FPGASYS2P 2
CLK_DAC1 17
FPGACLK3P 3
FPGACLK3N 3
R414 240R
R415 240R
R412 0R
R413 0R
ADCCLKP 15
ADCCLKN 15
R418 7.5R
R419 7.5R
SYSREFP 15
SYSREFN 15
R416 DNP 0402
R417 DNP 0402
C443 0.1UF 6.3V
C444 0.1UF 6.3V
PCIE_CLK1P 5
PCIE_CLK1N 5
C451 0.1UF 6.3V
C452 0.1UF 6.3V
PCIE_CLK2P 28
PCIE_CLK2N 28
R382 DNP 0402
R381 DNP 0402
R394 DNP 0402
R393 DNP 0402
C432 0.1UF 6.3V
C433 0.1UF 6.3V
U12 MMCX
U13 MMCX
R130 240R
R131 240R

LMK04828 Spec
VCC = 3.3

		(1600 or 2000 mVpp)		
1600-mVpp LVPECL CLOCK OUTPUTS (DCLKoutX and SDCLKoutY)				
V_{OH}	Output high voltage	DC measurement Termination = 50 Ω to V_{CC} - 2.0 V	V_{CC} - 1.04	V
V_{OL}	Output low voltage		V_{CC} - 1.80	V
V_{OD}	Output voltage Figure 9		760	|mV|
2000-mVpp LVPECL CLOCK OUTPUTS (DCLKoutX and SDCLKoutY)				
V_{OH}	Output high voltage	DC measurement Termination = 50 Ω to V_{CC} - 2.3 V	V_{CC} - 1.09	V
V_{OL}	Output low voltage		V_{CC} - 2.05	V
V_{OD}	Output voltage Figure 9		960	|mV|
LCPECL CLOCK OUTPUTS (DCLKoutX and SDCLKoutY)				
V_{OH}	Output high voltage	DC measurement Termination = 50 Ω to 0.5 V	1.57	V
V_{OL}	Output low voltage		0.62	V
V_{OD}	Output voltage Figure 9		950	|mV|

2.26

1.5

2.21

1.25

THS5641A Digital Input Spec

digital specifications

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Interface							
V_{IH}	High-level input voltage		DV_{DD} = 5 V	3.5	5		V
			DV_{DD} = 3.3 V	2.1	3.3		
V_{IL}	Low-level input voltage		DV_{DD} = 5 V		0	1.3	V
			DV_{DD} = 3.3 V		0	0.9	
		MODE and SLEEP	DV_{DD} = 3 V to 5.5 V	−15		15	