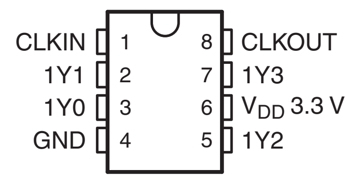
3.3-V CLOCK PHASE-LOCKED LOOP CLOCK DRIVER

FEATURES

- **Qualified for Automotive Applications**
- **Phase-Locked Loop Clock Driver for Synchronous DRAM and General-Purpose Applications**
- **Spread-Spectrum Clock Compatible**
- **Operating Frequency: 24 MHz to 200 MHz**
- **Low Jitter (Cycle-to-Cycle): <150 ps Over the Range 66 MHz to 200 MHz**
- **Distributes One Clock Input to One Bank of Five Outputs (CLKOUT Is Used to Tune the Input-Output Delay)**
- **Three-States Outputs When There Is No Input Clock**
- **Operates From Single 3.3-V Supply**
- **Available in 8-Pin SOIC Package**
- **Consumes Less Than 100 μA (Typically) in Power Down Mode**
- **Internal Feedback Loop Is Used to Synchronize the Outputs to the Input Clock**
- **25-Ω On-Chip Series Damping Resistors**
- **Integrated RC PLL Loop Filter Eliminates the Need for External Components**

D PACKAGE
(TOP VIEW)



DESCRIPTION

The CDCVF2505 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks (1Y[0–3] and CLKOUT) to the input clock signal (CLKIN). The CDCVF2505 operates at 3.3 V. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs provides low-skew, low-jitter copies of CLKIN. Output duty cycles are adjusted to 50 percent, independent of duty cycle at CLKIN. The device automatically goes in power-down mode when no input signal is applied to CLKIN.

Unlike many products containing PLLs, the CDCVF2505 does not require an external RC network. The loop filter for the PLLs is included on-chip, minimizing component count, space, and cost.

Because it is based on the PLL circuitry, the CDCVF2505 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN, and following any changes to the PLL reference.

The CDCVF2505 is characterized for operation from –40°C to 85°C.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Reel of 2500	CDCVF2505IDRQ1	CKV05Q

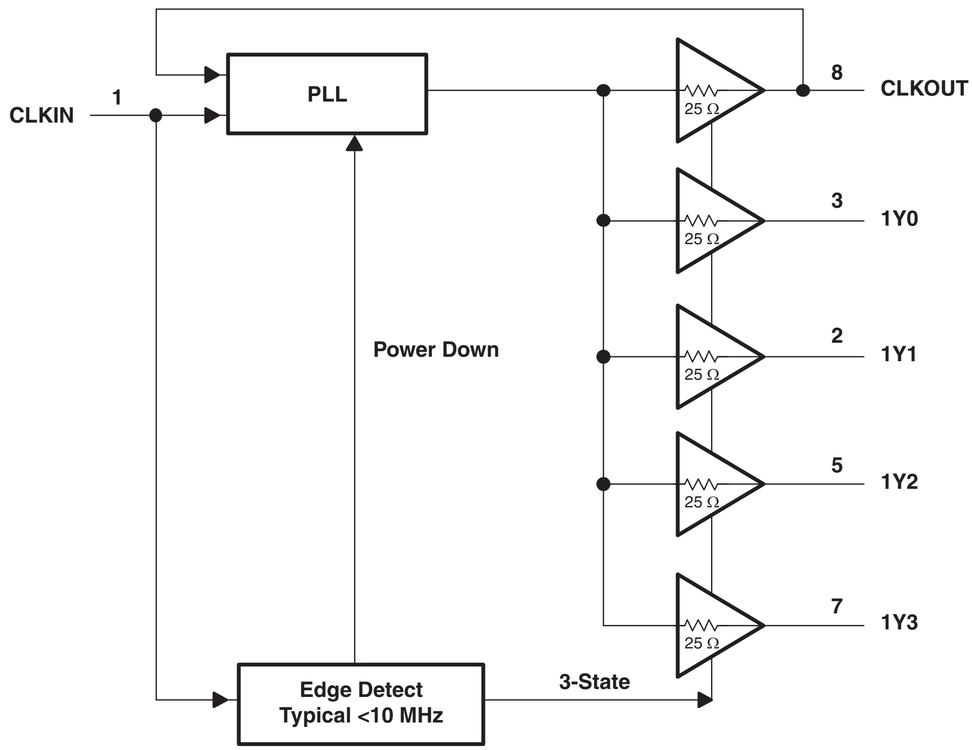
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE

INPUT	OUTPUTS	
CLKIN	1Y[0–3]	CLKOUT
L	L	L
H	H	H
<10 MHz[(1)]	Z	Z

(1) Below 2 MHz (typical) the device goes into power-down mode, during which the PLL is turned off and the outputs enter into Hi-Z mode. If a >10-MHz signal is applied at CLKIN, the PLL turns on, reacquires lock, and stabilizes after approximately 100 µs. The outputs are then enabled.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
1Y0	3	O	Clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series damping resistor.
1Y1	2		
1Y2	5		
1Y3	7		
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF2505 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid signal is applied, a stabilization time (100 µs) is required for the PLL to phase lock the feedback signal to CLKIN.
CLKOUT	8	O	Feedback output. CLKOUT completes the internal feedback loop of the PLL. This connection is made inside the chip and an external feedback loop should NOT be connected. CLKOUT can be loaded with a capacitor to achieve zero delay between CLKIN and the Y outputs.
GND	4	Power	Ground
V_{DD}3.3V	6	Power	3.3-V supply

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage range		–0.5 V to 4.3 V
V_I	Input voltage range[2][3]		–0.5 V to V_{DD} + 0.5 V
V_O	Output voltage range[2][3]		–0.5 V to V_{DD} + 0.5 V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	±50 mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	±50 mA
I_O	Continuous total output current	$V_O = 0$ to V_{DD}	±50 mA
θ_{JA}	Package thermal impedance[4]		97.1°C/W
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.3 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTROSTATIC DISCHARGE INFORMATION

ESD MODEL		LIMIT
HBM	Human-Body Model	2000 V
MM	Machine Model	300 V
CDM	Charged-Device Model	1000 V

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	0.7 × V_{DD}			V
V_{IL}	Low-level input voltage			0.3 × V_{DD}	V
V_I	Input voltage	0		V_{DD}	V
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–40		85	°C

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency		24		200	MHz
	Input clock duty cycle	24 MHz to 85 MHz[1]	30		85	%
		86 MHz to 200 MHz	40	50	60	
	Stabilization time[2]				100	µs

(1) Specified by design.
(2) Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{DD}	MIN	TYP[(1)]	MAX	UNIT
V_{IK}	Input voltage		I_I = –18 mA	3 V			–1.2	V
V_{OH}	High-level output voltage		I_{OH} = –100 µA	MIN to MAX	V_{DD} – 0.2			V
			I_{OH} = –12 mA	3 V	2.1			
			I_{OH} = –6 mA	3 V	2.4			
V_{OL}	Low-level output voltage		I_{OL} = 100 µA	MIN to MAX			0.2	V
			I_{OL} = 12 mA	3 V			0.8	
			I_{OL} = 6 mA	3 V			0.55	
I_{OH}	High-level output current		V_O = 1 V	3 V	–27			mA
			V_O = 1.65 V	3.3 V		–36		
I_{OL}	Low-level output current		V_O = 2 V	3 V	27			mA
			V_O = 1.65 V	3.3 V		40		
I_I	Input current		V_I = 0 V or V_{DD}				±5	µA
C_i	Input capacitance		V_I = 0 V or V_{DD}	3.3 V		4.2		pF
C_o	Output capacitance	Yn	V_I = 0 V or V_{DD}	3.3 V		2.8		pF
		CLKOUT				5.2		

(1) All typical values are at nominal V_{DD} and T_A = 25°C.

SWITCHING CHARACTERISTICS[(1)]

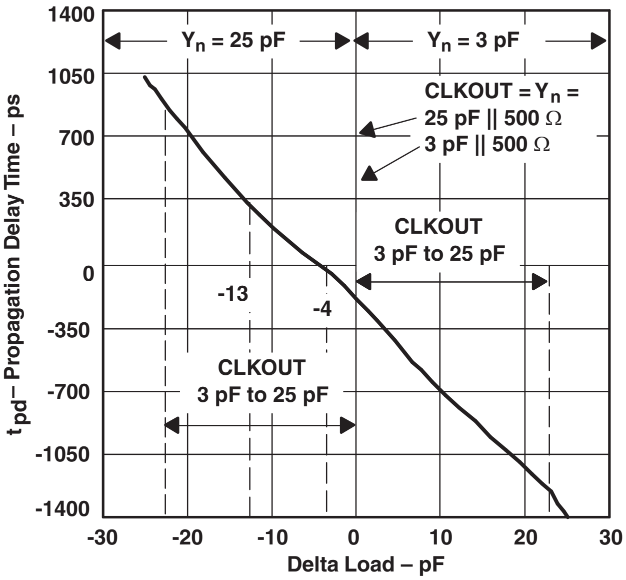
over recommended ranges of supply voltage and operating free-air temperature, C_L = 25 pF, V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(2)]	MAX	UNIT
t_{pd}	Propagation delay, normalized (see Figure 1)	CLKIN to Yn, f = 66 MHz to 200 MHz	–150		150	ps
$t_{sk(o)}$	Output skew[(3)]	Yn to Yn			150	ps
$t_{c(jit\_cc)}$	Jitter (cycle to cycle) (see Figure 5)	f = 66 MHz to 200 MHz		70	150	ps
		f = 24 MHz to 50 MHz		200	400	
odc	Output duty cycle (see Figure 4)	f = 24 MHz to 200 MHz at 50% V_{DD}	45		55	%
t_r	Rise time	V_O = 0.4 V to 2 V	0.5		2	ns
t_f	Fall time	V_O = 2 V to 0.4 V	0.5		2	ns

(1) Not production tested
(2) All typical values are at nominal V_{DD} and T_A = 25°C.
(3) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

TYPICAL CHARACTERISTICS

t_{PD}, PROPAGATION DELAY TIME vs DELTA LOAD (TYPICAL VALUES at 3.3 V, 25°C) CLOCK FREQUENCY, f = 100 MHz



NOTE: Delta Load = CLKOUT Load – Yn Load

Figure 1.

t_{pd}, PROPAGATION DELAY TIME vs FREQUENCY (TYPICAL VALUES at 3.3 V, 25°C)

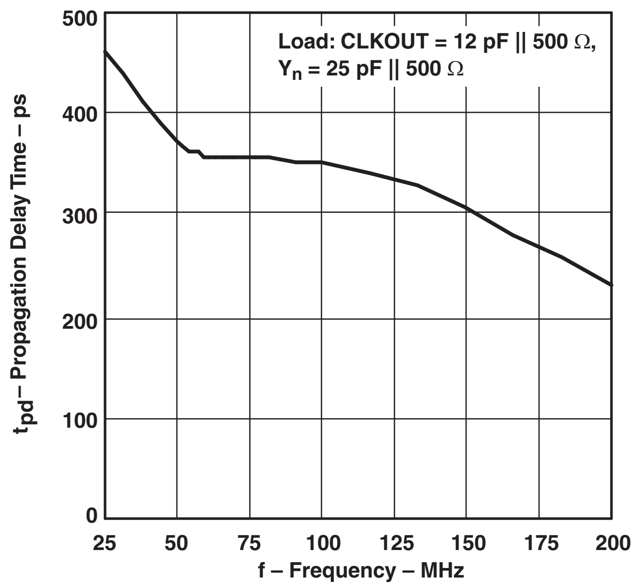


Figure 2.

t_{pd}, TYPICAL PROPAGATION DELAY TIME vs FREQUENCY (TUNED FOR MINIMUM DELAY)

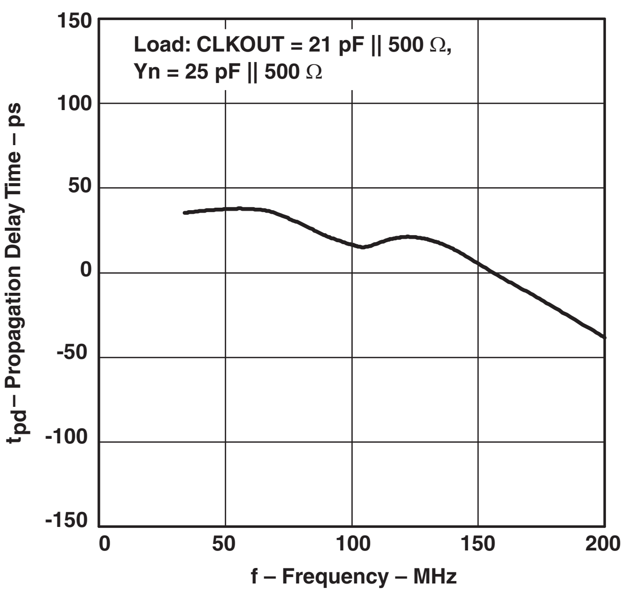


Figure 3.

DUTY CYCLE vs FREQUENCY

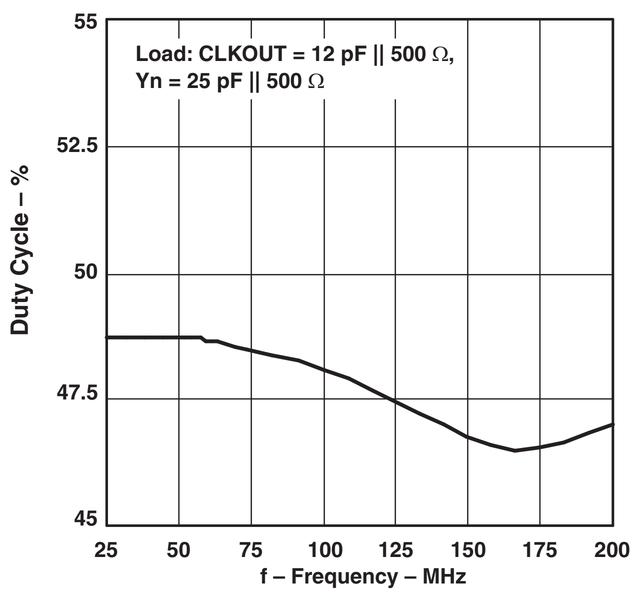


Figure 4.

TYPICAL CHARACTERISTICS (continued)

CYCLE-to-CYCLE JITTER vs FREQUENCY

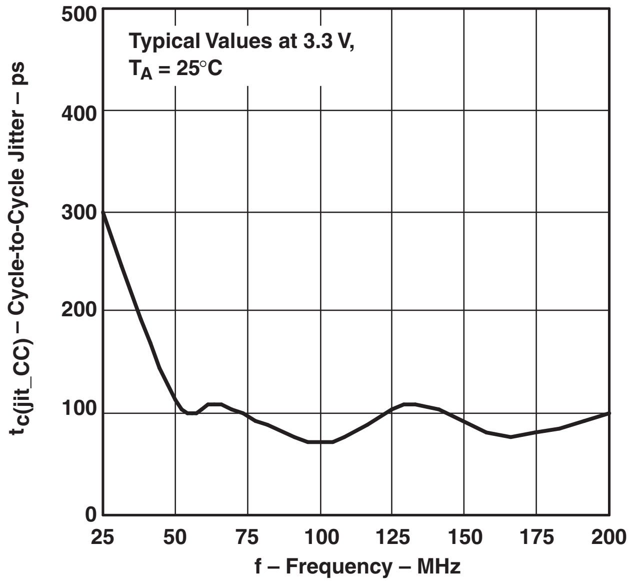


Figure 5.

I_{CC}, SUPPLY CURRENT vs FREQUENCY

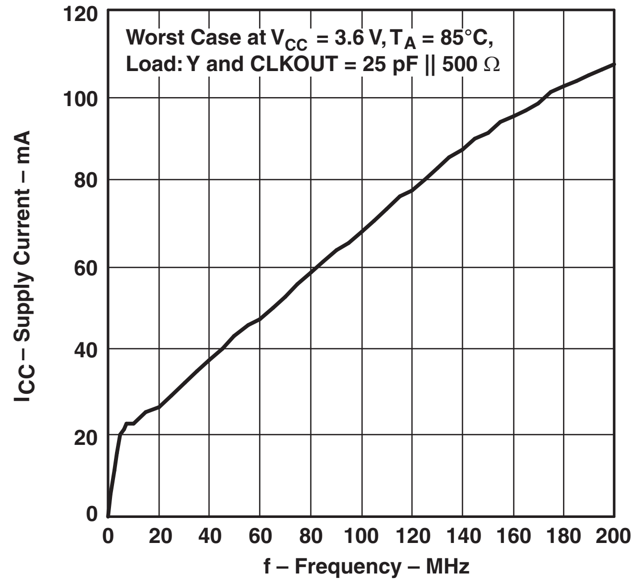


Figure 6.

PARAMETER MEASUREMENT INFORMATION

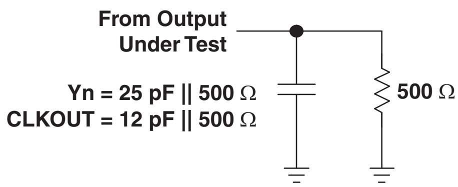


Figure 7. Test Load Circuit

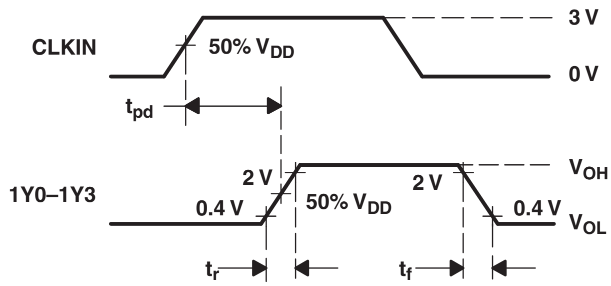


Figure 8. Voltage Threshold for Measurements, Propagation Delay (t_{pd})

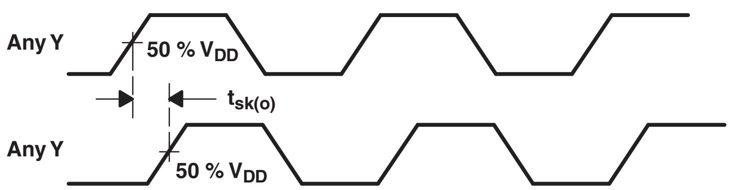
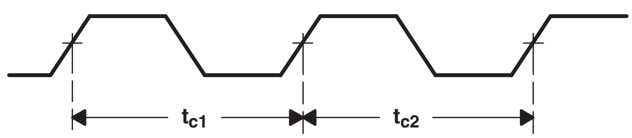


Figure 9. Output Skew



$t_{c(jit\_CC)} = t_{c1} - t_{c2}$

Figure 10. Cycle-to-Cycle Jitter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2505IDRQ1	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV05Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CDCVF2505-Q1 :

- Catalog: CDCVF2505

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product