Application Report
SNVA009AG–September 1999–Revised August 2015

AN-1112 DSBGA Wafer Level Chip Scale Package

ABSTRACT

This application note provides information about the Die Size BGA (DSBGA) Wafer Level Chip Scale Package (WLCSP).

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1 Introduction

DSBGA is a wafer level CSP (WLCSP) with the following features:

- Package size equal to die size
- Smallest footprint per I/O count
- Interconnect layout available in 0.3, 0.35, 0.4 or 0.5 mm pitch
- No interposer between the silicon IC and the printed circuit board
- Both Lead-free and Eutectic solder versions available. Refer to Application Report , Forward/Backward Compatibility SNOA923 for details.
- TI DSBGA products are designed and tested to ensure excellent board-level thermal cycling reliability without the need for underfill in intended applications. If a customer chooses to underfill a DSBGA product, TI recommends following the guidelines below to maximize reliability.
  - The underfill fillet should extend partially up the die edges. Underfill that ends at the bottom (ball side) of the die will degrade reliability.
  - The underfill should have a CTE closely matched to the CTE of the solder interconnect.
  - The underfill should have a Tg above the expected maximum exposure temperature.

2 Package Construction

Figure 1 shows typical DSBGA products. They have solder bumps located on the active side of silicon IC. The DSBGA is offered in thin, ultra-thin and extreme-thin version. The DSBGA manufacturing process steps include standard wafer fabrication process, wafer re-passivation, deposition of solder bumps on i/o pads, backgrinding (for thin version), application of protective encapsulation coating, testing using wafer sort platform, laser marking, singulation and packing in tape and reel. The package is assembled on PCB using standard surface mount assembly techniques (SMT).

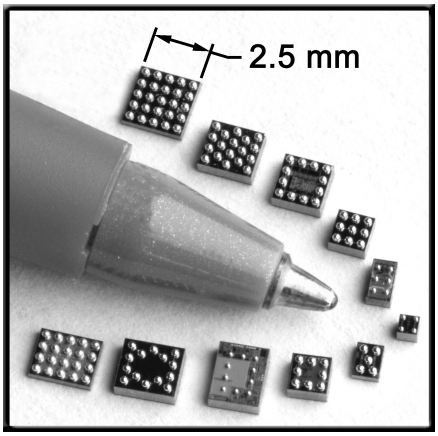


Figure 1. DSBGA 4–25 Bump

3 DSBGA Package Data

Table 1. Package Arrays

Bump Count	Array Outline
4	2 x 2
5	2 x 1 x 2
6	3 x 2
8	3 x 3 (perimeter)
8	4 x 2 (perimeter)
9	3 x 3 (area)
10	4 x 3 (perimeter)
12	4 x 3 (area)
12	4 x 4 (perimeter)
14	5 x 4 (stagger perimeter)
16	4 x 4 (area)
18	5 x 4 (stagger area)
20	4 x 5 (area)
25	5 x 5 (area)
30	5 x 6 (area)
64	8 x 8 (area)

Table 2. Bump Size Options

	0.5 mm Pitch			0.4 mm Pitch		0.35 mm Pitch	0.3 mm Pitch
	0.170 mm Diameter	0.275 mm Diameter	0.320 mm Diameter	0.240 mm Diameter	0.265 mm Diameter	0.200 mm Diameter	0.210 mm Diameter
I/O Count Range	4 – 9	4 — 16	4 – 30	4 — 9	4 – 64	4 — 56	4 – 30
Thin Package Thickness (mm)	0.5	0.5	0.6	N/A	0.6	N/A	0.55
Ultra-Thin Package Thickness (mm)	0.35	0.35	N/A	0.35	0.425 (4 – 30)	0.4	N/A
Extreme-Thin Package Thickness (mm)	0.25	0.25	N/A	0.25	N/A	N/A	N/A
Bump Height (mm)	0.11 – 0.15	0.11 — 0.15	0.21 – 0.26	0.11 — 0.15	0.165 – 0.205	0.14 — 0.18	0.145 – 0.185
Bump Coplanarity within package (mm)	<0.03	<0.05	<0.05	<0.05	<0.05	<0.05	<0.05
Shipping Media	Tape & Reel			Tape & Reel		Tape & Reel	Tape & Reel
Moisture Sensitivity Level (MSL)	Level 1			Level 1		Level 1	Level 1

4 Surface Mount Assembly Considerations

DSBGA surface mount assembly operations include:

- Printing solder paste onto a PCB.
- Component placement using standard pick and place equipment.
- Solder reflow and cleaning (depending on flux type).

Advantages of DSBGA during SMT assembly include,

- Standard tape and reel shipping media eases handling issues (per EIA-481-1)
- Requires standard SMT pick and place equipment.
- Standard reflow process (both Lead-free and Eutectic compatible).

0.5 mm pitch Large Dome Bump micro DSBGA: Recommendations for SMT assembly are the same as those used for 0.32 mm bump diameter micro DSBGA.

The 0.5 mm pitch Large Dome Bump DSBGA achieves the same bump height as the 0.5 mm pitch, 0.17 mm ball size version. This results in a package thickness that enables adoption in applications where lowest possible package thickness is desired. The large dome bump DSBGA has solder joint strength of >250 gm per joint which is higher than that of the 0.17 mm ball size at ~80 gm per joint, but is lower than that of the 0.3 mm ball DSBGA at >300 gm per joint.

5 PCB Layout

Two types of PCB land patterns are used for surface mount packages:

1. Non-solder mask defined (NSMD)
2. Solder mask defined (SMD).

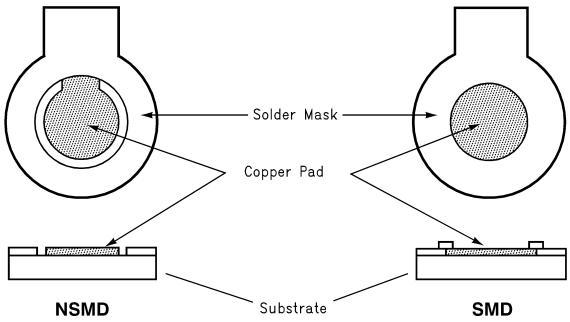


Figure 2. NSMD and SMD Pad Definition

1. The NSMD configuration is preferred due to its tighter control of the copper etch process and a reduction in the stress concentration points on the PCB side compared to SMD configuration.
2. A copper layer thickness of less than 1 oz is recommended to achieve higher solder joint stand-off. A 1 oz. (30 micron) or greater copper thickness causes a lower effective solder joint stand-off, which may compromise solder joint reliability.
3. For the NSMD pad geometry, the trace width at the connection to the land pad should not exceed 2/3 of the pad diameter.

The recommended pad geometry is shown in Table 3 and Table 4.

Table 3. Recommended PCB Pad Geometry — 0.4 & 0.5 mm pitch

	0.5 mm Pitch				0.4 mm Pitch	
Solder Ball Diameter	**0.170 mm**		**0.275 & 0.320 mm**		**0.240 & 0.265 mm**	
Pad Definition	**Copper Pad**	**Solder Mask Opening**	**Copper Pad**	**Solder Mask Opening**	**Copper Pad**	**Solder Mask Opening**
NSMD	0.165 ± 0.020 mm	0.265 ± 0.025 mm	0.265 ± 0.020 mm	0.365 ± 0.025 mm	0.225 ± 0.02 mm	0.325 ± 0.02 mm
SMD	0.265 ± 0.020 mm	0.165 ± 0.025 mm	0.365 ± 0.020 mm	0.265 ± 0.025 mm	0.325 ± 0.02 mm	0.225 ± 0.02 mm

Table 4. Recommended PCB Pad Geometry — 0.3 & 0.35 mm pitch

	0.3 mm Pitch		0.35 mm Pitch	
Solder Ball Diameter	**0.210 mm**		**0.200 mm**	
Pad Definition	**Copper Pad**	**Solder Mask Opening**	**Copper Pad**	**Solder Mask Opening**
NSMD	0.160 ± 0.015 mm	0.225 ± 0.015 mm	0.180 ± 0.020 mm	0.245 ± 0.020 mm
SMD	0.225 ± 0.015 mm	0.160 ± 0.015 mm	0.245 ± 0.020 mm	0.180 ± 0.020 mm

For PCB layouts employing via-in-pad structures (micro-via), NSMD pad definition should be used, since this ensures adequate wetting area on the copper pads and hence a better joint. It is also recommended that the wall thickness of the microvias be a minimum of 15 microns. It is also recommended that 'offset' vias be used when microvias are required for routing on the PCB.

Organic solderability preservative coating (OSP) as well as ENIG (Electroless Nickel Immersion Gold) finish is used for internal characterization.

- For Ni-Au (electroplated Nickel, immersion Gold) gold thickness must be less than 0.2 microns to avoid solder joint embrittlement.
- The fan-out for the traces should be symmetrical across X and Y directions to avoid part rotation due to surface tension of solder.

- HASL (Hot Air Solder Leveled) board finish is not recommended.

6 Stencil Printing Process

- Use laser cutting followed by electro-polishing for stencil fabrication.
- The recommended stencil apertures are shown in *Table 5*.
- If possible, offset apertures from land pads to maximize separation and minimize possibility of bridging for DSBGA packages with less than 10 bump counts with small bump size. No print offset is required for higher bump counts and larger bump size.
- Use Type 3 (25 to 45 micron particle size range) or finer solder paste for printing.

Table 5. Recommended Stencil Apertures

	0.5 mm Pitch		0.4 mm Pitch	0.35 mm Pitch	0.3 mm Pitch
Solder Ball Diameter	**0.170**	**0.275 & 0.320 mm**	**0.240 & 0.265 mm**	**0.200 mm**	**0.210 mm**
Recommended Stencil Aperture Size	0.3 x 0.3 mm square, 0.125 mm thick	0.25 x 0.25 mm square, 0.1 mm thick	0.25 x 0.25 mm square, 0.1 mm thick	0.21 x 0.21 mm square, 0.1 mm thick	0.20 x 0.20 mm square, 0.1 mm thick

7 Component Placement

Standard pick-and-place machines can be used for placing the micro DSBGA. Either of the following methods can be used for recognition and positioning.

1. Vision system to locate package silhouette.
2. Vision system to locate individual bumps. It is recommended that side-lighting on the pick and place machine's vision system be used when attempting to use individual bump recognition.

Other features of DSBGA placement:

1. It is preferable to use IC placement/fine pitch placement machines over chip-shooters for better accuracy.
2. DSBGA solder bumps self-align when placed at an offset due to self-centering nature of solder bumps.
3. Though DSBGA can withstand a placement force of up to 1 kg for 0.5 seconds, little or no force needs to be exerted during placement. It is recommended that bumps be immersed into the solder paste on the PCB to greater than 20% of paste block height.

8 Solder Paste Reflow And Cleaning

- DSBGA is compatible with industry standard reflow for both Lead-free and Eutectic processes.
- DSBGA is qualified for up to four reflow operations (260°C peak) per J-STD-020.
- Use of Pb-free DSBGA with eutectic solder paste is not recommended. Such an application can result in assemblies that will not meet desired reliability standards.

9 Rework

The key features for the DSBGA rework are listed below.

1. Rework procedure used is identical to the one used for most BGA and CSP packages.
2. Rework reflow process should duplicate original reflow profile used for SMT assembly.
3. Rework system should include localized convection heating element with profiling capability, a bottom side pre-heater and a part pick and placer with image overlay.
4. A rework demo video is available from Texas Instruments at www.ti.com

10 Qualification

The following sections describe solder joint reliability qualification and mechanical testing results for DSBGA when mounted on FR-4 PCB. Testing included use of daisy chain components. Product reliability data is included in respective product qualification reports.

10.1 Solder Joint Reliability Qualification

1. TEMPERATURE CYCLING: Testing performed per IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments. The results of this testing after following the above mentioned assembly conditions described here are shown in Figure 3, Figure 4, Table 6, Table 7 and Table 9.

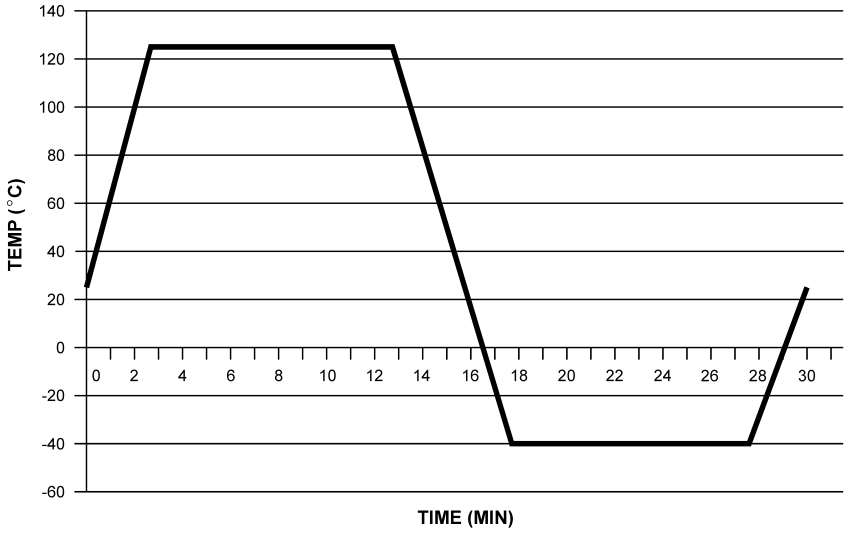


Figure 3. Thermal cycling profile specified for the −40 to 125°C profile with 5 minute ramp and 10 minute hold times.

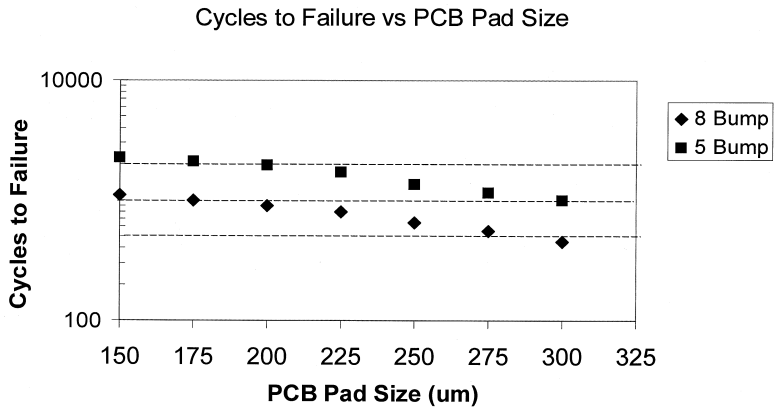


Figure 4. Impact of PCB Pad Size on Reliability for 0.17 mm Bump Package

Table 6. Temperature Cycling of 0.5 mm Pitch DSBGA Devices

DSBGA Assembly	Stencil Type	Test Condition	0 cycles	284 cycles	764 cycles	1056 cycles	1152 cycles	
8 bump 0.17 mm bump diameter	0.100 mm thick 0.250 x 0.300 mm Oval aperture	−40 to 125°C, 1 cycle/hr, 25 min dwell, 5 min transfer	0/32	0/32	0/32	4/32	5/32	
8 bump 0.17 mm bump diameter	0.125 mm thick 0.300 x 0.300 mm Square aperture		0/32	0/32	0/32	0/32	0/32	
DSBGA Assembly	**Stencil Type**	**Test Condition**	**0 cycles**	**300 cycles**	**600 cycles**	**624 cycles**	**924 cycles**	**1224 cycles**
18 bump 0.320 mm bump diameter	0.125 mm thick 0.250 x 0.250 mm Square aperture	−40 to 125°C, 1 cycle/hr, 15 min dwell, 15 min ramp	0/102	0/102	0/102	0/102	0/102	0/102
DSBGA Assembly	**Stencil Type**	**Test Condition**	**0 cycles**	**500 cycles**	**600 cycles**	**700 cycles**	**800 cycles**	
36 bump 0.320 mm bump diameter	0.125 mm thick 0.250 x 0.250 mm Square aperture	−40 to 125°C, 1 cycle/34 min, 14min dwell, 3min ramp	0/79	0/79	0/79	0/79	0/79	

Table 7. Temperature Cycling of 0.4 mm Pitch DSBGA Devices

DSBGA Assembly	Stencil Type	Test Condition	0 cycles	500 cycles	600 cycles	700 cycles	800 cycles
16 bump 0.275 mm bump diameter	0.100 mm thick 0.2 x 0.2 mm Square aperture	−40 to 125°C, 1 cycle/30 min dwell, 10min ramp	0/62	0/62	0/62	0/62	0/62
36 bump 0.265 mm bump diameter	0.100 mm thick 0.2 x 0.2 mm Square aperture	−40 to 125°C, 1 cycle/34 min, 14min dwell, 3min ramp	0/288	0/288	0/288	13/288	25/288
64 bump 0.265mm bump diameter	0.100 mm thick 0.2 x 0.2mm Square aperture	−40 to 125°C, 1 cycle/5min dwell, 10min ramp	0/60	0/60	0/60	0/60	1/60

Table 8. Temperature Cycling of 0.35 mm Pitch DSBGA Devices

DSBGA Assembly	Stencil Type	Test Condition	0 cycles	500 cycles	600 cycles	700 cycles	800 cycles
64 bump 0.200 mm bump diameter	0.100 mm thick 0.21 x 0.21 mm Square aperture	−40 to 125°C, 1 cycle/30 min, 10 min dwell, 5 min ramp	0/64	1/64	7/64	33/64	42/64

Table 9. Temperature Cycling of 0.3 mm Pitch DSBGA Devices

DSBGA Assembly	Stencil Type	Test Condition	0 cycles	500 cycles	600 cycles	700 cycles	800 cycles
36 bump 0.210 mm bump diameter	0.100 mm thick 0.2 x 0.2 mm Square aperture	−40 to 125°C, 1 cycle/30 min, 10 min dwell, 5 min ramp	0/96	0/96	2/96	8/96	22/96

2. PACKAGE SHEAR: As part of the manufacturing process, bump shear data is collected at the package level to ensure attachment of the solder ball to the package.

- 0.5 mm pitch micro SMD
  - 0.320 mm and 0.275 mm diameter solder bump: The package shear strength is greater than 200 gm per solder joint.
  - 0.17 mm diameter solder bump: The package shear strength is greater than 100 gm per solder joint.
- 0.4 mm pitch micro SMD
  - 0.265 mm and 0.240 mm diameter solder bump: The package shear strength is greater than 165 gm per solder joint.

The measured value of package shear may vary depending on materials and methods used in surface mount assembly.

3. PULL TEST: Assembled DSBGA 8 bump units were pulled vertically upward with a stud machined into the back of the component. The component was pulled till it was removed from the PCB. Average stud pull strength was measured at 80 gm per solder joint for 0.17 mm diameter solder bump.

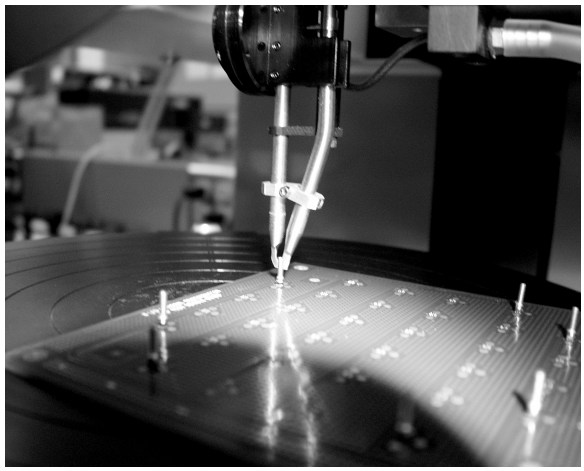


Figure 5. Pull Test Carried Out on the SMD 8 Bump (0.17 mm Diameter Bump)

4. DROP TEST: Drop test results are shown in Figure 6 — Figure 11. Drop test were performed with the following test conditions:

- PCB Thickness: 0.98 mm ± 10%
- Peak Acceleration: 1500 g ±10%
- Pulse Duration: 1 ms ± 10%
- Pulse Shape: Half Sine Wave

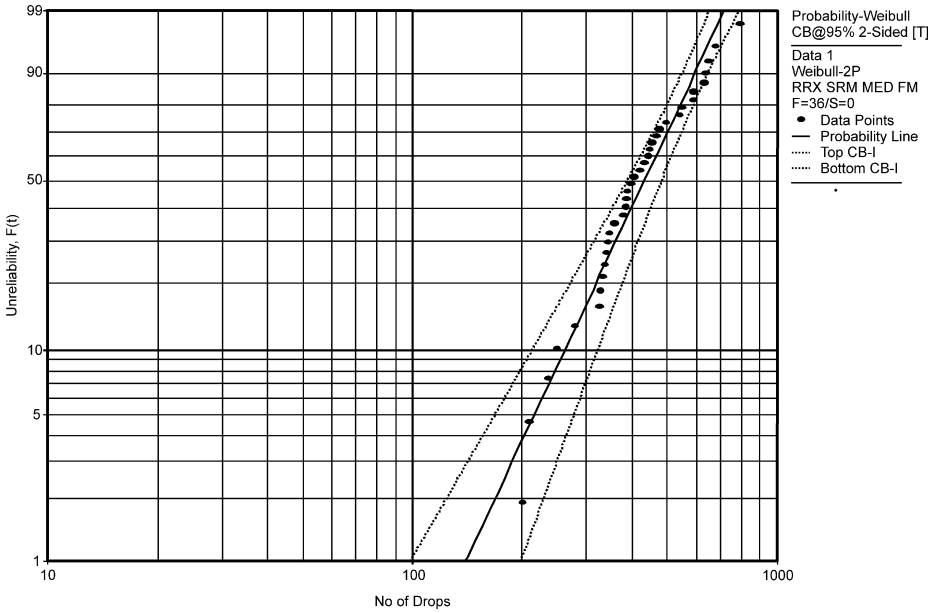


Figure 6. DSBGA 0.5 mm Pitch, 30 Bumps

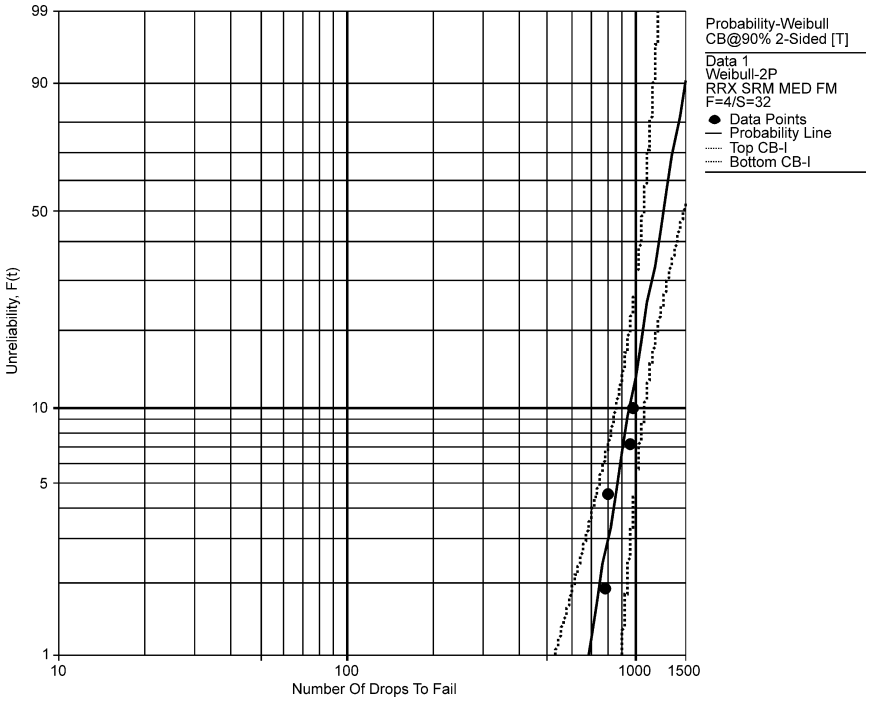


Figure 7. DSBGA 0.5mm Pitch, 16 Bumps, 0.275mm Bump Diameter.

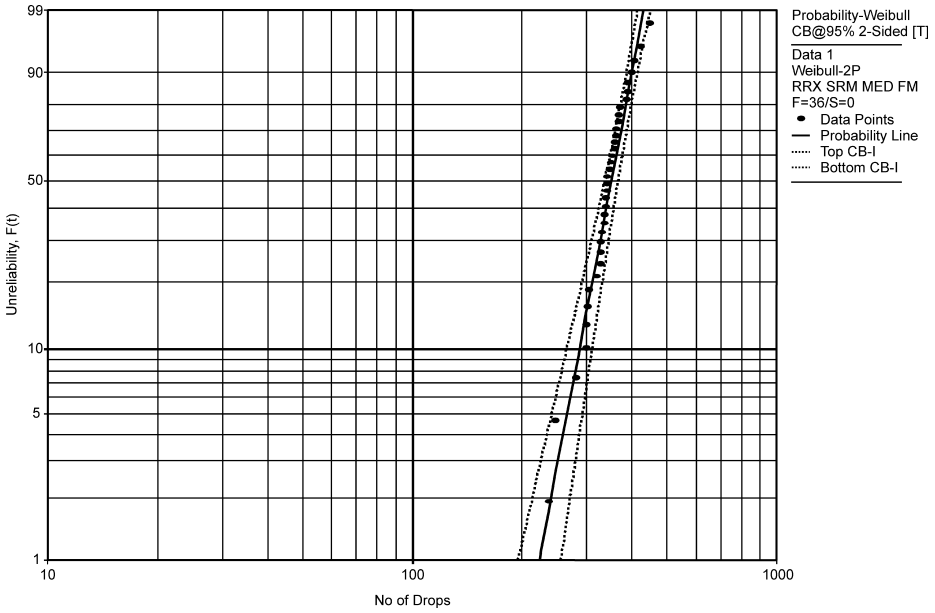


Figure 8. DSBGA 0.4 mm Pitch, 36 Bumps

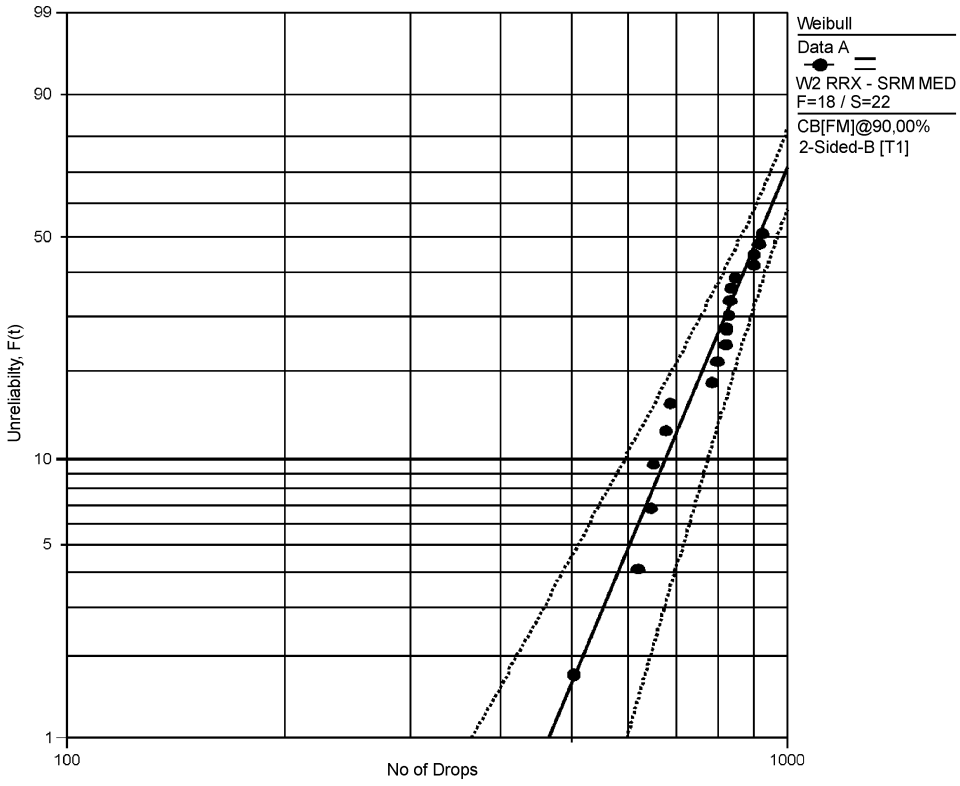


Figure 9. DSBGA 0.4 mm Pitch, 64 Bumps

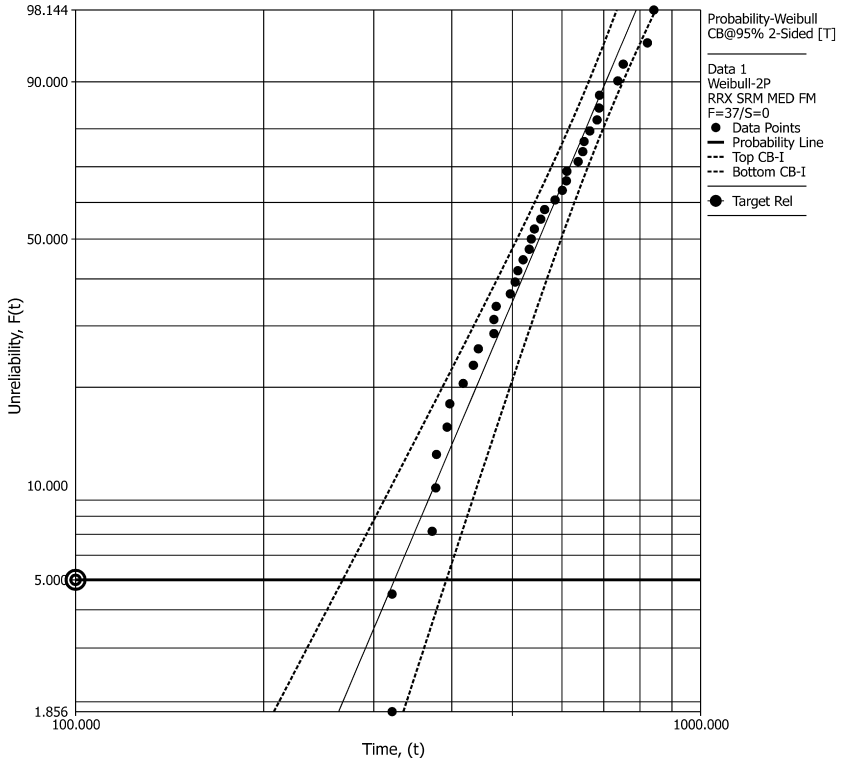


Figure 10. DSBGA 0.35 mm Pitch, 64 Bumps

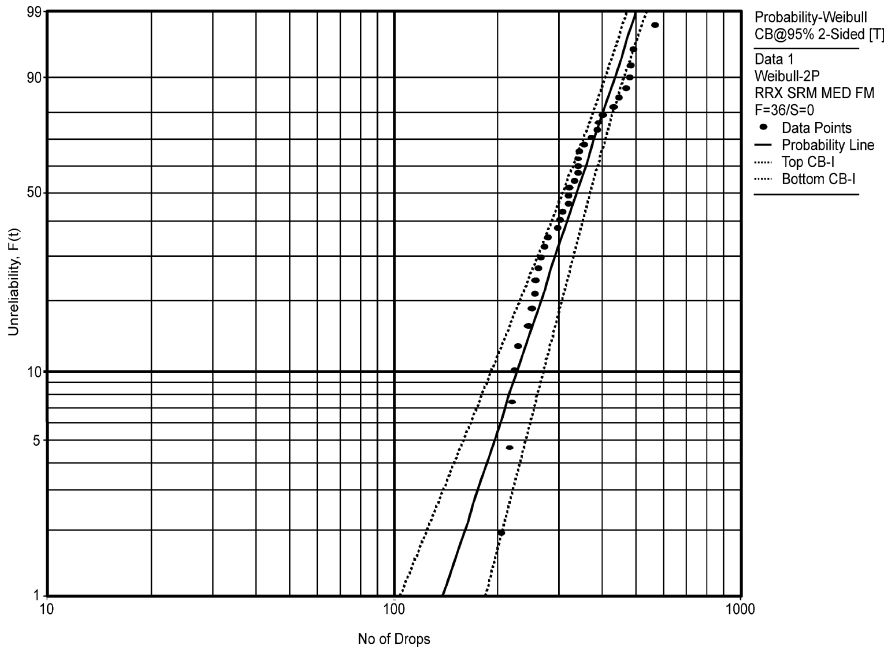


Figure 11. DSBGA 0.3 mm Pitch, 36 Bumps

5. THREE-POINT BEND TEST: The three-point bend test used a test board with a 100 mm span. Deflection was applied at the center at 9.45 mm/min. No solder joint failure was observed even with deflections as high as 25 mm.

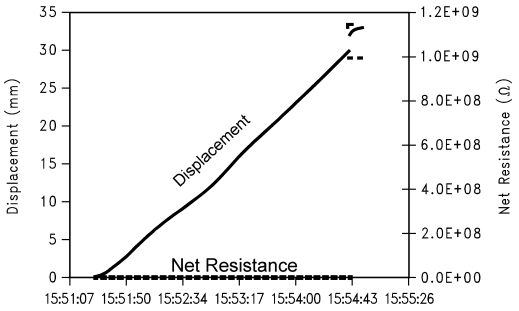


Figure 12. Board Deflection and Net Resistance (0.17 mm Diameter Bump Package)

6. FLEX TEST: This is a repetitive flexing test where PCB is flexed at a pre-set frequency. Flex test results are shown in Table 10. An increase of 10% in resistance of network (daisy chain) is considered a failure. Figure 13 and Figure 14 show the setup used for the Flex test.

7. RECOMMENDATIONS FOR DEVICE PLACEMENT ON PCB: It is recommended that in cases where PCB flexing is likely, the part should be placed as close to the mounting/rivet point as possible. It is also recommended that the device location be away from the area of maximum PCB flexing (deflection).

Table 10. Flex Test Results

Bump Count	Bump Size (micron)	PCB Pad Size (micron)	Cycles to First Fail	Comments
PCB Displacement: 1.0 mm				
8	170	170	7769	
8	170	265	244	Not Recommended
8	320	265	9221	
PCB Displacement: 1.5 mm				
8	170	170	502	
8	170	265	49	Not Recommended
8	320	265	621	
PCB Displacement: 2.0 mm				
8	170	170	129	
8	170	265	26	Not Recommended
8	320	265	534	

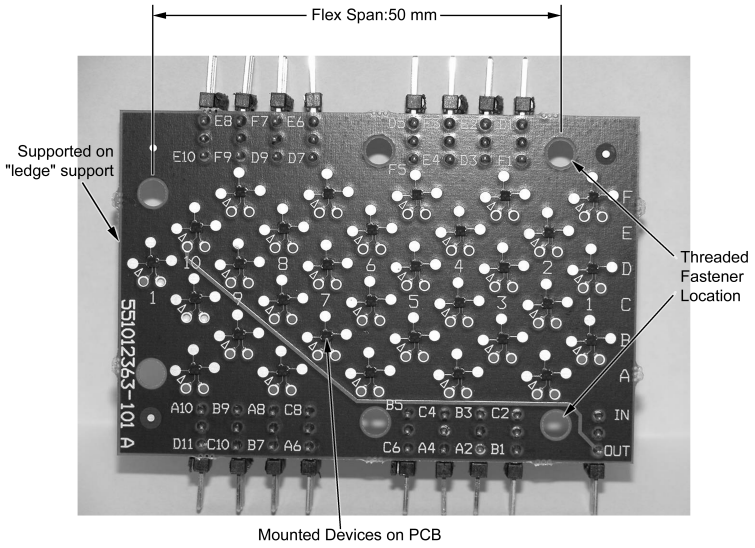


Figure 13. Flex Test PCB Layout

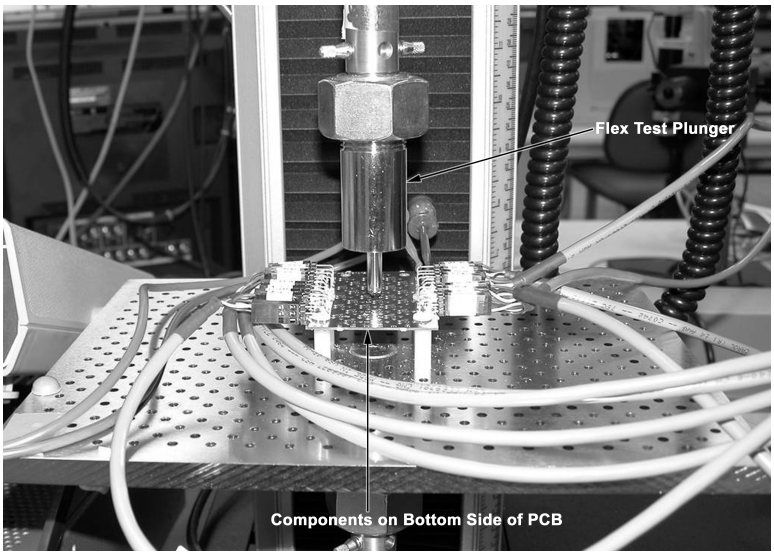


Figure 14. Test Setup for Flexural Testing

11 Thermal Characterization

Thermal performance of DSBGA packages was assessed using low effective thermal conductivity test boards per EIA/JESD51-3. The performance of the DSBGA product depends on product die size and application (PCB layout and design), and the details of Theta JA values are available in product data sheets at www.ti.com.

12 DSBGA Do's and Don'ts (Assuming NSMD pads)

0.5 mm Pitch DSBGA (0.170 mm diameter)		
	DO's	**DON'Ts**
PCB	145 µm < Pad Dia < 185 µm	Pad Dia < 145 µm or Pad Dia > 185 µm
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD). Solder mask opening ≤ 285 µm round.	Solder mask opening > 285 µm round.
	Organic Solderability Preservative (OSP) or Ni-Au surface finish (Less than 0.2 µm Au thickness).	Greater than 0.2 µm Au thickness for Ni-Au surface finish.
		HASL (Hot Air Solder Leveled) board finish.
Stencil	300 x 300 µm square aperture	Less than 275 x 275 µm square aperture
		Greater than 300 x 300 µm square aperture
	Laser cut + electro-polished or Additive build-up	Chemical etch
	100 µm < Thickness < 125 µm	Thickness > 125 µm or < 100 µm
Solder Paste	Type 3 (25 to 45 µm particle size range)	Type 2 or Type 1 (Particle size > 45 µm)
	Match solder paste alloy and assembly process with the component bumps alloy. (e.g. Pb-free paste and process to be used with Pb-free components)	Mix Lead-free DSBGA components with eutectic solder paste or vice versa

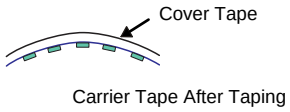
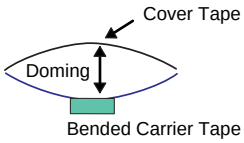
0.5 mm Pitch DSBGA (0.275 mm & 0.320 mm diameter)		
	DO's	**DON'Ts**
PCB	245 µm < Pad Dia < 285 µm	Pad Dia < 245 µm or Pad Dia > 285 µm
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD). Solder mask opening ≤ 375 µm round.	Solder mask opening > 375 µm round.
	Ni-Au surface finish (Less than 0.2 µm Au thickness) or Organic Solderability Preservative (OSP).	Greater than 0.2 µm Au thickness for Ni-Au surface finish.
		HASL (Hot Air Solder Leveled) board finish.
Stencil	Square Aperture	Round Aperture
	250 x 250 µm square aperture	Less than 225 x 225 µm square aperture
		Greater than 250 x 250 µm square aperture
	Laser cut + electro-polished or Additive build-up	Chemical etch
	Thickness ≤ 100 µm	Thickness > 100 µm
Solder Paste	Type 3 (25 to 45 µm particle size range)	Type 2 or Type 1 (Particle size > 45 µm)
	Match solder paste alloy and assembly process with the component bumps alloy. (eg. Pb-free paste and process to be used with Pb-free components)	Mix Lead-free DSBGA components with eutectic solder paste or vice versa

0.4 mm Pitch DSBGA (0.240 mm & 0.265 mm diameter)		
	DO's	**DON'Ts**
PCB	205 µm < Pad Dia < 245 µm	Pad Dia < 205 µm or Pad Dia > 245 µm
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD). Solder mask opening ≤ 325 µm round.	Solder mask opening > 325 µm round.
	Organic Solderability Preservative (OSP) or Ni-Au surface finish (Less than 0.2 µm Au thickness).	Greater than 0.2 µm Au thickness for Ni-Au surface finish.
		HASL (Hot Air Solder Leveled) board finish.

0.4 mm Pitch DSBGA (0.240 mm & 0.265 mm diameter)		
	DO's	**DON'Ts**
Stencil	250 x 250 µm square aperture	Less than 225 x 225 µm square aperture
		Greater than 250 µm x 250 µm square aperture
	Laser cut + electro-polished or Additive build-up	Chemical etch
	Thickness ≤100 µm	Thickness > 100 µm
Solder Paste	Type 3 (25 to 45 µm particle size range)	Type 2 or Type 1 (Particle size > 45 µm)
	Match solder paste alloy and assembly process with the component bumps alloy. (eg. Pb-free paste and process to be used with Pb-free components)	Mix Lead-free DSBGA components with eutectic solder paste or vice versa

0.3 mm Pitch DSBGA (0.210 mm diameter)		
	DO's	**DON'Ts**
PCB	145 µm < Pad Dia < 175 µm	Pad Dia < 145 µm or Pad Dia > 175 µm
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD). Solder mask opening ≤ 225 µm round.	Solder mask opening > 225 µm round.
	Organic Solderability Preservative (OSP) or Ni-Au surface finish (Less than 0.2 µm Au thickness).	Greater than 0.2 µm Au thickness for Ni-Au surface finish.
		HASL (Hot Air Solder Leveled) board finish.
Stencil	200 x 200 µm square aperture	Less than 180 x 180 µm square aperture
		Greater than 200 µm x 200 µm square aperture
	Laser cut + electro-polished or Additive build-up	Chemical etch
	Thickness ≤100 µm	Thickness > 100 µm
Solder Paste	Type 3 (25 to 45 µm particle size range)	Type 2 or Type 1 (Particle size > 45 µm)
	Match solder paste alloy and assembly process with the component bumps alloy. (eg. Pb-free paste and process to be used with Pb-free components)	Mix Lead-free DSBGA components with eutectic solder paste or vice versa

0.35 mm Pitch DSBGA (0.200 mm diameter)		
	DO's	**DON'Ts**
PCB	160 µm < Pad Dia < 200 µm	Pad Dia < 160 µm or Pad Dia > 200 µm
	Prefer non-solder mask defined (NSMD) over solder mask defined (SMD). Solder mask opening ≤ 245 µm round.	Solder mask opening > 245 µm round.
	Organic Solderability Preservative (OSP) or Ni-Au surface finish (Less than 0.2 µm Au thickness).	Greater than 0.2 µm Au thickness for Ni-Au surface finish.
		HASL (Hot Air Solder Leveled) board finish.
Stencil	210 x 210 µm square aperture	Less than 190 x 190 µm square aperture
		Greater than 210 µm x 210 µm square aperture
	Laser cut + electro-polished or Additive build-up	Chemical etch
	Thickness ≤100 µm	Thickness > 100 µm
Solder Paste	Type 3 (25 to 45 µm particle size range)	Type 2 or Type 1 (Particle size > 45 µm)
	Match solder paste alloy and assembly process with the component bumps alloy. (eg. Pb-free paste and process to be used with Pb-free components)	Mix Lead-free DSBGA components with eutectic solder paste or vice versa

0.35 mm Pitch DSBGA (0.200 mm diameter)		
	DO's	**DON'Ts**
Carrier tape/Reel handling	Handling or perform inspection the reel in "cry face" mode  Carrier Tape After Taping	Handling or perform inspection the reel in "smile face" mode  Bended Carrier Tape Bended tape to "Smile face" there is extra space between pocket and cover tape

Mounting Conditions

For surface mount validation, more than 1000 components have been successfully mounted on a PCB without any failure. Mounting conditions are as follows:

- Machine: Fuji CP65 chip shooter
- Pick up nozzle: 0.4 mm diameter
- Speed: 2.4 seconds per placement

DSBGA Bump Site/Assembly Site Code Pin 1 Identification

Table 11. DSBGA Bump Site/Assembly Site Code Pin 1 Identification

Bump Company (Country)	Pin 1 Identification Symbol	
	Assembly Site: TIEM	Assembly Site: SVA
TIEM (Malaysia)		
JCAP (China) and FCI (US)		

Revision History

Revision Date	Description
December 2004	Replaced Table 6. Current Figure 6 was Figure 8. Replaced Figure 7 and Figure 8. Modified Do's and don'ts tables.
August 2005	Added 0.4 mm pitch information.
September 2005	Added “Large Dome Bump” paragraph to the Surface Mount Assembly Considerations section.
August 2006	General review, minor edits.
October 2006	Modify 0.5 mm Pitch (0.3 mm dia) Do's and Don'ts
December 2006	Add a bullet to the Solder Paste Reflow and Cleaning section.
March 2007	Modify Table 1. Recommended PCB Pad Geometry
June 2007	Update Figure 1. Remove 36 bump references. Update Table 5. Replace Figure 3. Update all Do's and Don'ts
December 2007	Add 0.3 mm pitch information
September 2009	Add in 0.4mm pitch 64bumps DSBGA package information
January 2010	Add dome bump, ultra-thin and extreme-thin package information.
September 2011	Added 0.35 mm pitch info to Recommended PCB pad and Recommended Stencil Apertures tables.
April 2012	Added more 0.35 mm pitch information.
May 2012	Insert Appendix A. Modify Appendix B.
March 2015	Removed “Use of underfill is not recommended” from section 1 and 8. Added “The use of an underfill with a CTE matching the solder will enhance the board level performance” to section 1. Added “Refer to Application Report, Forward/Backward Compatibility snoa923 for details” to section 1. Corrected figure 1 from “DSBGA 4-30 Bump” to “DSBGA 4-25 Bump” Updated table 3. Changed “micro SMD” to “DSBGA” in section 4, 7 and 11. Changed “Ni-Gold board finish” to “Electroless Nickel Immersion Gold “
August 2015	• TI DSBGA products are designed and tested to ensure excellent board-level thermal cycling reliability without the need for underfill in intended applications. If a customer chooses to underfill a DSBGA product, TI recommends following the guidelines below to maximize reliability. – The underfill fillet should extend partially up the die edges. Underfill that ends at the bottom (ball side) of the die will degrade reliability. – The underfill should have a CTE closely matched to the CTE of the solder interconnect. – The underfill should have a Tg above the expected maximum exposure temperature.

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