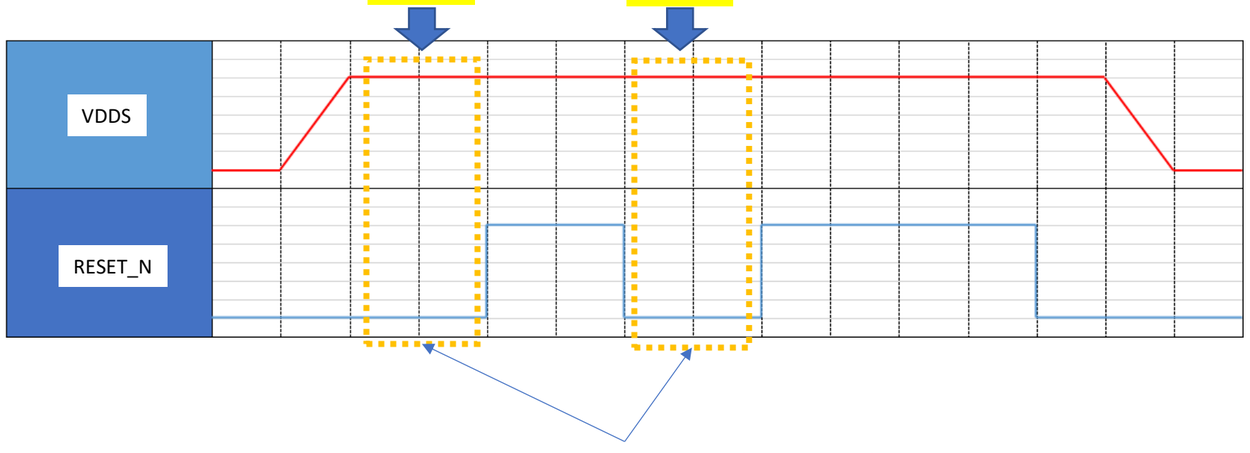
(1) Current at the time of reset (typ)

8.5 Power Consumption - Power Modes

When measured on the CC26x2REM-7ID-Q1 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption				
I_{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	150	nA
		Shutdown. No clocks running, no retention	150	
	Standby without cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	0.94	µA
		RTC running, CPU, 80KB RAM and (partial) register retention XOSC_LF	1.09	µA
	Standby with cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	3.2	µA
		RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF	3.3	µA
	Idle	Supply Systems and RAM powered RCOSC_HF	675	µA
	Active	MCU running CoreMark at 48 MHz RCOSC_HF	3.39	mA

(2) Difference in current at RESET timing



In some samples, Timing A has 0.1 mA more current at low RESET_N than Timing B.
However, in most samples, there is no difference in timing.
What's the difference?

Leakage Current when RESET_N is Low

	Most Samples (518/520 pcs)	Some samples (2/520 pcs)
Timing A	330nA	0.103mA
Timing B	330nA	330nA