Document Type: Schematic Review

Customer Name: Schneider

TI Product No: CC2340R5 5x5

Reviewed By: Jake Pulliam

Date: 2023-02-15

JIRA Ticket: SLWIFIHWAPPS-672

Customer Project Details

- Schematic file received:
  - 3E511197_REV A.PDF
- Layout Files Received:
  - 3E511197_REV A_GRB.ZIP
- BOM and Stack-up included

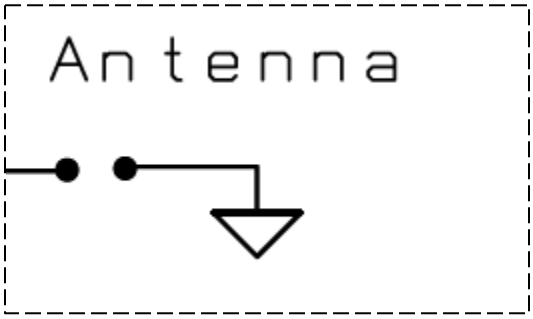
Reference Documents

Document ID	Title	Reference for
SWRS272	CC2340R5 Datasheet	Interconnect / System Design
LP-EM-CC2340R5	Schematic Reference Design	Interconnect / System Design

Schematic Review

- **Decoupling**
  - Decoupling is insufficient as compared to TI reference design. Reference design uses 1 0.1µF per VDDS pin and 1 10µF on pin 31
- **32 kHz Crystal**
  - Verify that system meets requirements when running with the lower accuracy LFOSC (No XTAL). See https://www.ti.com/lit/an/swra499c/swra499c.pdf for ideas on what to consider
- **48 MHz Crystal**
  - According to the BOM description the crystal does not meet the requirements for BLE (+/- 10%?, I'm not even sure that can be correct) or for load capacitance 10pF exceeds the datasheet specification where the maximum is 9pF. Please review and verify specifications are met.

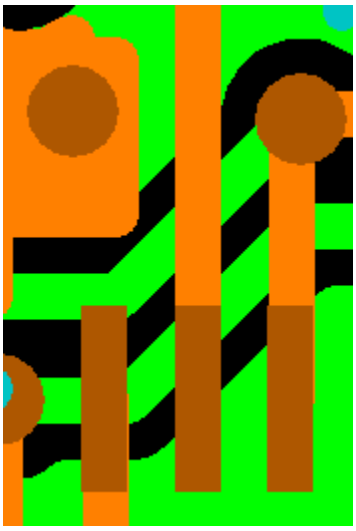
- RF Path
    - D1 is only needed in the case an external connector is used.
    - L5 will be removed from the next revision of the TI reference design, Rev A
    - Do not recommend jumper in RF path as it will affect impedence:



    - If CN3 is used then a DC blocking cap should be included in the path to CN3. In addition C9 should be removed so that both the PCB antenna and external connector for antenna are not in use at the same time.

Layout Review

- Verify RF Path meets 50-ohm characteristic impedance
    - With 1.6mm FR4 Core and 0.2mm trace width my PCB calculator estimates 136-ohm. Typically, we design the RF path as a coplanar waveguide rather than microstrip. See TI reference design for example geometry.
- RF Path must have a reference to ground plane. Breaks in the ground plane change impedance which leads to unwanted reflections and performance degradation:



- Simulate and verify antenna geometry. I'm not sure this would achieve 50-ohm impedance.
- C10, L3, C11 should be placed as close together as possible and as close to pin 1 as possible to reduce PCB parasitic effects on filter