

# **TAS58xxM TDM Configurations (16-ch, 32-bit)**

# Register Setting

## Register 0x33

Table 15. SAP\_CTRL1 Register Field Descriptions

| Bit | Field           | Type | Reset | Description                                                                                                                                                                    |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | I2S_SHIFT_MSB   | R/W  | 0     | I2S Shift MSB                                                                                                                                                                  |
| 6   | RESERVED        | R/W  | 0     | This bit is reserved                                                                                                                                                           |
| 5-4 | DATA_FORMAT     | R/W  | 00    | I2S Data Format<br>These bits control both input and output audio interface formats for DAC operation.<br>00: I2S<br>01: TDM/DSP<br>10: RTJ<br>11: LTJ                         |
| 3-2 | I2S_LRCLK_PULSE | R/W  | 00    | 01: Irclk pulse < 8 SCLK                                                                                                                                                       |
| 1-0 | WORD_LENGTH     | R/W  | 10    | I2S Word Length<br>These bits control both input and output audio interface sample word lengths for DAC operation.<br>00: 16 bits<br>01: 20 bits<br>10: 24 bits<br>11: 32 bits |

## Register 0x34

Table 16. SAP\_CTRL2 Register Field Descriptions

| Bit | Field     | Type | Reset    | Description                                                                                                                                                                                                                                                                                                                                                                           |
|-----|-----------|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7-0 | I2S_SHIFT | R/W  | 00000000 | I2S Shift LSB<br>These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample.<br>00000000: offset = 0 SCLK (no offset)<br>00000001: offset = 1 SCLK<br>00000010: offset = 2 SCLKs<br>and<br>11111111: offset = 512 SCLKs |

# Device Configurations (1 / 2)

## Device 0:

w 98 00 00  
w 98 7f 00  
w 98 33 17 #TDM/DSP, 32-bit  
w 98 34 00 #Channel 0&1

## Device 1:

w 98 00 00  
w 98 7f 00  
w 98 33 17 #TDM/DSP, 32-bit  
w 98 34 40 #Channel 2&3

## Device 2:

w 98 00 00  
w 98 7f 00  
w 98 33 17 #TDM/DSP, 32-bit  
w 98 34 80 #Channel 4&5

## Device 3:

w 98 00 00  
w 98 7f 00  
w 98 33 17 #TDM/DSP, 32-bit  
w 98 34 c0 #Channel 6&7

Note: All the TAS58xxM devices share the same TDM bus.

# Device Configurations (2 / 2)

## Device 4:

w 98 00 00  
w 98 7f 00  
w 98 33 97 #TDM/DSP, 32-bit  
w 98 34 00 #Channel 8&9

## Device 5:

w 98 00 00  
w 98 7f 00  
w 98 33 97 #TDM/DSP, 32-bit  
w 98 34 40 #Channel 10&11

## Device 6:

w 98 00 00  
w 98 7f 00  
w 98 33 97 #TDM/DSP, 32-bit  
w 98 34 80 #Channel 12&13

## Device 7:

w 98 00 00  
w 98 7f 00  
w 98 33 97 #TDM/DSP, 32-bit  
w 98 34 c0 #Channel 14&15

Note: All the TAS58xxM devices share the same TDM bus.