

# TAS2770 I2S External Source

Applications Engineering – Low Power Audio & Actuators

# Default On-Board Audio Source (USB)

- TDM format
  - FSYNC single bit pulse
- 8 channels (slots)
- 32-bit slot length
- 24-bit word length
- FSYNC = 48kHz
- SBCLK =  $32 * 8 * \text{FSYNC} = 12.288\text{MHz}$

# Custom Input Data Requirements (External)

- I2S format
  - FSYNC 50%
- 2 channels
- 16-bit slot length
- 16-bit word length
- FSYNC = 44.1kHz
- SBCLK =  $16 * 2 * \text{FSYNC} = 1.4112\text{MHz}$

# Hardware Setup

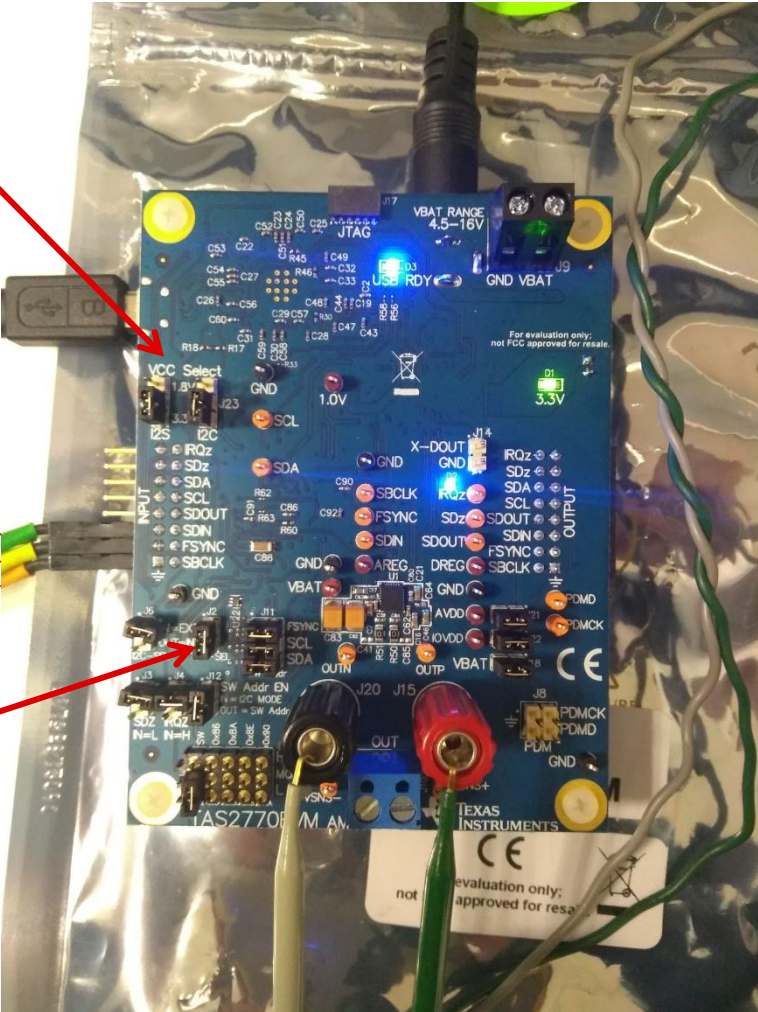
I2S source  
is 3.3V

SDIN

FSYNC

SBCLK

J2 shorted

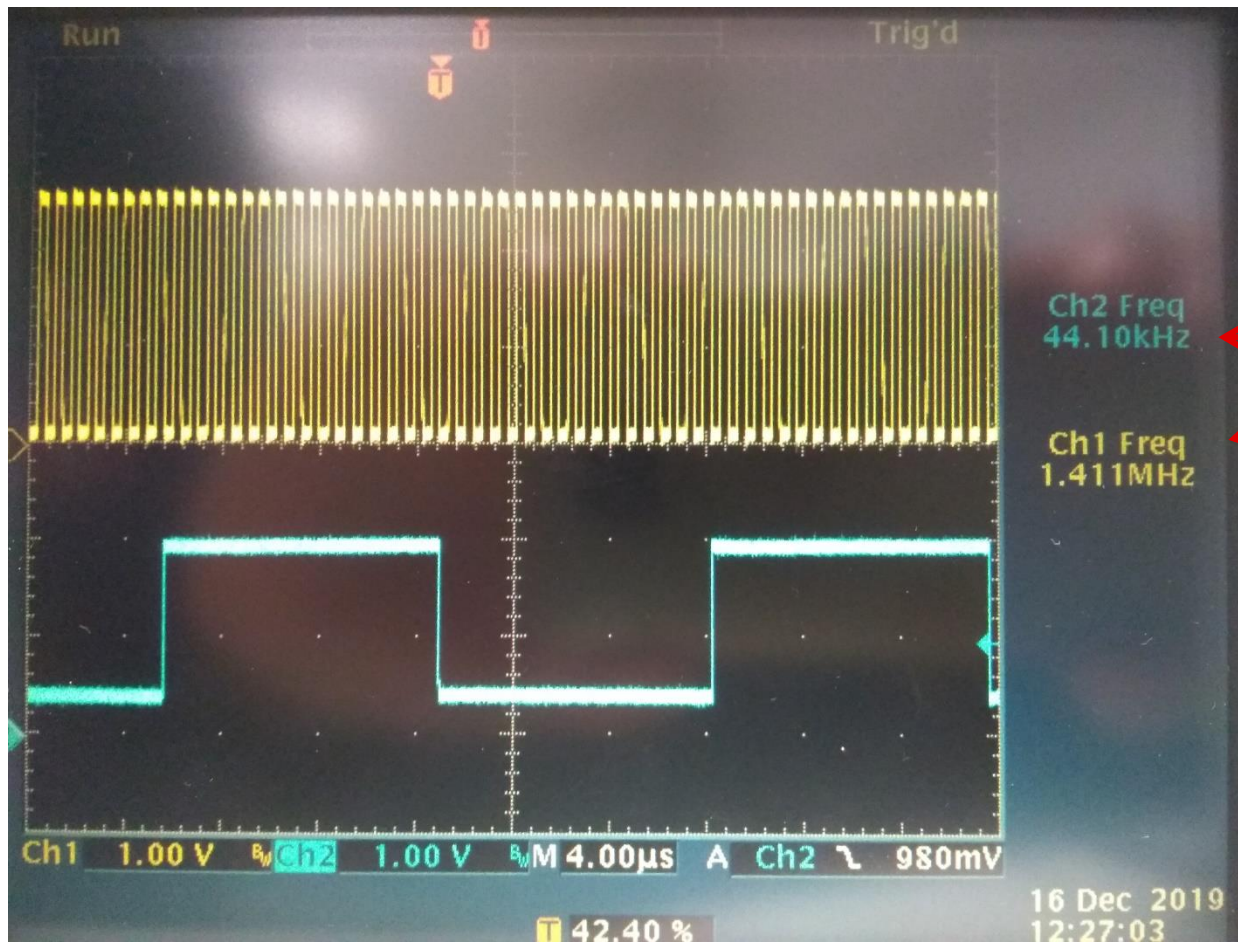


# Audio Source Configuration

The screenshot shows the PSIA Serial Interface Transmitter configuration window. The 'Channel Data Assignment' section has 'I2S' selected in the format dropdown. The 'Channel Data Structure' section shows '16' bits for the word length. The 'Clocks' table is annotated with 'FSYNC' pointing to the Frame Clock (Fs) row, 'SBCLK' pointing to the Slot length (16 bits/channel) row, and 'Number of channels' pointing to the Channel Clock (Subframe Clock) row. The 'Logic Voltage Level' section shows 'TTL' selected for 5V and 3.3V, and 'CMOS' selected for 3.3V, 2.4V, and 1.8V.

Clocks	Direction Out / In	Bit Clock Edge Sync Rise / Fall	Invert Wfm	Shift 1 bit left	Bit Wide Pulse	Setting	Computed Rate
Frame Clock (Fs) (Word Clock)	<input checked="" type="radio"/> <input type="radio"/>	<input type="radio"/> <input checked="" type="radio"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	44.1000 kHz	= 44.1000 kHz
Channel Clock (Subframe Clock)	OUT	<input type="radio"/> <input checked="" type="radio"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	x 2 channels	= 88.2000 kHz
Bit Clock	<input checked="" type="radio"/> <input type="radio"/>	<input type="radio"/> <input type="radio"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	x 16 bits/channel	= 1.41120 MHz
N FPs	OUT	<input type="radio"/> <input type="radio"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	256 x Fs	= 11.2896 MHz
Master Clock	Tx Out, Rx In	<input type="radio"/> <input type="radio"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	x Fs	= 11.2896 MHz

# Audio Source Configuration

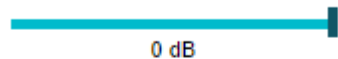


← FSYNC  
← SBCLK

# Device Configuration (Advanced Mode)

## Playback

Volume Control



Volume Ramp Rate

0.5 dB per 1 sample

Amplifier Level



Sample Rate Auto Detect

Sample Rate

44.1/48 kHz

Sample Ramp Rate

44.1 KHz

Playback Source

PCM

PDM

SBCLK / FS Auto Detect

SBCLK / FS Ratio

32

## TDM

Receiver

Transmitter

Edge polarity

Rising edge of SBCLK

Justification

Left

Frame Start Polarity

High to Low on FSYNC

Word Length

16 bits

Slot Length

16 bits

Receiver Offset

1

Left Channel Time Slot

0

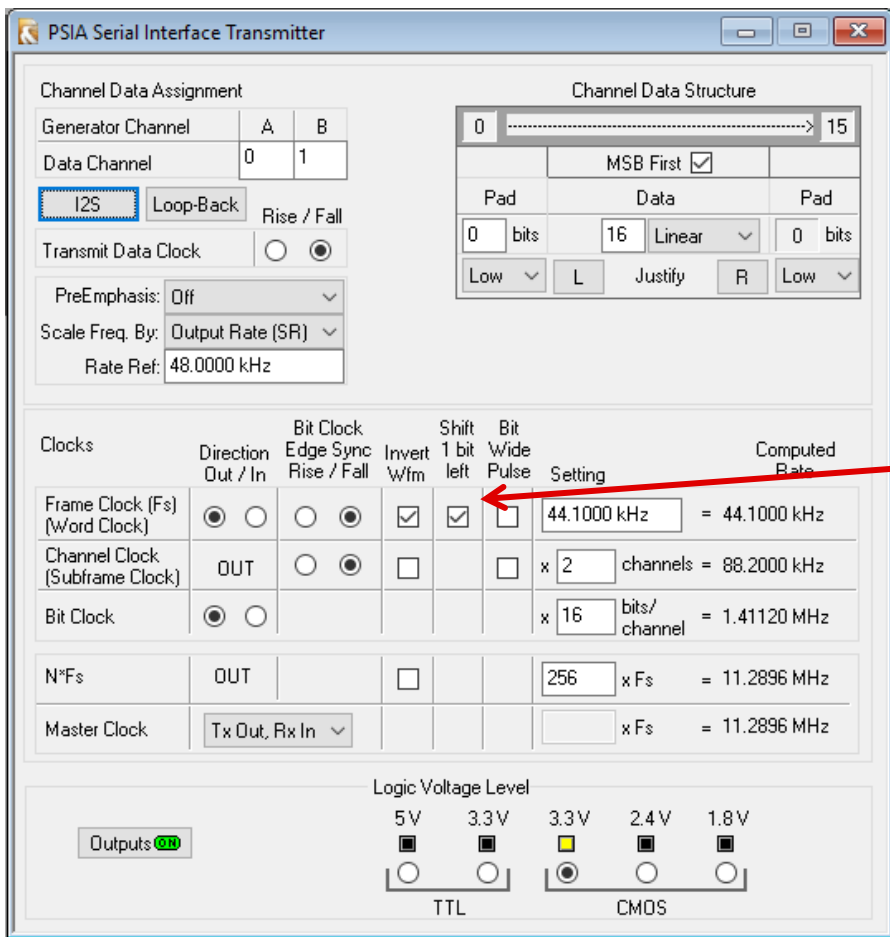
Right Channel Time Slot

1

Slot Select Config

Mono with slot as I2C address

# Special Note



TDM

Receiver

Transmitter

Edge polarity

Rising edge of SBCLK

Justification

Left

Frame Start Polarity

High to Low on FSYNC

Word Length

16 bits

Slot Length

16 bits

Receiver Offset

1

Left Channel Time Slot

0

Right Channel Time Slot

1

Slot Select Config

Mono with slot as I2C address

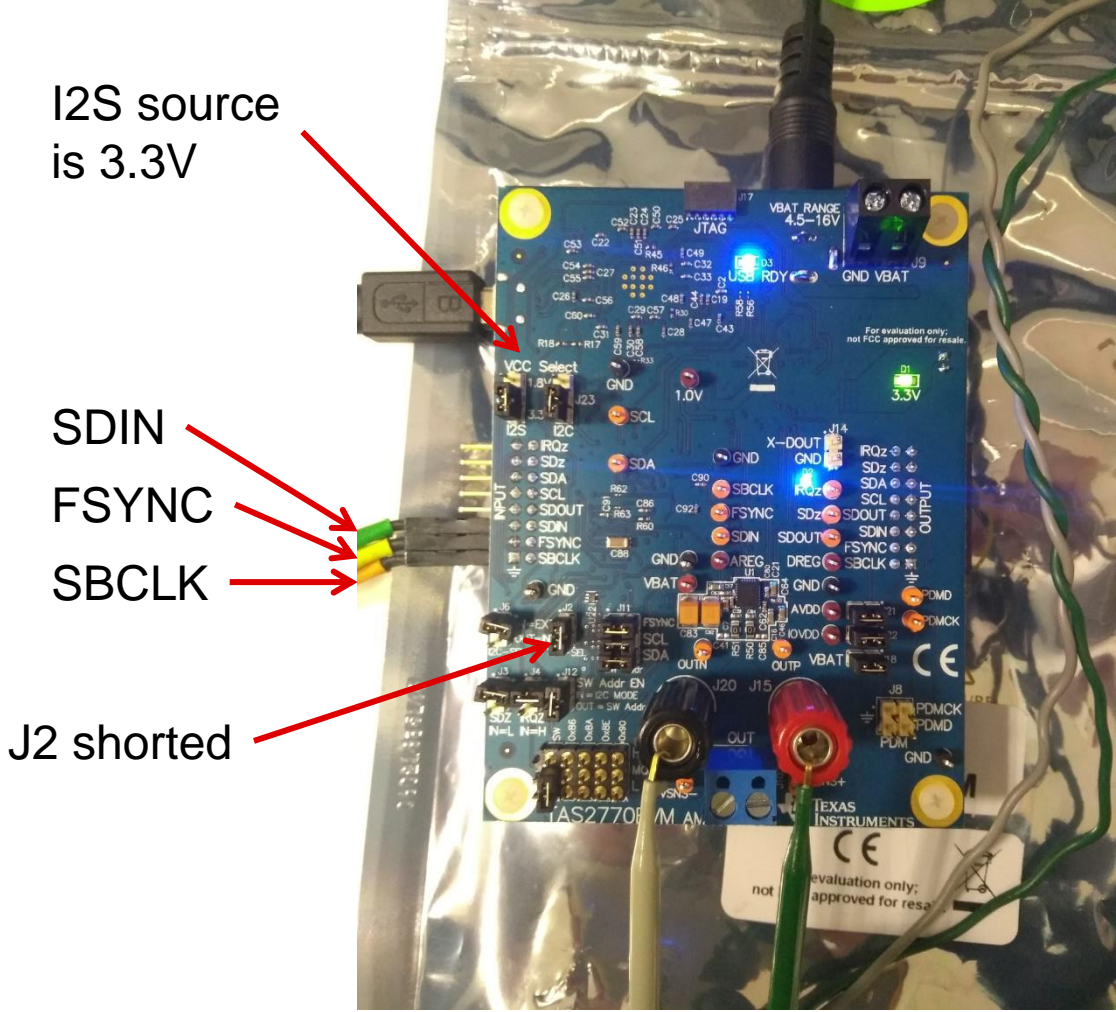
“Shift 1 bit left” is directly related to “Receiver Offset” configuration.  
If “1 bit left” is un-checked, then receiver offset must be 0.



# Custom Input Data Requirements (External)

- I2S format
  - FSYNC 50%
- 2 channels
- 16-bit slot length
- 32-bit word length
- FSYNC = 48kHz
- SBCLK =  $32 * 2 * \text{FSYNC} = 3.072\text{MHz}$

# Hardware Setup



# Audio Source Configuration

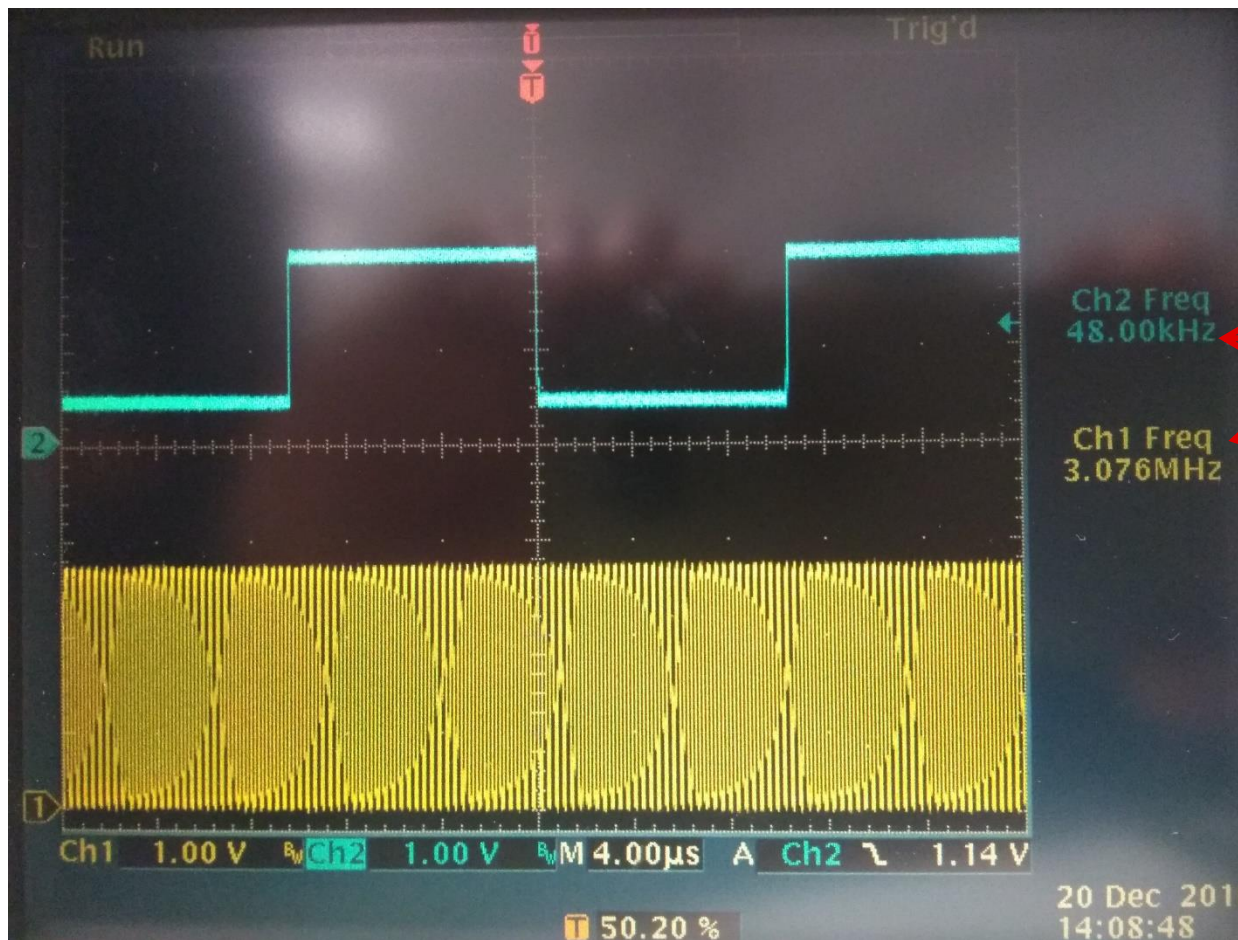
The screenshot shows the configuration window for a PSIA Serial Interface Transmitter. It is divided into several sections:

- Channel Data Assignment:** Includes fields for Generator Channel (A, B), Data Channel (0, 1), and format options (I2S, Loop-Back, Rise / Fall). The I2S format is selected.
- Channel Data Structure:** A diagram showing a 32-bit word structure. It includes fields for Pad, Data (16 bits), and another Pad. The MSB First checkbox is checked. The Data field is annotated with "Word length".
- Clocks Table:** A table with columns for Clocks, Direction, Edge Sync, Invert, Shift, Bit, and Computed Rate. The settings are as follows:

Clocks	Direction	Edge Sync	Invert	Shift	Bit	Computed Rate
Frame Clock (Fs) (Word Clock)	OUT	Sync	Wfm	1 bit left	Wide Pulse	48.0000 kHz = 48.0000 kHz
Channel Clock (Subframe Clock)	OUT	Sync			x 2 channels	= 96.0000 kHz
Bit Clock	OUT				x 32 bits/channel	= 3.07200 MHz
N Fs	OUT				256 x Fs	= 12.2880 MHz
Master Clock	Tx Out, Rx In				x Fs	= 12.2880 MHz

The Frame Clock (Fs) setting is annotated with "FSYNC". The Channel Clock (Subframe Clock) setting is annotated with "SBCLK". The Bit Clock setting is annotated with "Slot length".
- Logic Voltage Level:** Includes radio buttons for 5V, 3.3V, 2.4V, and 1.8V, and checkboxes for TTL and CMOS. The 3.3V CMOS option is selected.

# Audio Source Configuration



Ch2 Freq  
48.00kHz

Ch1 Freq  
3.076MHz

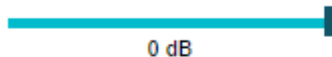
FSYNC

SBCLK

# Device Configuration (Advanced Mode)

## Playback

Volume Control



Volume Ramp Rate

0.5 dB per 1 sample

Amplifier Level



Sample Rate Auto Detect

Sample Rate

44.1/48 kHz

Sample Ramp Rate

48 KHz

Playback Source

PCM

PDM

SBCLK / FS Auto Detect

SBCLK / FS Ratio

64

## TDM

Receiver

Transmitter

Edge polarity

Rising edge of SBCLK

Justification

Left

Frame Start Polarity

High to Low on FSYNC

Word Length

16 bits

Slot Length

32 bits

Receiver Offset

1

Left Channel Time Slot

0

Right Channel Time Slot

1

Slot Select Config

Mono with slot as I2C address