

How to Update BQ Coefficients

Register Page Structure

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Page:	0	1	2-43	44-52	53-61	62-70	71-151	152-186
Func:	Control	Analog Control	Reserved	Coefficient A	Reserved	Coefficient B	Reserved	Instruction
Desc:	General Control and Configuration	Analog Control		256 24-bit coefficients, 30 coefficients per page, 4 registers per coefficient		256 24-bit coefficients, 30 coefficients per page, 4 registers per coefficient		1024 24-bit instructions, 30 instructions per page, 4 registers per instruction

Coefficient Buffer-A Map

Coeff NO	Page NO	Base Register	Base Register+0	Base Register+1	Base Register+2	Base Register+3
C0	62	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	62	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C29	62	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	63	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C59	63	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	64	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C89	64	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	65	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C119	65	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	66	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C149	66	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	67	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C179	67	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	68	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C209	68	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	69	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C239	69	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	70	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C255	70	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Coefficient Buffer-B Map

Coeff NO	Page NO	Base Register	Base Register+0	Base Register+1	Base Register+2	Base Register+3
C0	62	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	62	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C29	62	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	63	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C59	63	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	64	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C89	64	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	65	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C119	65	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	66	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C149	66	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	67	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C179	67	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	68	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C209	68	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	69	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C239	69	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	70	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
..
C255	70	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

How to Determine Coefficient Locations

The screenshot displays the PurePath™ Console -TAS5766M interface. The main window shows the Equalizer settings, including a Gain plot, Phase plot, and Group Delay plot. The I2C Monitor window is open, showing a list of I2C commands. Red boxes and numbers 1, 2, and 3 highlight the I2C icon, the circular button in the I2C Monitor, and the 'On' button for the SmartEq EQ, respectively.

1 Click the "I2C" icon.

2 Click the circular button in the I2C Monitor.

3 Enable one EQ and then all the i2c commands will show in the I2C Monitor.

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2. Click the circular button in the I2C Monitor.
3. Enable one EQ and then all the i2c commands will show in the I2C Monitor.

How to Interpolate the I2C Commands (Part I)

#Ignore those below

w 98 00 00

r 98 76 01

w 98 00 00

r 98 76 01

w 98 00 00

r 98 76 01

#Page = 49 (0x31)

w 98 00 31

#Update biquad coefficients

#0xc8 = 0x80 + 0x48; The actual register address is 0x48.

#The MSB (0x80) is set for multiple writes.

#Refer to the device data sheet for more information.

w 98 c8 7f ff ff 00 88 e4 09 00 70 46 2a 00 77 1b f7 00 8f b9 d6 00

How to Interpolate the I2C Commands (Part 2)

```
#Page = 51 (0x33)
```

```
w 98 00 33
```

```
#Update preGain
```

```
w 98 d0 20 00 00 00
```

```
#Page = 44 (0x2c)
```

```
w 98 00 2c
```

```
#Update volume
```

```
w 98 88 14 49 60 00
```

```
#Page = 44 (0x2c)
```

```
w 98 00 2c
```

```
#Request a buffer switch
```

```
#Refer to this app note below for more details
```

```
#www.ti.com/lit/an/slaa425d/slaa425d.pdf
```

```
w 98 01 05
```

How to Interpolate the I2C Commands (Part 3)

#Update biquad coefficients

w 98 c8 7f ff ff 00 88 e4 09 00 70 46 2a 00 77 1b f7 00 8f b9 d6 00

#Page = 51 (0x33)

w 98 00 33

#Update preGain

w 98 d0 20 00 00 00

#Page = 44 (0x2c)

w 98 00 2c

#Update volume

w 98 88 14 49 60 00

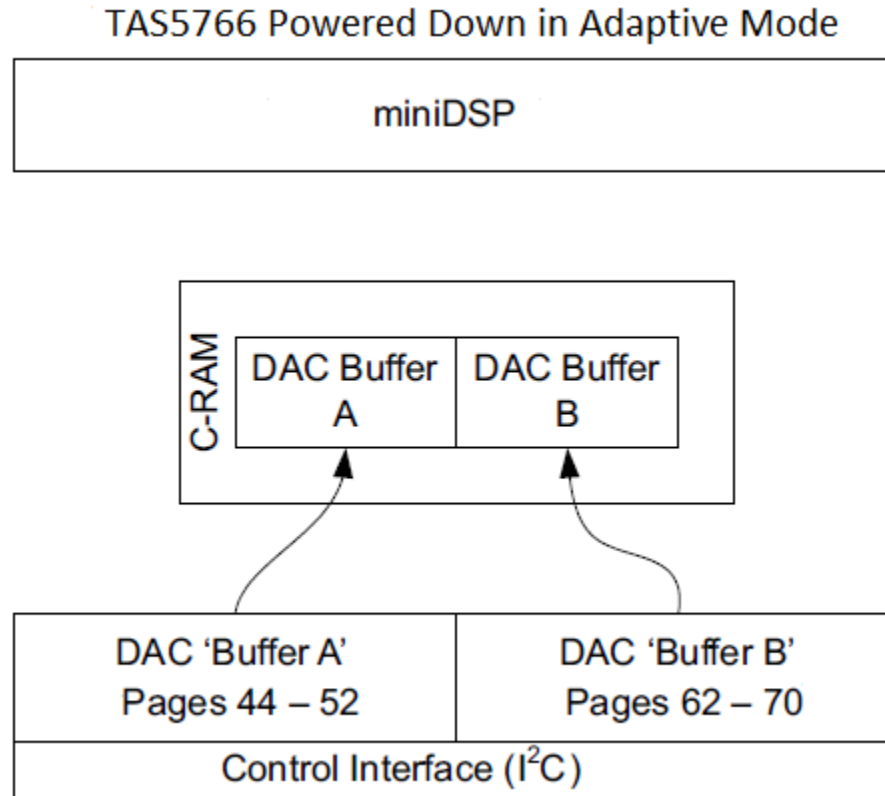
C-RAM Access

C-RAM Access Table – Adaptive

Status	miniDSP C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes (Buffer A and Buffer B)
Powered Up (p44_r1_b1 = 0)	Buffer A only	Buffer B only
Powered Up (p44_r1_b1 = 1)	Buffer B only	Buffer A only

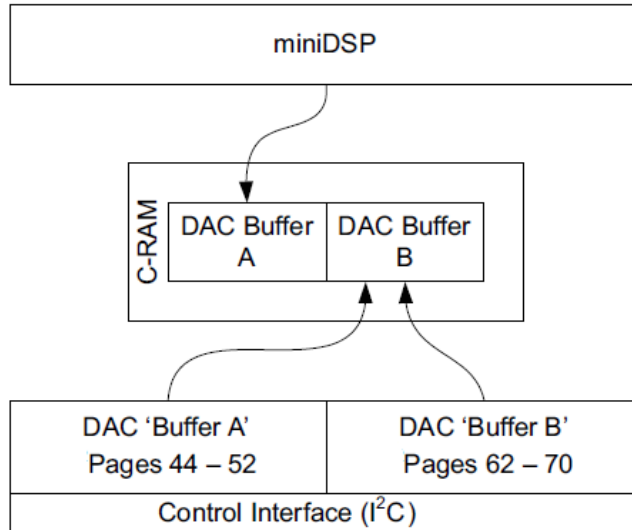
p44_r1_b1 is short for Page 44 / Register 1, Bit 1

C-RAM Access at Power-Down Mode

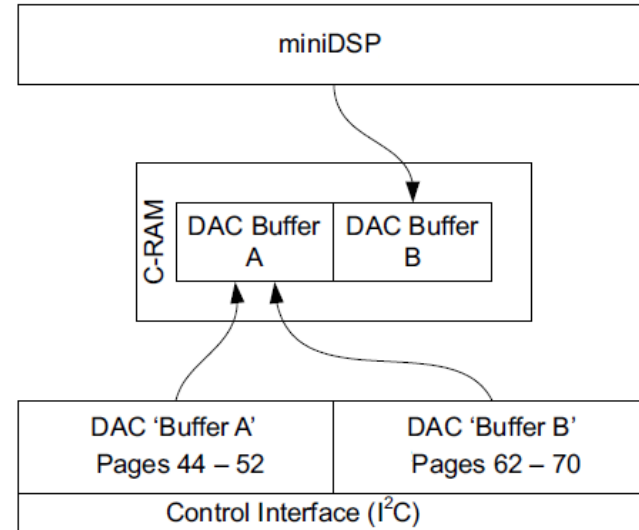


C-RAM Access at Power-Up Mode

TAS5766 Powered Up in Adaptive Mode (p44_r1_b1 = 0)



TAS5766 Powered Up in Adaptive Mode (p44_r1_b1 = 1)



Page 44 / Register 1 (Hex 0x01)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	b0
1	0x01	RSV	RSV	RSV	RSV	ACRM	AMDC	ACRS	ACSW
Reset Value							0		0

ACRS	<p>Active CRAM Selection (Read Only)</p> <p>This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can be accessed by serial interface (SPI/I2C)</p> <p>0: CRAM A is active and being used by the DSP 1: CRAM B is active and being used by the DSP</p>
ACSW	<p>Switch Active CRAM</p> <p>This bit is used to request switching roles of the two buffers, i.e. switching the active buffer role between CRAM A and CRAM B. This bit is cleared automatically when the switching process is completed.</p> <p>Default value: 0 0: No switching requested or switching completed 1: Switching is being requested</p>

C-RAM Access (Adaptive Mode) Example



Header File Structure

Content	Size (%)	Comment
Page 0	0.5	Reset TAS5766 and put it into power-down and then standby mode
Page 44 - 52	23	Coefficient A (C-RAM)
Page 62 - 70	23	Coefficient B (C-RAM)
Page 152 - 186	47	Instruction (I-RAM)
Page 0 -1	6	General control and analog control
Page 0	0.5	Enable adaptive mode and wake up the device

BQ Coefficient Update Procedure

Step 1: Update BQ coefficients.

Step 2: Update preGain.

Step 3: Request a buffer switch.

Step 4: Update BQ coefficients.

Step 5: Update preGain.

Assumptions:

a) The digital gain in the PPC3 GUI is set to less than 6dB.

preGain and Volume

Coefficient Buffer A							
Register	Page No	Page No (hex)	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
preGain	51	33	80	Coef [23:16]	Coef [15:8]	Coef [7:0]	Reserved
Volume	44	2c	8	Coef [23:16]	Coef [15:8]	Coef [7:0]	Reserved
Coefficient Buffer B							
Register	Page No	Page No (hex)	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
preGain	69	45	80	Coef [23:16]	Coef [15:8]	Coef [7:0]	Reserved
Volume	62	3e	8	Coef [23:16]	Coef [15:8]	Coef [7:0]	Reserved

```
{ 0x50, 0x37 }, //preGain { 0x50, 0x37 }, //preGain
{ 0x51, 0x2a }, //Page 51 { 0x51, 0x2a }, //Page 69
{ 0x52, 0x3b }, { 0x52, 0x3b },
{ 0x53, 0x00 }, { 0x53, 0x00 },
```

```
// Page 44 (0x2C) Dump
```

```
{ 0x00, 0x2c },
{ 0x08, 0x80 }, //Volume
{ 0x09, 0x00 },
{ 0x0a, 0x00 },
{ 0x0b, 0x00 },
```

```
// Page 62 (0x3E) Dump
```

```
{ 0x00, 0x3e },
{ 0x08, 0x80 }, //Volume
{ 0x09, 0x00 },
{ 0x0a, 0x00 },
{ 0x0b, 0x00 },
```