TAS5805/25 Register Map Introduction

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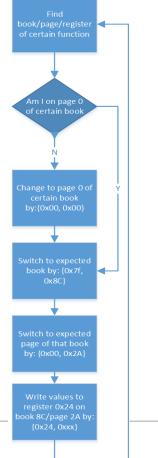
Register Structure

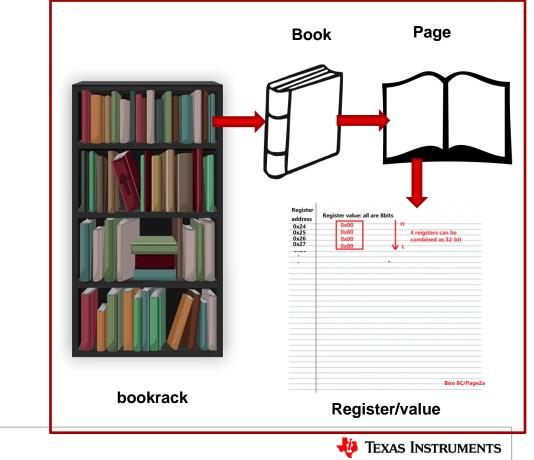


2

TAS58x5m: Register structure Overview

- □ How to configure certain registers
 - Eg. book 8c, page 2a, register 24 as an example
- How to switch book/page?
 See next page;





TAS58x5m: Register structure Overview

Overview

- Non-DSP (in book 0/ page 0)
- DSP (in other book/page)

□ TAS5825 register structure:

- 1. Book 0
 - Page 0
 - Page 1
- 2. Book 8C
 - Page 0x00
 - Page 0x01
- 3. Book 78
 - Page 0x00
 - Page 0x01
- 4. Book AA
 - Page 0x00
 - Page 0x01

Note: See Maps of TAS5825's datasheet

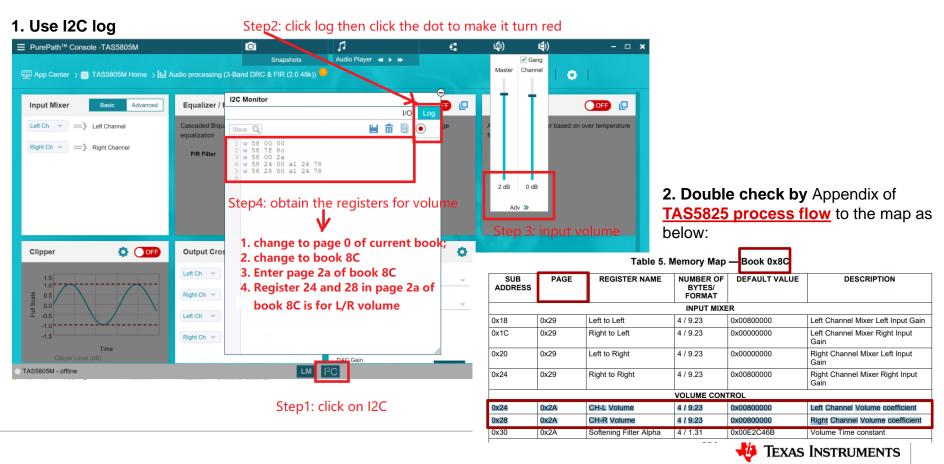
Note: See **Appendix** of <u>TAS5825 process flow</u> to the map <u>TAS5805 Process Flow:</u>

Register operation:

- Change Book (0x7f is the specified flag of book) {0x00, 0x00} // must change to page 0 of current book {0x7f, 0xaa} // Then change to book aa {0x00, 0x24} // go to book aa/ page 24. If no operation, its default page is 0x00;
- 2. Change page (0x00 is the specified flag of book) {0x00, 0x24} // change to page 24
- 3. Change address <u>under certain book/page</u> {0x00, 0x00} {0x00, 0xaa} {0x00, 0x24} //page 24 {0x7f, 0x24} //change value of register 0x7f to 0x24



Example to find registers for volume



How to understand dumped .h file

[] cfg reg registers[] = { $\{0x00, 0x00\}, //change to page 0$ $\{0x7f, 0x00\}, //change to book 0$ { 0x03, 0x02 }, //all lines start from here { 0x01, 0x11 }, //are in book 0/ page 0 before the switch { 0x00, 0x00 }, 61 Note: See Maps of TAS5825's 62 { 0x7f, 0x00 }, 63 { 0x03, 0x02 }, datasheet and they are in book 64 { CFG META DELAY, 5 }, 65 $\{ 0x00, 0x00 \},\$ 0/page 0 always 66 $\{ 0x00, 0x00 \},$ $\{ 0x00, 0x00 \},\$ 67 $\{ 0x00, 0x00 \},$ { 0x00, 0x00 }, { 0x7f, 0x00 }, { 0x03, 0x12 }, { 0x00, 0x00 }, Note: See Appendix of TAS5825 $\{0x00, 0x00\},\$ process flow to the map 74 { 0x00, 0x00 }, { 0x00, 0x00 }, { 0x00, 0x00 }, { 0x7f, 0x00 }, { 0x48, 0x0c }, { 0x00, 0x00 }, // change to page 0 $\{0x7f, 0x64\}, // cange to book 64$ $\{0x00, 0x01\}, // change to page 1 of book 64$ { 0x08, 0x00 }, // all lines start from here { 0x09, 0xfe }, //are in book 64/ page 1 before the switch 8/ 1 0x02 0x00 1

TEXAS INSTRUMENTS

TAS5825M SLASEH7D – MARCH 2018 – REVISED DECEMBER 2018

9.6 Register Maps

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9.6.1 CONTROL PORT Registers

Table 5 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Register 1	Go
2h	DEVICE_CTRL_1	Register 2	Go
3h	DEVICE_CTRL2	Register 3	Go
Fh	I2C_PAGE_AUTO_INC	Register 15	Go
28h	SIG_CH_CTRL	Register 40	Go
29h	CLOCK_DET_CTRL	Register 41	Go
30h	SDOUT_SEL	Register 48	Go
31h	I2S_CTRL	Register 49	Go
33h	SAP_CTRL1	Register 51	Go
34h	SAP_CTRL2	Register 52	Go
37h	FS_MON	Register 55	Go
38h	BCK (SCLK)_MON	Register 56	Go
39h	CLKDET STATUS	Register 57	Go

TEXAS INSTRUMENTS

Appendix A SLAA786A-February 2018-Revised July 2018

Memory Maps

A.1 DSP Memory Map for Process Flow 1

Table 9. DSP Memory Map for Process Flow 1

BasePro(2.0 96k) Mode Memory Map — Book 0x78								
SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES/ FORMAT	DEFAULT VALUE	DESCRIPTION			
0x48	0x01	Level Meter Left Output	4/1.31	0x000000	Level Meter Left Output flag			
0x7C	0x01	Level Meter Right Output	4 / 1.31	0x000000	Level Meter Right Output flag			
		BasePro(2.0 96k) Mode Me	mory Map - Book 0	x8C				
SUB ADDRESS	PAGE	REGISTER NAME	NUMBER OF BYTES/ FORMAT	DEFAULT VALUE	DESCRIPTION			
		VOLUME AL	PHA FILTER					
0x2C	0x01	Softening Filter Alpha	4 / 1.31	0x00E2C46B	Volume Time constant			
		DR	C					
0x58	0x06	DRC 1 Mixer Gain	4 / 9.23	0x00800000	DRC 1 Mixer Gain coefficient			
0x5C	0x06	DRC 2 Mixer Gain	4/9.23	0x0000000	DRC 2 Mixer Gair coefficient			
0x60	0x06	DRC 3 Mixer Gain	4/9.23	0x00000000	DRC 3 Mixer Gain coefficient			
0x64	0x06	DRC1 Energy	4 / 1.31	0x7FFFFFFF	DRC1 Energy Time constant			
0x68	0x06	DRC1 Attack	4 / 1.31	0x7FFFFFFF	DRC1 Attack Time constant			
0x6C	0x06	DRC1 Decay	4 / 1.31	0x7FFFFFFF	DRC1 Decay Time constant			
0x70	0x06	K0_1	4/9.23	0x00000000	DRC1 Region 1 Slope (comp/Exp)			
0.71	0.00	374 3	410.00	0.00000000	DOOL DUNING D			

6

INTS

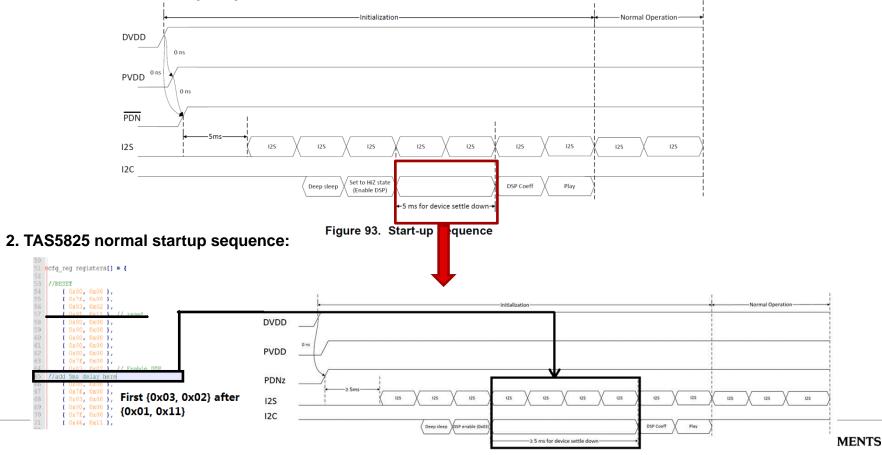
Power on Sequence



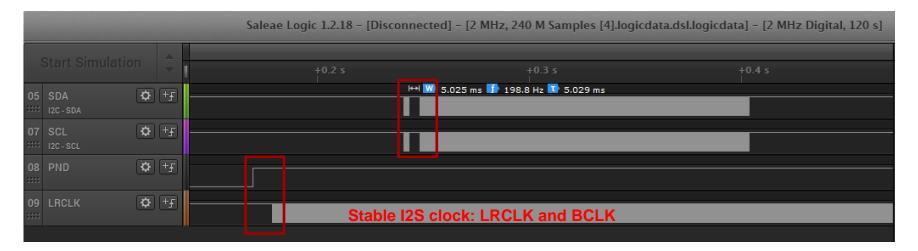
7

TAS5825 Power on sequence

1. TAS5825 normal startup sequence:



Power on sequence Implementation



As can be seen above:

- 1. I2S comes out after 5ms delay after PDN is pulled high (not a must)
- 2. I2S clocks are needed to be stable before I2C commands (must);
- 3. 5ms for device settle down is required in during writing I2C commands(must);

