Serial Ports

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, unless otherwise noted. BCLK in Table 8 refers to BCLK_OUT3 to BCLK_OUT0 and BCLK_IN3 to BCLK_IN0. LRCLK refers to LRCLK_OUT3 to LRCLK_OUT0 and LRCLK_IN3 to LRCLK_IN0.

Table 8.

Parameter	Min	Typ	Max	Unit	Description
f_{LRCLK}			192	kHz	LRCLK frequency
t_{LRCLK}	5.21			µs	LRCLK period
f_{BCLK}			24.576	MHz	BCLK frequency, sample rate ranging from 6 kHz to 192 kHz
t_{BCLK}	40.7			ns	BCLK period
t_{BIL}	10			ns	BCLK low pulse width, slave mode; BCLK frequency = 24.576 MHz; BCLK period = 40.6 ns
t_{BIH}	14.5			ns	BCLK high pulse width, slave mode; BCLK frequency = 24.576 MHz; BCLK period = 40.6 ns
t_{LIS}	20			ns	LRCLK setup to BCLK_INx input rising edge, slave mode; LRCLK frequency = 192 kHz
t_{LIH}	5			ns	LRCLK hold from BCLK_INx input rising edge, slave mode; LRCLK frequency = 192 kHz
t_{SIS}	5			ns	SDATA_INx setup to BCLK_INx input rising edge
t_{SIH}	5			ns	SDATA_INx hold from BCLK_INx input rising edge
t_{TS}			10	ns	BCLK_OUTx output falling edge to LRCLK_OUTx output timing skew, slave mode
t_{SODS}			35	ns	SDATA_OUTx delay in slave mode from BCLK_OUTx output falling edge; serial outputs function in slave mode at all valid sample rates, provided that the external circuit design provides sufficient electrical signal integrity
t_{SODM}			10	ns	SDATA_OUTx delay in master mode from BCLK_OUTx output falling edge
t_{TM}			5	ns	BCLK falling edge to LRCLK timing skew, master mode

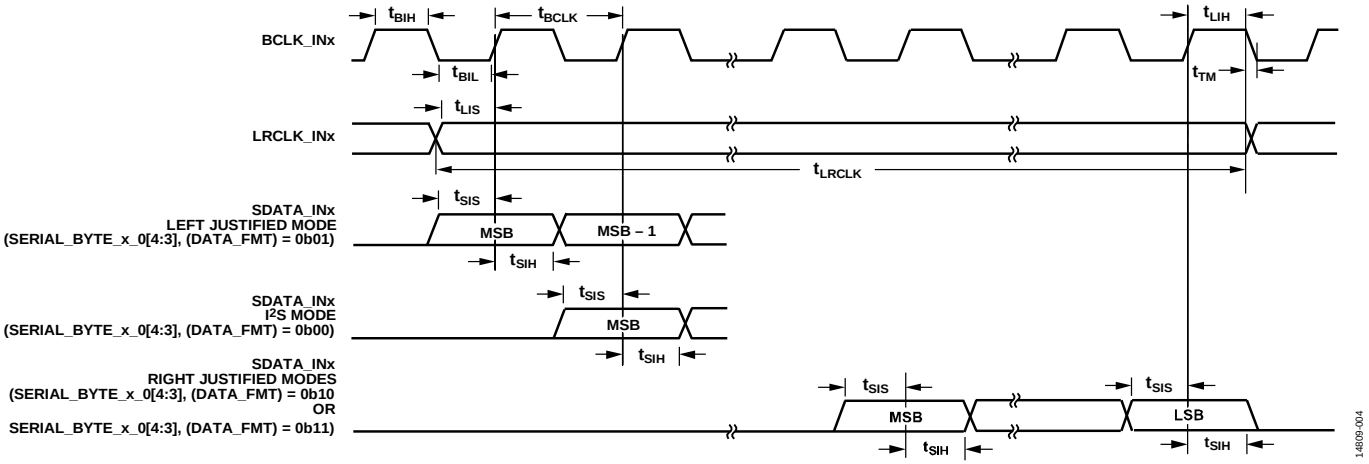

Figure 4. Serial Input Port Timing Specifications

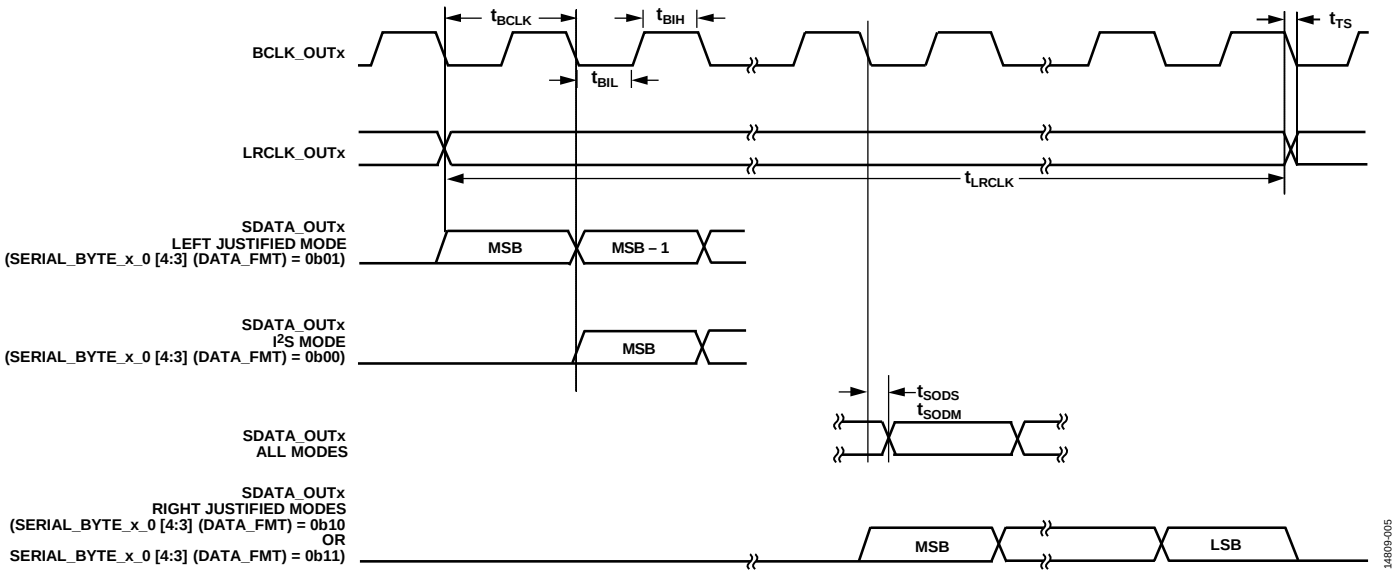

Figure 5. Serial Output Port Timing Specifications

Multipurpose Pins (MPx)

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 9.

Parameter	Min	Typ	Max	Unit	Description
f_{MP}			24.576	MHz	MPx maximum switching rate when pin is configured as a general-purpose input or general-purpose output
t_{MPIL}	10 × t_{CORE}		6144 × t_{CORE}	sec	MPx pin input latency until high/low value is read by core; the duration in the Max column is equal to the period of one audio sample when the DSP is processing 6144 instructions per sample

S/PDIF Transmitter and Receiver

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 10.

Parameter	Min	Typ	Max	Unit	Description
AUDIO SAMPLE RATE					
Transmitter	18		192	kHz	Audio sample rate of data output from S/PDIF transmitter
Receiver	18		192	kHz	Audio sample rate of data input to S/PDIF receiver