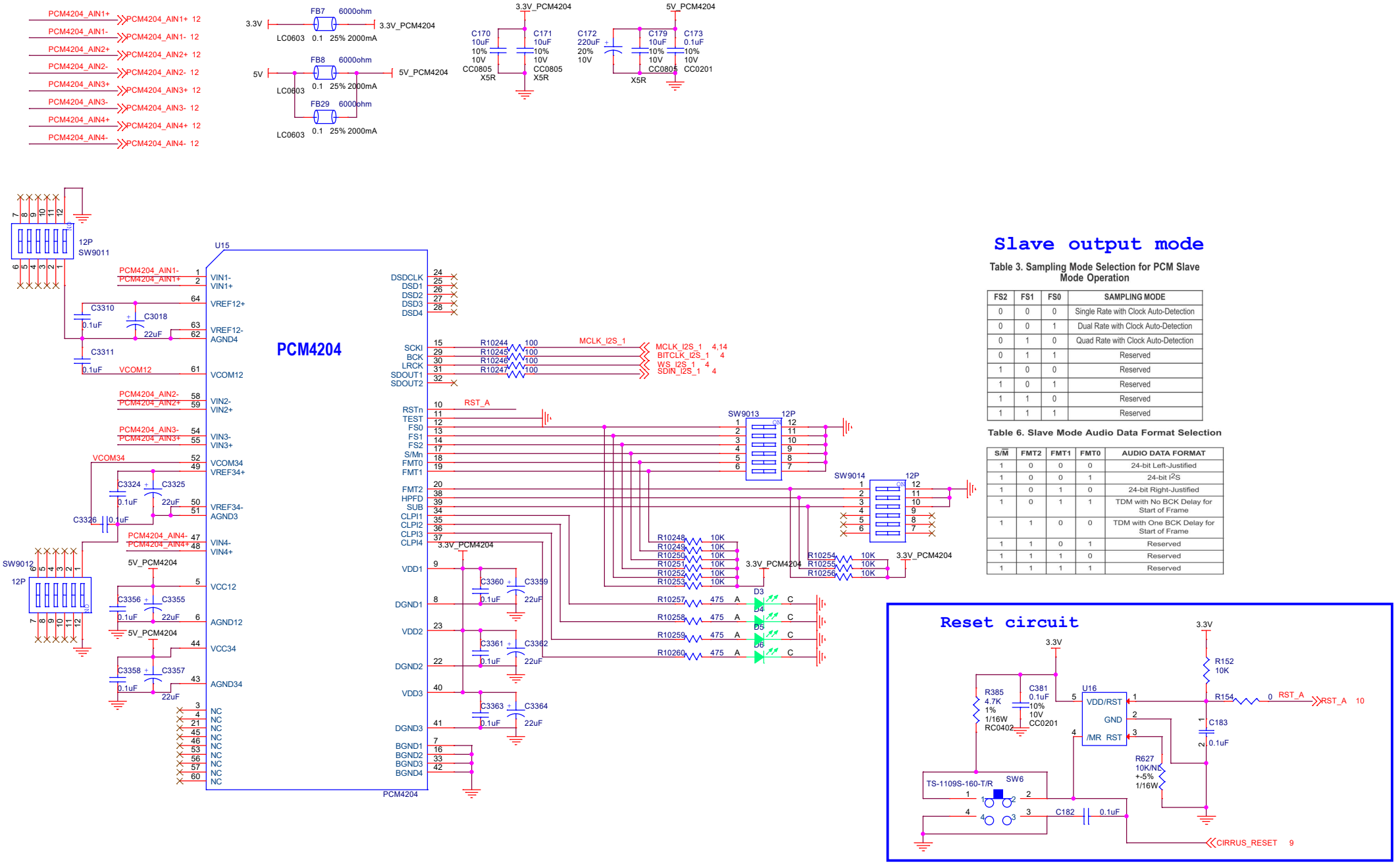


Slave output mode

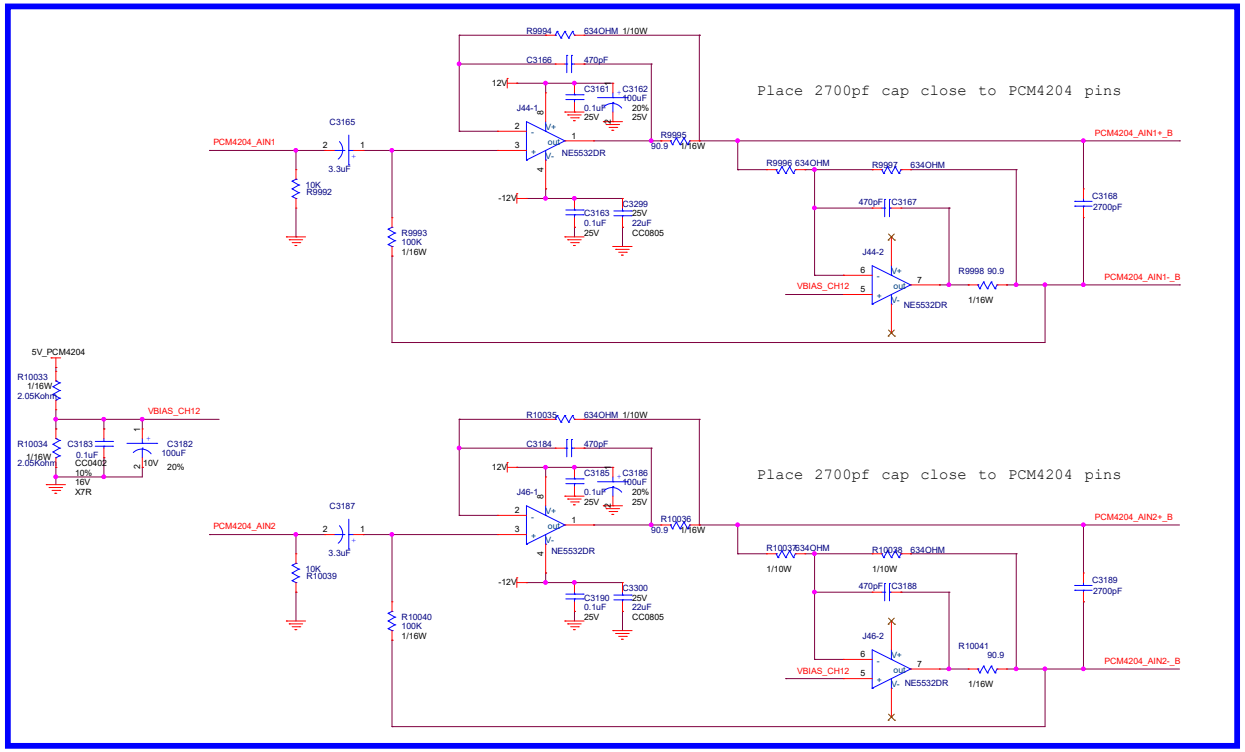
Table 3. Sampling Mode Selection for PCM Slave Mode Operation

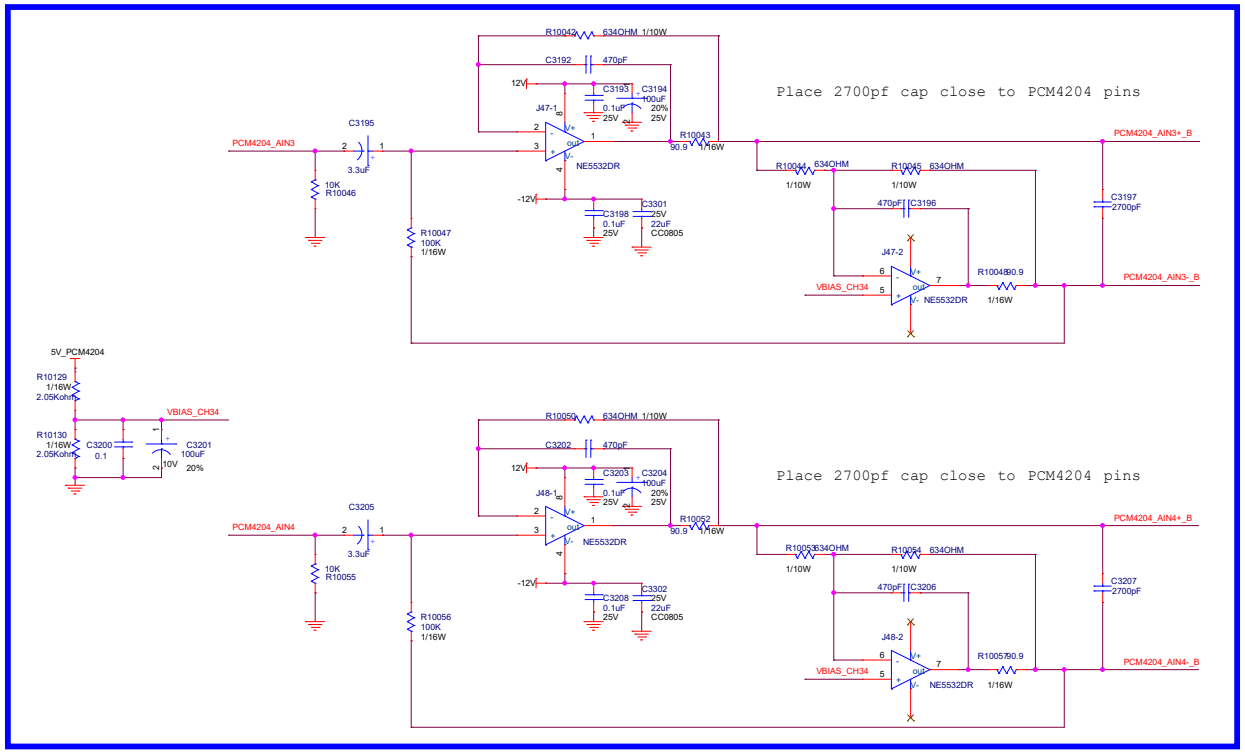
FS2	FS1	FS0	SAMPLING MODE
0	0	0	Single Rate with Clock Auto-Detection
0	0	1	Dual Rate with Clock Auto-Detection
0	1	0	Quad Rate with Clock Auto-Detection
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

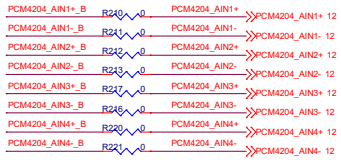
Table 6. Slave Mode Audio Data Format Selection

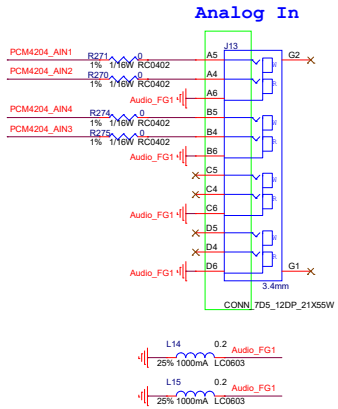
S/$\overline{M}$	FMT2	FMT1	FMT0	AUDIO DATA FORMAT
1	0	0	0	24-bit Left-Justified
1	0	0	1	24-bit I^{2}S
1	0	1	0	24-bit Right-Justified
1	0	1	1	TDM with No BCK Delay for Start of Frame
1	1	0	0	TDM with One BCK Delay for Start of Frame
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Reset circuit


Place 2700pf cap close to PCM4204 pins
PCM4204_AIN1
PCM4204_AIN1+_B
PCM4204_AIN1-_B
PCM4204_AIN2
PCM4204_AIN2+_B
PCM4204_AIN2-_B
5V_PCM4204
VBIAS_CH12
NE5532DR


Place 2700pf cap close to PCM4204 pins
PCM4204_AIN3
PCM4204_AIN3+_B
PCM4204_AIN3-_B
PCM4204_AIN4
PCM4204_AIN4+_B
PCM4204_AIN4-_B
5V_PCM4204
VBIAS_CH34
NE5532DR


PCM4204_AIN1+_B
PCM4204_AIN1-_B
PCM4204_AIN2+_B
PCM4204_AIN2-_B
PCM4204_AIN3+_B
PCM4204_AIN3-_B
PCM4204_AIN4+_B
PCM4204_AIN4-_B
PCM4204_AIN1+ 12
PCM4204_AIN1- 12
PCM4204_AIN2+ 12
PCM4204_AIN2- 12
PCM4204_AIN3+ 12
PCM4204_AIN3- 12
PCM4204_AIN4+ 12
PCM4204_AIN4- 12


Analog In
PCM4204_AIN1
PCM4204_AIN2
PCM4204_AIN4
PCM4204_AIN3
Audio_FG1
CONN_7D5_12DP_21X55W
3.4mm

L14
L15
Audio_FG1
25% 1000mA LC0603