Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	2.00mil	3.5	
1	Top Layer	Copper	1.50mil		
	Dielectric 1	FR-4 HIGH Tg	4.31mil	4.1	
2	GND1 Layer	Copper	1.40mil		
	Dielectric 2	FR-4 HIGH Tg	44.49mil	4.8	
3	GND2 Layer	Copper	1.40mil		
	Dielectric 3	FR-4 HIGH Tg	4.31mil	4.1	
4	Bottom Layer	Copper	1.50mil		
	Bottom Solder	Solder Resist	2.00mil	3.5	
	Bottom Overlay				

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Length
⌘	64	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	-
▽	2	39.37mil (1.000mm)	PTH	Slot	Top Layer - Bottom Layer	98.43mil (2.500mm)
✡	2	43.00mil (1.092mm)	NPTH	Round	Top Layer - Bottom Layer	-
□	4	66.93mil (1.700mm)	NPTH	Round	Top Layer - Bottom Layer	-
	72 Total					

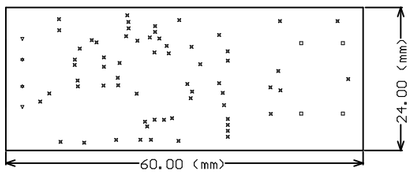
Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

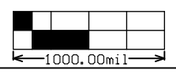
TOLERANCE
+0/-12 MILS FOR 12 MILS DRILL
+/- 3 MILS FOR PTH AND SLOT
+/- 2 MILS FOR NPTH

*FOR 90 OHMS IMPEDANCE 6 MILS TRACE WIDTH AND 6 MILS SPACING WITH 10 % TOLERANCE. IN TOP AND BOTTOM.

* ALL VIA'S ARE TENTED.

* VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED,PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED VIA TENTING/COVERING REQUIREMENTS.





DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 26 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER_____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

Texas Instruments

PROJECT TITLE: DEM-PCM2912AEVM
DESIGNED FOR: Public Release
FILE NAME: PCM2912AEVM-PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #:AMPS149	REV: A	SVN REV: Not in version control
LAYER NAME = Fabrication Drawing	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 8/6/2021 3:42:00 PM	TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	LAYOUT BY:
Ivan Salazar	TESSOLVE
SCALE: 1.00	ALTIUM DESIGNER VERSION: 21.2.2.38