Application Note

TAS6584-Q1 DC and AC Load Diagnostics

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ABSTRACT

TI's digital input automotive Class-D audio amplifier, TAS6584-Q1, offers a complete solution for both DC and AC load diagnostics. This amplifier is capable of detecting the connection of a single speaker and also two-way speaker systems consisting of a woofer in parallel with an AC-coupled tweeter. This application note provides insight into the working principle and application of DC and AC diagnostics in the TAS6584-Q1.

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Trademarks

1 Introduction

Class-D audio amplifier load diagnostics is a valuable tool for the ability of the amplifier to identify an incorrect connection from the amplifier speaker output pin to the speaker and within the speaker itself. This protects the amplifier from delivering energy into a potentially unsafe load. There are four conditions that are detected during load diagnostics:

- Short to Power (S2P)
- Short to Ground (S2G)
- Shorted Load (SL)
- Open Load (OL)

2 DC Load Diagnostics

2.1 What is DC Diagnostics

DC load diagnostics forces a direct current to measure the four conditions on the load. In a BTL, class-D amplifier each output pin must be tested. Figure 2-1 shows a simplified diagram of the configuration from the TAS6584-Q1 amplifier and the speaker load.

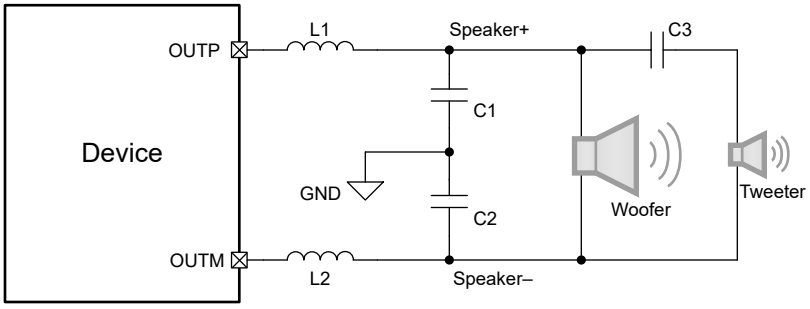

Figure 2-1. Simplified Diagram of Class-D Amplifier Output Connections

The Short to Power (S2P) and Short to Ground (S2G) tests determine if the output pins (OUTP, OUTM) or speaker terminals (speaker±) are shorted to the battery or GND. The Shorted Load (SL) and Open Load (OL) tests measure the DC resistance between OUTP or OUTM to determine if it is shorted or open.

2.2 DC Diagnostics, Short to Power, and Short to Ground

Figure 2-2 shows the simplified block diagram of DC diagnostics circuitry for S2P.

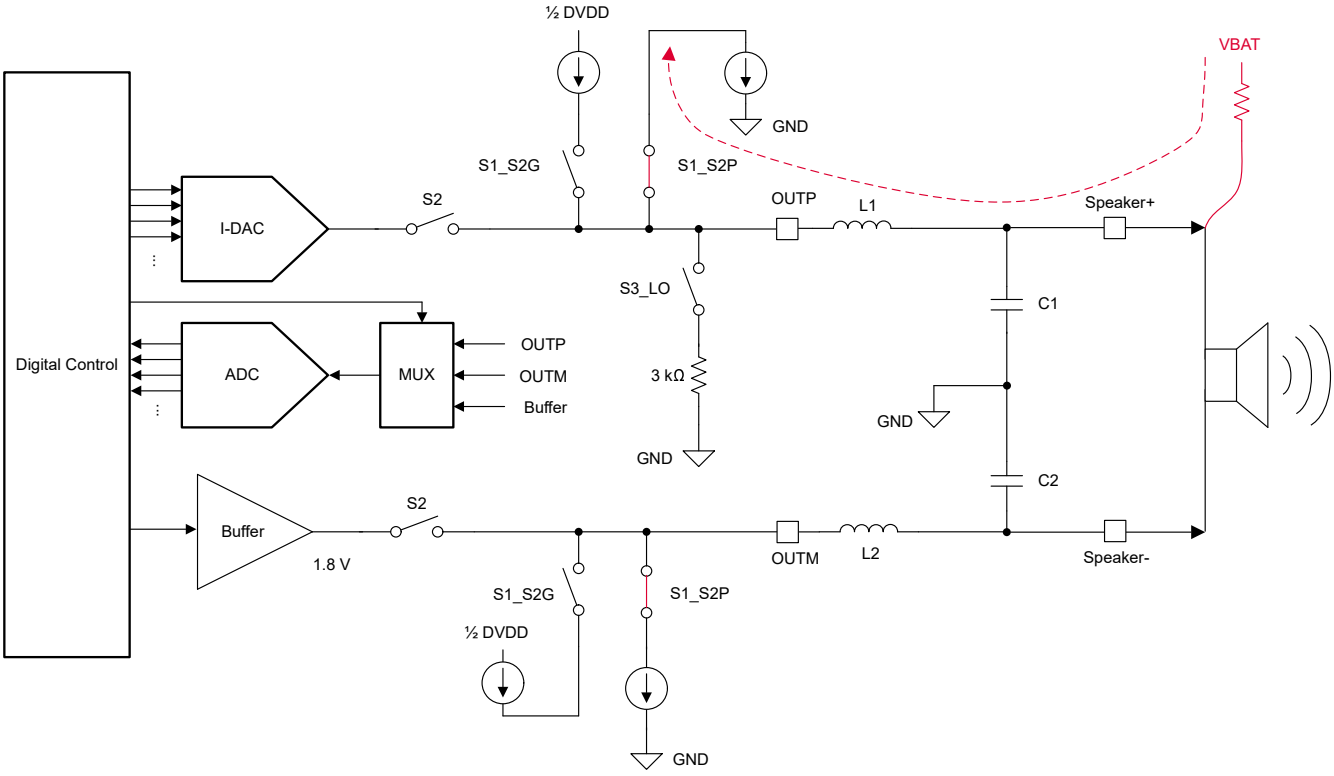

Figure 2-2. Diagram of S2P Detection

In S2P detection, the switches, S1_S2G, S2 and S3_LO are all opened, and S1_S2P are closed. The current sources sink current from the OUTP and OUTM pins. The sink current starts from 0 and ramps up to 1 mA linearly in 5 ms by default. After a settling time, which is 10 ms by default, an internal 10-bit ADC captures the voltage on the OUTP and OUTM pin. The ADC sampling results are averaged in a 0.2-ms time window to avoid incorrect detection caused by voltage spikes. Finally, the voltage information is compared with the internal S2P threshold to decide whether there is an S2P load fault.

Figure 2-3 shows the simplified block diagram of DC diagnostics circuitry for S2G.

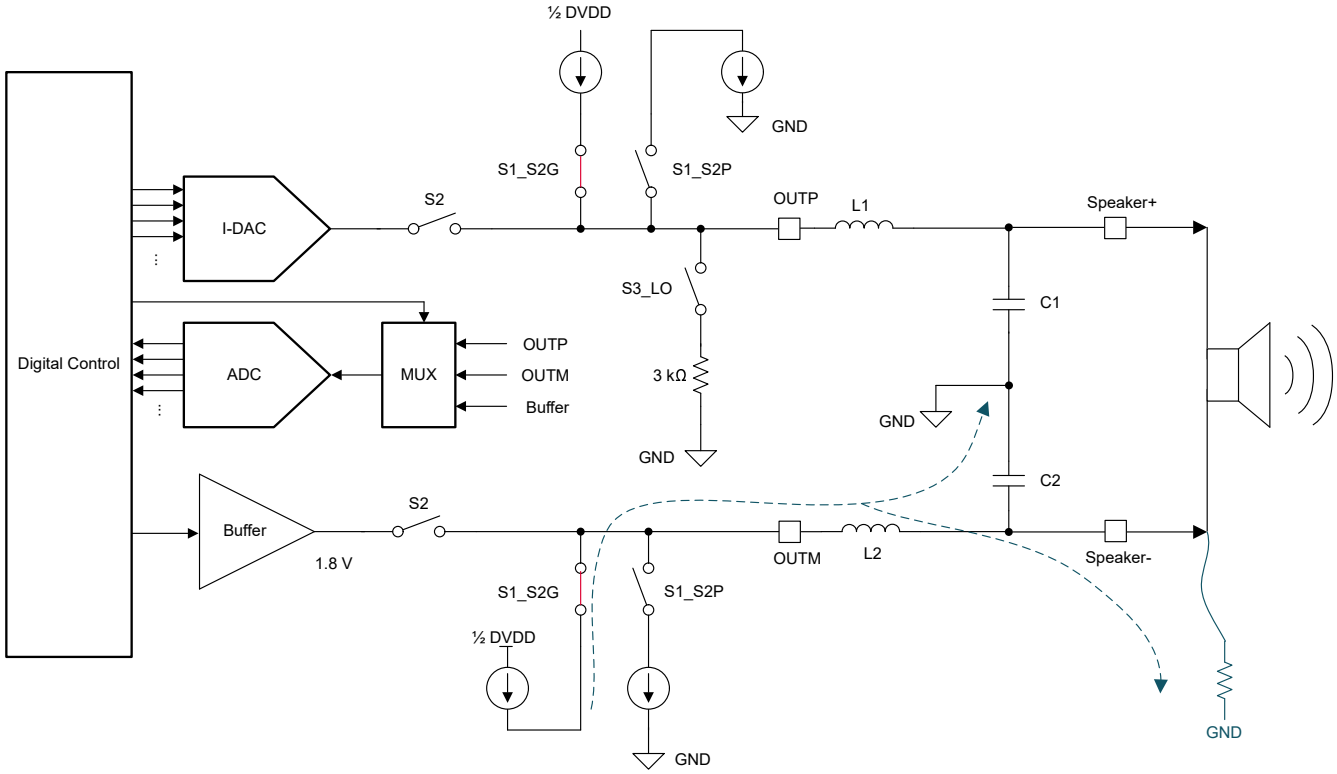

Figure 2-3. Diagram of S2G Detection

In S2G detection, only the S1_S2G switch is closed, all others are open. This is very similar to S2P detection, the current sources force current to the OUTP and OUTM pins. After the ramping time and the settling time, the voltage on the OUTP and OUTM nodes are captured and compared with the internal threshold to decide whether there is an S2G load fault.

The settings of ramp time, and settling time are combined for both S2P and S2G, which are configurable in register 0xB2. The options are listed in Table 2-1. These programmable ramping up time, ramping down time, and settling time provide options to eliminate the pop-click noise during the load diagnostic and improve the detection accuracy.

Table 2-1. Time Settings for S2P and S2G Detection

DC_LDG_CONTROL3 (Reg 0xB2)	LDG_RAMP1 <3:2>	Ramp Up Time or Ramp Down Time
	00	**5 ms**
	01	2.5 ms
	10	10 ms
	11	15 ms
	LDG_Settling <1:0>	Settling Time
	00	**10 ms**
	01	1 ms
	10	20 ms
	11	30 ms

2.3 DC Diagnostics, Shorted Load, and Open Load

Figure 2-4 shows the simplified block diagram of DC diagnostics circuitry for SL and OL detection.

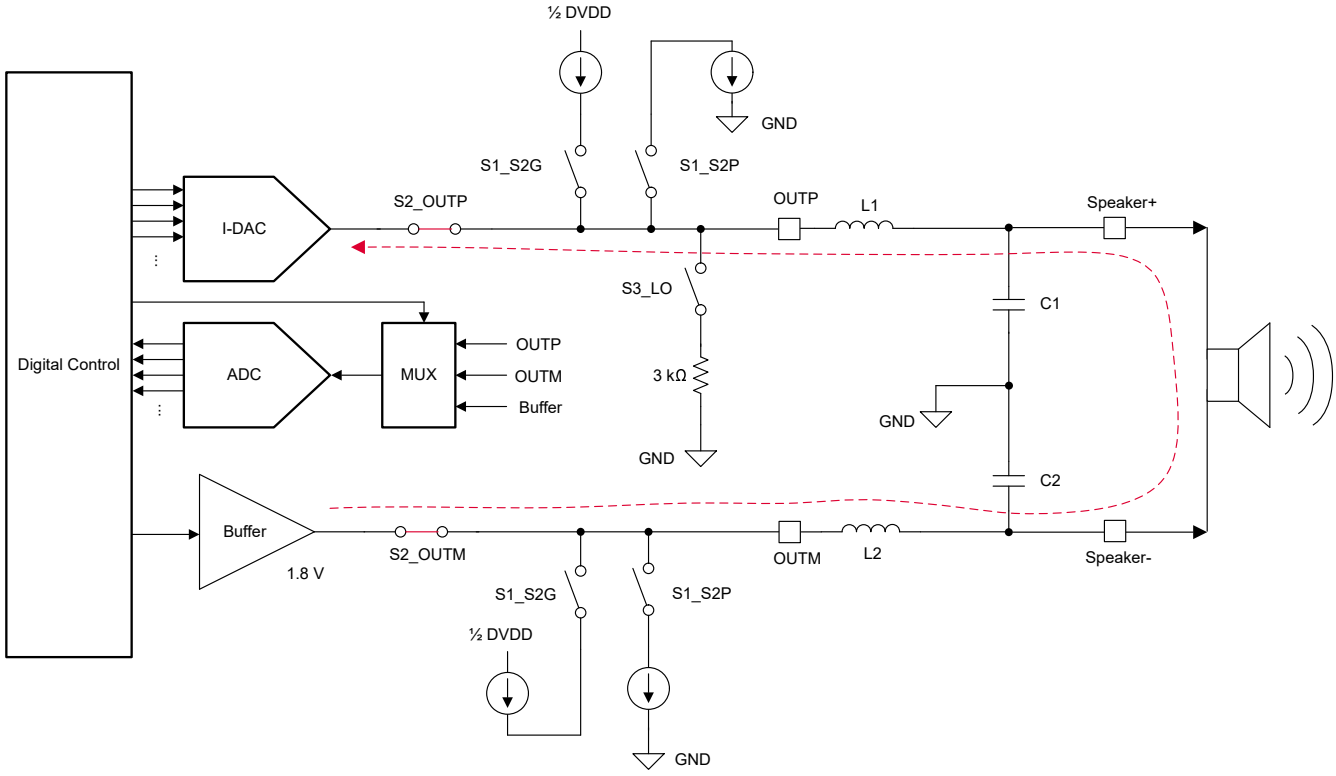

Figure 2-4. Diagram of SL and OL Detection

In the SL and OL detection, only the S2 switches are closed. The current DAC sinks a current to build a current loop indicated by the red dashed line. The sinking current starts from 0 and finally ramps up to 10 mA linearly in 15 ms by default. After a settling time, which is 10 ms by default, an internal 10-bit ADC captures the voltage on the OUTP and OUTM pin. The ADC sampling results are averaged in a 0.2-ms time window to avoid incorrect detection caused by any transient voltage spikes. Finally, the voltage information is compared with the SL threshold, which is programmable in register 0xB1, 0xB2, and B3 to decide if there is any short of load fault; and finally compared to an internal OL threshold to decide if there is an open load fault.

The settings of ramp time, settling time, and averaging time window for SL and OL detection are configurable in register 0xB2 and 0xB3. The options are listed in Table 2-2.

Table 2-2. Timing for SL and OL Detection

DC_LDG_CONTROL3 (Reg 0xB2)	LDG_RAMP2<7:6>	Ramp Up Time, Ramp Down Time
	00	10 ms
	01	5 ms
	10	20 ms
	11	15 ms
	LDG_SETTLING2<5:4>	Settling time
	00	10 ms
	01	5 ms
	10	20 ms
	11	15 ms
DC_LDG_ CONTROL4 (Reg 0xB3) Only Channel 1 is shown	DC_LDG_SL<7:4>	SL threshold
	0000	0.5 Ω
	0001	1.0 Ω
	0010	1.5 Ω
	...	
	1001	5.0 Ω

In some application circumstances where the speaker is AC coupled, there could be residual charges on the AC coupling capacitor due to the current flow in SL and OL detection leaving a voltage across the capacitor. This may lead to pop or click noise, or potentially incorrect results. The TAS6584-Q1 solves this problem by continuously sampling the voltage across OUTP and OUTM and does not allow the internal state machine to proceed to the next state until the voltage across OUTP and OUTM has been discharged to less than 10 mV.

TAS6584-Q1 supports DC load diagnostics in PBTL configuration. The working principle is quite similar to BTL configuration, with the OUTP and OUTM pair changes to OUT1P, OUT2M and OUT3P, OUT4M.

2.4 DC Diagnostics Flowcharts and Timing

Figure 2-5 shows the flowchart and fault handling strategy in the TAS6584-Q1 DC load diagnostic procedure.

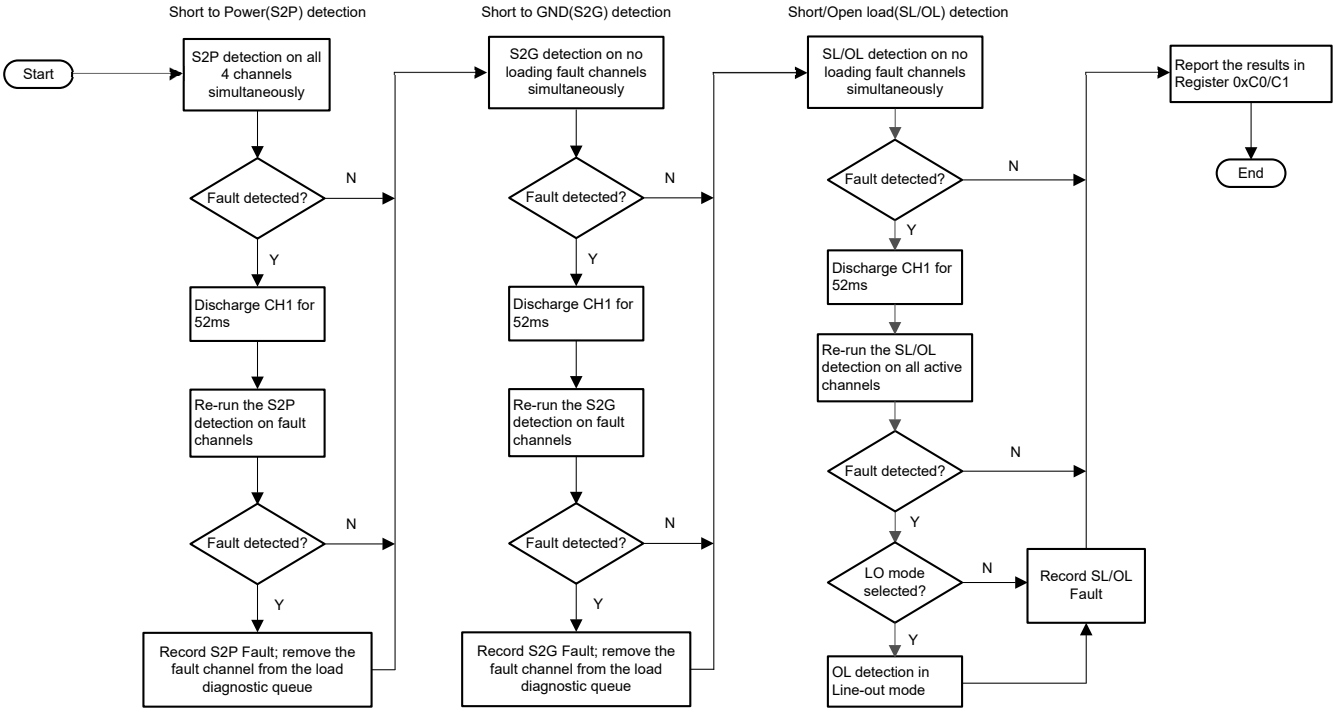

Figure 2-5. DC Load Diagnostic Flowchart

There are two ways to initialize a DC load diagnostic on TAS6584-Q1:

1. Change the channel state from Sleep to Mute or Sleep to Play. This occurs when the LDG BYPASS bit is not set in the DC load diagnostics control register (0xB0).
2. Manually set the channel state to DC load diagnostic. This is instigated by writing "11" to the channel state controlling bits in the Channel State Control Registers (0x03 and 0x04).

Figure 2-6 illustrates the recommended steps to execute a manually initialized DC load diagnostic on all 4 channels.

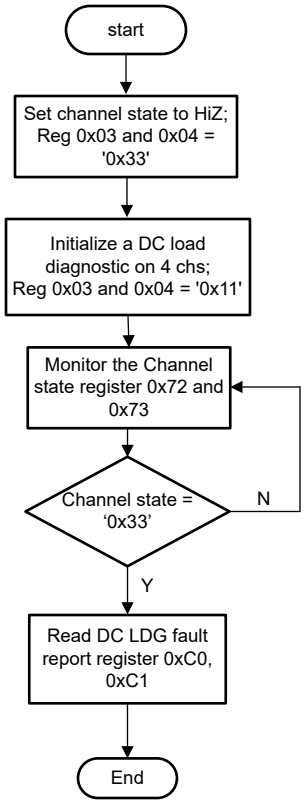

Figure 2-6. Manual DC Load Diagnostics Flowchart

TAS6584-Q1 employs parallel signal path in the DC load diagnostic detections to accelerate the execution on multichannels. The time consumption of a DC load diagnostic procedure depends on the fault conditions. In the case where no fault is detected, it typically takes about 154 ms to finish the procedure on all 4 channels, assuming the ramp time and settling time are all in default settings. In a worst-case scenario with default settings, it takes about 360 ms to complete the DC load diagnostic, at the condition of one channel in S2P fault, another channel in S2G fault, and at least one of the other two channels in SL or OL fault. If any of the channels is using AC coupled speakers, it could take a little bit longer because the device waits for the AC coupling capacitors to discharge after a *SL/OL detection* before moving forward.

2.5 Typical Cases and Associated Waveforms

Figure 2-7 shows the waveforms of good load in the case where DC load diagnostic was run on a single channel. An 8-Ω resistor was connected as the load.

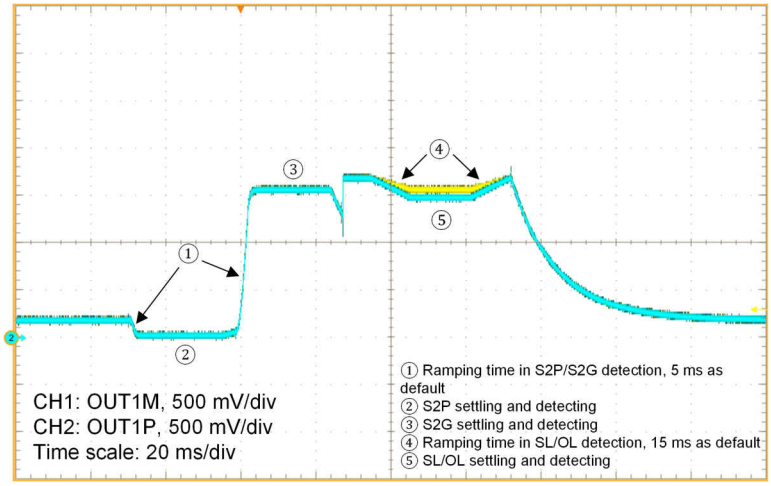

Figure 2-7. DC Load Diagnostic Waveform Without a Fault

Figure 2-8 shows the waveforms of the short-to-power (S2P) load fault condition in the case where the DC load diagnostic was run on a single channel. In this test, the speaker terminal connected to OUT1P was shorted to battery via a 2-kΩ resistor. To show the working principle more clearly, no load (OL) was connected between the output speaker terminals. The waveform shows that the internal circuit sinks 1-mA current from the OUT1P pin during the S2P detection, the voltage on OUT1P had an approximate 2-V drop due to the 2-kΩ resistance to battery. The voltage is still above the S2P threshold is thus reported as an S2P fault. An auto-retry was executed after S2P fault detected in the first trial. Figure 2-8 also shows that the DC detection did not proceed to S2G, OL or SL tests with the S2P fault present; therefore, the OL is not reported in the DC load diagnostics fault registers: 0xC0 and 0xC1.

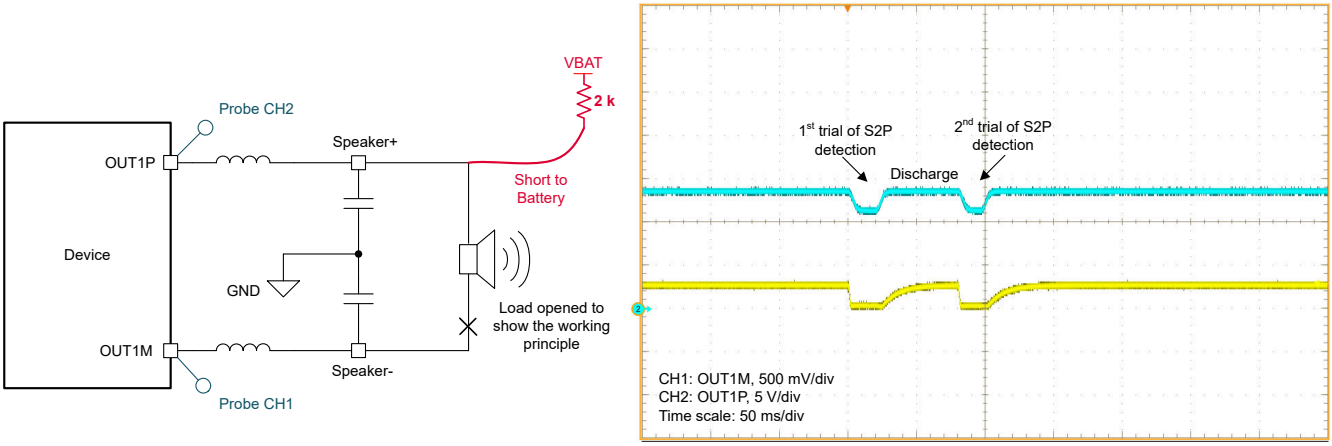

Figure 2-8. DC Load Diagnostic Waveform With a S2P Fault

Figure 2-9 shows the waveforms of short-to-ground (S2G) fault load condition in the case where the DC load diagnostic is run on a single channel. In this test, the speaker terminal connected to OUT1P is shorted to GND. To show the working principle more clearly, there is no load (OL) connected between the output speaker terminals. The waveform shows that when the internal circuit sources 1-mA current onto the OUT1P pin during the S2G detection, the voltage on OUT1P stayed at about 0 V due to the short to GND condition, which is below the S2G threshold. Thus a S2G fault is reported. An automatic retry is executed after the S2G fault is detected in the first trial. Figure 2-9 also shows that the DC detection did not proceed to OL or SL tests with the S2G fault present. Again, the OL will not be reported in the DC load diagnostics fault registers: 0xC0 and 0xC1.

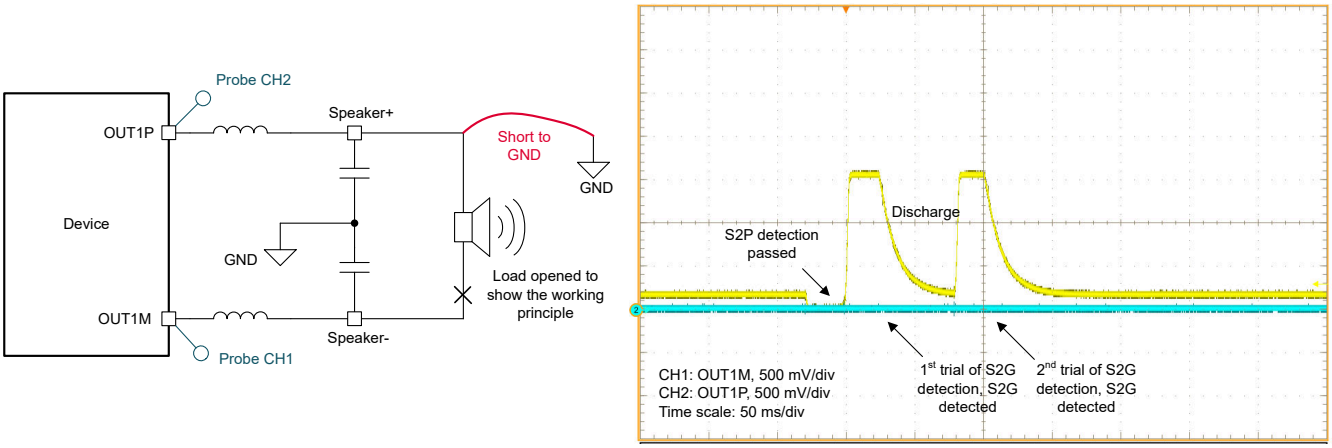

Figure 2-9. DC Load Diagnostic Waveform With an S2G Fault

Figure 2-10 shows the waveforms of an OL fault load condition in the case where DC load diagnostics is run on a single channel. The image shows that during the *SL/OL detection* phase, the voltage across the OUT1P, OUT1M pins is much higher than the normal case because of the OL condition. Thus an OL fault is reported. An automatic retry is executed after the fault was detected in the first trial to verify the fault.

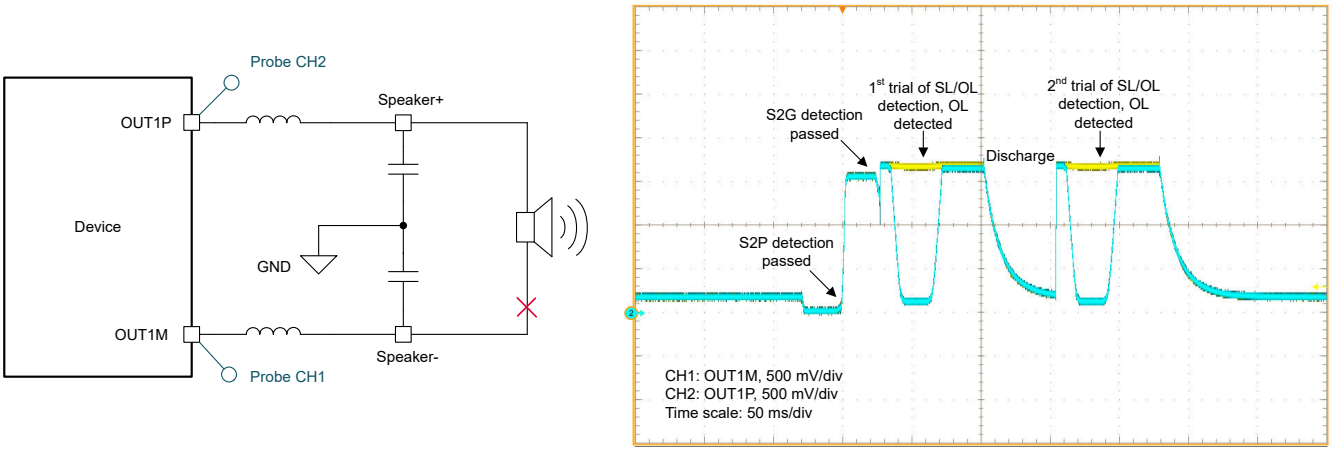

Figure 2-10. DC Load Diagnostics Waveform With an OL Fault

Figure 2-11 shows the waveforms of an shorted load (SL) fault load condition in the case where the DC load diagnostic is run on a single channel. The waveform shows that during the *SL/OL detection*, the phase voltage across the OUT1P and OUT1M pins is almost zero because of the shorted load condition. Thus an SL fault is reported. An automatic retry is executed after the fault was detected in the first trial to verify the fault.

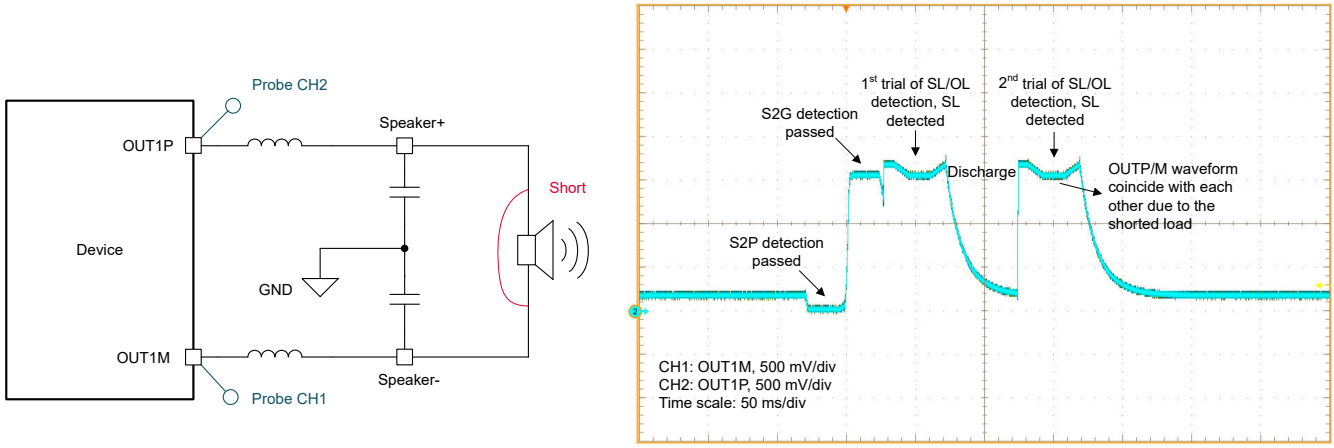

Figure 2-11. DC Load Diagnostic Waveform With a SL Fault

Figure 2-12 shows the waveform of the case where all 4 channels have good load conditions. The waveforms show that the diagnostics are run in parallel among the 4 channels, ensuring a fast diagnostic procedure.

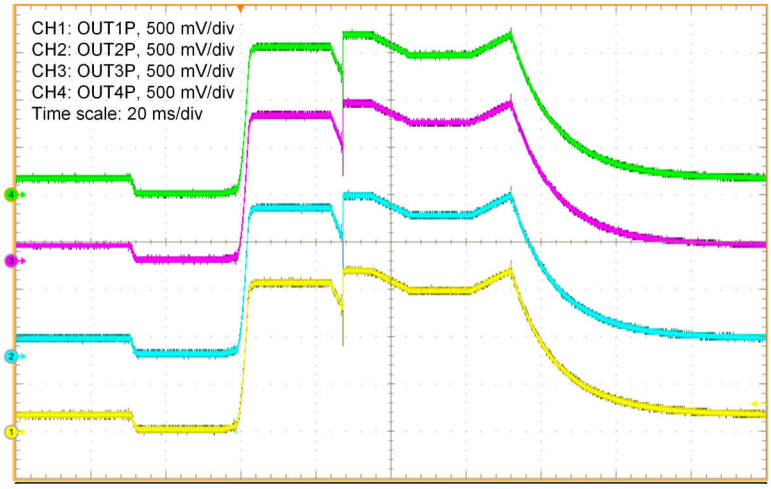

Figure 2-12. Four Channel Load Diagnostic Waveform Without Faults

Figure 2-13 shows the waveform of the case where CH2 had an S2G fault, CH4 has a OL fault and the other channels have a good load.

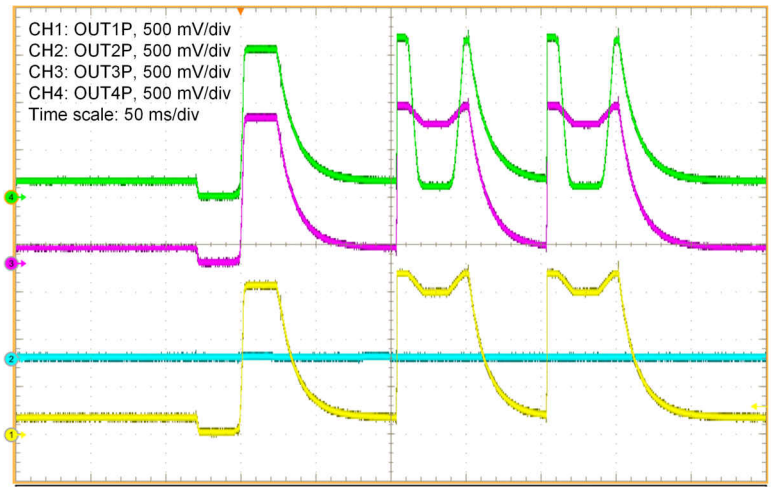

Figure 2-13. Four Channel DC Load Diagnostic Waveform With Faults

The image shows that the device first detected an S2G fault on channel 2; after 52 ms discharging, it re-ran the detection and confirmed the S2G fault; thus channel 2 was removed from further diagnostic detection sequence; then the remaining 3 channels moved forward to *SL/OL detection*; the *SL/OL detection* also ran a second time because of the OL fault detected on channel 4 in the first trial.

3 AC Load Diagnostics

The AC load diagnostics feature is needed to identify whether an AC coupled speaker is properly connected. The TAS6584-Q1 employs unique internal circuits and algorithms to measure the real part and the imaginary part of the load impedance accurately making the AC diagnostic easy to use. Users are responsible to determine the impedance threshold which indicates the load faults based on their system design.

Figure 3-1 illustrates the simplified block diagram for AC load diagnostics. A device self-generated 18.75-kHz sine current stimulus is applied across OUTP and OUTM. Voltages on OUTP and OUTM are captured for impedance calculation. All four channels share the same measurement circuits. Therefore, AC load diagnostics must run sequentially through the channels. It takes approximately 55 ms for each channel and 217 ms for all four channels to complete the AC diagnostic procedure.

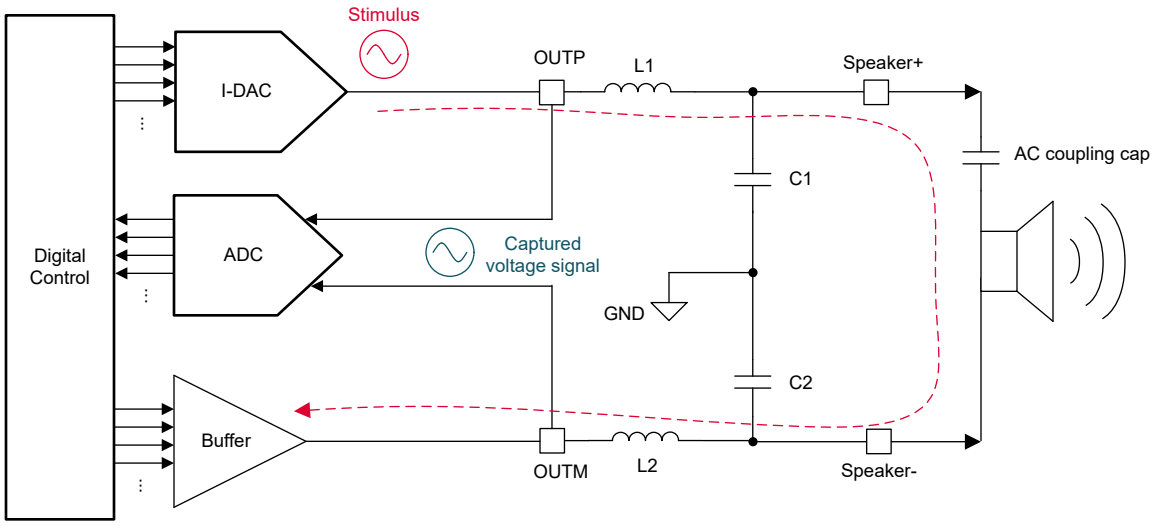

Figure 3-1. Diagram for AC Load Diagnostics

Note

The device measures the impedance of the path between the OUTP and OUTM pins, including the LC filter.

The TAS6584 also supports the ability to compare the results with a user-defined threshold to flag whether the AC-coupled loading is properly connected; or users can read the impedance results from the corresponding registers and have their own criterion based on the real or imaginary impedance measuring results. Table 3-1 lists the settings for AC load diagnostics.

Table 3-1. AC Load Diagnostic Setting

Register	Control Bits	Options	Description
AC_LDG_Ctrl1 (Reg 0xB5)	AC DIAG GAIN<4>	0	Gain = 1, range = 0–100 Ω
		1	Gain = 8, range = 0–25 Ω
AC_LDG_Ctrl2 (Reg 0xB6)	TW DET AVG<3>	0	Fast mode (4096 samples averaged, takes about 43 ms for each channel)
		1	Normal mode (32768 samples averaged, takes about 55 ms for each channel)
	TW DET CALC TYPE<1>	0	Impedance = Re(Z) + 0.5 × Im(Z)
		1	Impedance = Re(Z)
	TW DET JUDGE<0>	0	Enable tweeter detection, the result is compared with user-defined threshold and reported to Reg 0x2F
		1	Disable tweeter detection
AC_LDG_Ctrl3 (Reg 0xB7)	TW DET THRESHOLD<7:0>	/	0.8 Ω / code if AC DIAG GAIN = 0 0.1 Ω / code if AC DIAG GAIN = 1

Figure 3-2 illustrates the recommended flowchart to run AC load diagnostics.

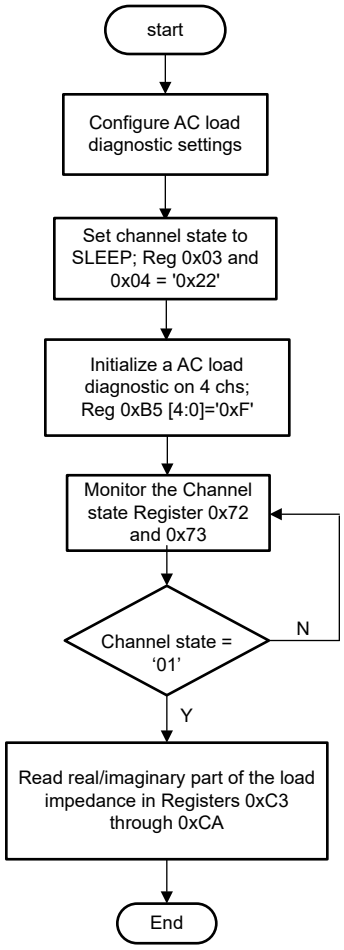

Figure 3-2. AC Load Diagnostics Flowchart

3.1 AC Load Diagnostics Example

This section gives an example of applying the AC load diagnostic on a tweeter or woofer in crossover connection, as Figure 3-3 shows.

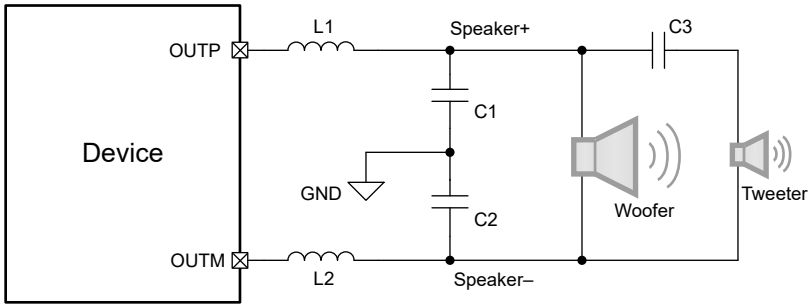

Figure 3-3. AC Load Diagnostic Test Setup

Figure 3-4 shows the impedance versus frequency sweep results of an independent woofer or tweeter and woofer plus an AC-coupled tweeter. These data were collected by a high-accuracy impedance analyzer. The image also shows the AC load diagnostic results reported by TAS6584-Q1. The following items can be identified from Figure 3-4:

- At the frequency point of 18.75-kHz, there is significant impedance difference among the good load and missing load. Users can take advantage of the impedance difference to identify different load status.
- The AC load diagnostic feature of TAS6584-Q1 is capable to identify the impedance.

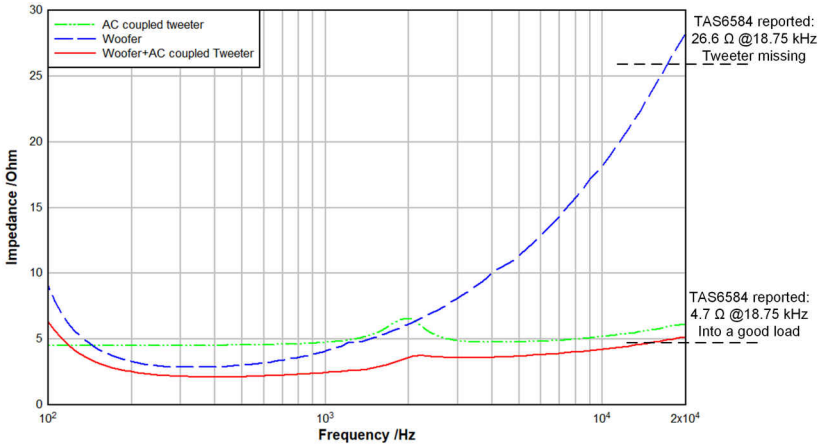

Figure 3-4. Impedance Measurement and AC Load Diagnostics Results

4 Summary

This application note provides detailed information on the use of DC load diagnostics and AC load diagnostics. Additional details are included from the TAS6584-Q1 data sheet. DC load diagnostics is a valuable tool in the system design for safe operation of an automotive audio system.

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