Hi3798M V200 Data Sheet

General Information

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About This Document

Purpose

The following table describes the content of the *Hi3798M V200 Data Sheet*. The highlighted portion outlines information contained in this document.

Document No.	Document Name	Description
Hi3798M V200 Data Sheet 01	General Information	• Product Overview • Boot Mode • Address Space Mapping • Soldering Process • Moisture-Sensitive Specifications • Ordering Information • Acronyms and Abbreviations
Hi3798M V200 Data Sheet 02	Hardware	• Package and Pins • Electrical Characteristics • Recommendations on Schematic Diagram Design • PCB Design Recommendations • Thermal Design Recommendations • Interface Timings
Hi3798M V200 Data Sheet 03	System	• Processor Subsystem • Security Subsystem • Always-on area subsystem • Power Management and Low-Power Control • Reset • Clock • System Controller • Peripheral Controller • Interrupt System • Timer • 64-bit Timer • WDG

Document No.	Document Name	Description
		• DMAC
Hi3798M V200 Data Sheet 04	Peripherals	• DDRC • FMC • MMC/SD/SDIO Controller • GPIO • UART • I^2C • IR • KEYLED • SCI • SPI • USB 2.0 • USB 3.0 • PCIe • SATA • LSDAC
Hi3798M V200 Data Sheet 05	Data Stream/Graphics Processing/Audio/Video Interfaces	• ETH • GMAC • FE PHY • TSI • Video Encoder • Video Decoder • HWC • GPU • VPSS • VDP • HDMI TX • AIAO

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3798M	V2*XX*

Intended Audience

This document is intended for:

- Technical support engineers
- Software development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 00B03 (2017-02-28)

This issue is the third draft release, which incorporates the following change:

modified.

Issue 00B02 (2017-01-15)

This issue is the second draft release, which incorporates the following changes:

Chapter 4 and chapter 5 are modified.

Issue 00B01 (2016-03-30)

This issue is the first draft release.

Contents

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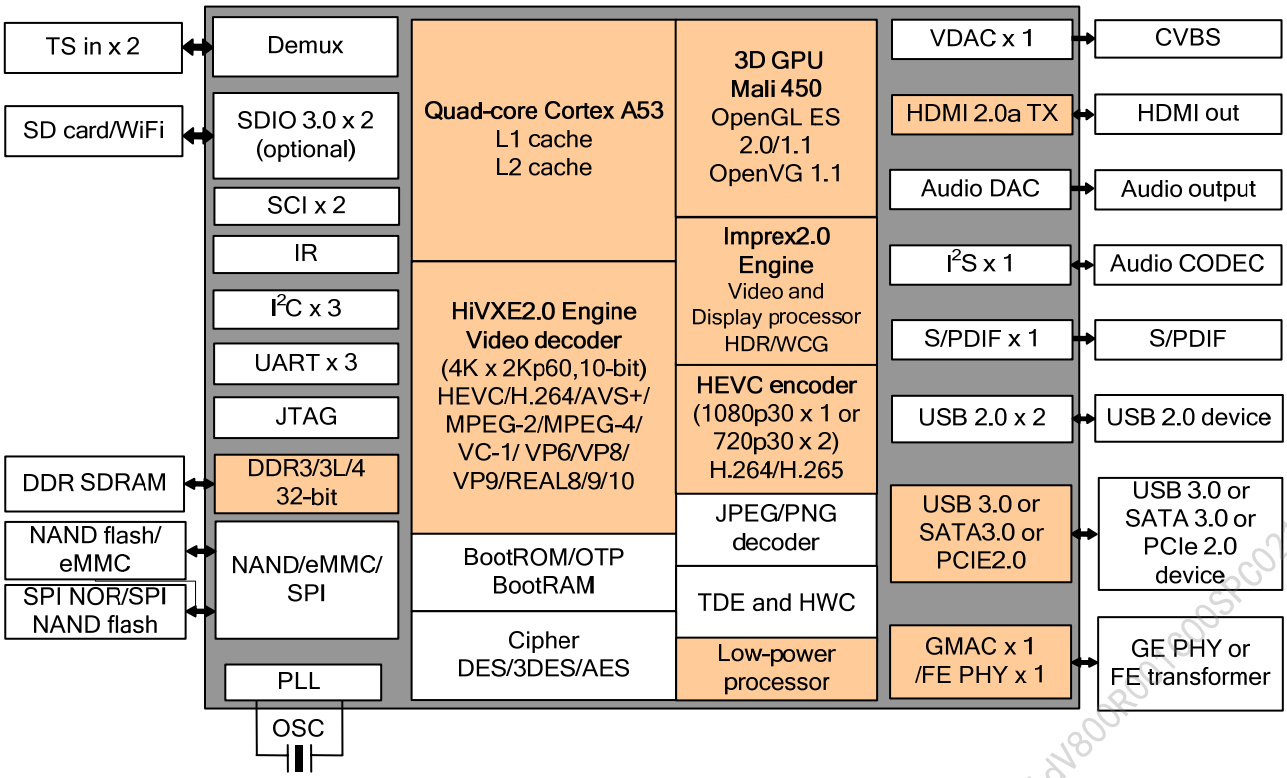
1 Product Overview

1.1 Application Scenario

Hi3798M V200 is a full-4K high-performance SoC that supports 4Kp60 decoding for the Internet Protocol television (IPTV)/over-the-top (OTT) STB markets. It integrates the 4-core 64-bit high-performance Cortex A53 processor and multi-core high-performance 2D/3D acceleration engine. Besides, it supports H.265 4K x 2K@P60 10-bit ultra-HD video decoding, high-performance H.265 HD video encoding, HDR video decoding and display, HDR-to-SDR conversion, and BT.2020, Dolby, and DTS audio processing. Hi3798M V200 also provides rich internal peripheral interfaces, such as USB 2.0, USB 3.0, SDIO 3.0, and PCIe 2.0 interfaces. These features help customers implement full-4K service deployment, and enable Hi3798M V200 to provide the best user experience in the industry in terms of picture quality, stream compatibility, video playback smoothness, and STB performance and meet the requirements of continuously increasing value-added services such as video communication, karaoke, cloud game, and multi-screen interaction.

Figure 1-1 Application block diagram



1.2 Architecture

Hi3798M V200 has the following features:

- Master processor
- 3D engine
- Security processing
- Memory interfaces
- Data stream interfaces
- Video codec
- Graphics and display processing
- Audio/Video interfaces
- Peripheral interfaces
- Low-power control

1.2.1 Master Processor

Hi3798M V200 integrates a quad-core ARM Cortex A53 processor as the master CPU to implement system functions and some audio and video processing tasks. This processor has the following features:

- Independent 32 KB I-cache and 32 KB D-cache, 512 KB shared L2 cache

- Integrated NEON
- Dynamic power consumption reduction such as dynamic voltage and frequency scaling (DVFS) and adaptive voltage scaling (AVS)

1.2.2 3D Engine

Hi3798M V200 integrates the high-performance quad-core Mali GPU to process 3D graphics and videos.

- OpenGL ES 2.0/1.1/1.0
- OpenVG 1.1
- 1080p30 UI processing capability
- 1080p@30 gaming applications

1.2.3 Security Processing

Hi3798M V200 has the following advanced security features:

- Trusted execution environment (TEE)
- Secure video path (SVP)
- Secure boot
- Secure storage
- Secure upgrade
- Protection for Joint Test Action Group (JTAG) and other debugging ports
- One-time programmable (OTP)
- Digital rights management (DRM)
- Downloadable conditional access (CA) (DCAS)
- HDCP 2.2/1.4 protection for HDMI outputs

1.2.4 Memory Interfaces

Hi3798M V200 provides the DDR SDRAM controller (DDRC), SDIO/MMC controller, and flash memory controller (FMC) that supports the SPI NOR, SPI NAND, and NAND flash.

DDRC

The DDRC controls the access to the dynamic DDR3/DDR3L/DDR4 SDRAM. It supports the following features:

- Maximum 2 GB capacity
- 32-bit memory
- Maximum 1066 MHz frequency
- Standby power-down

FMC

The FMC provides memory controller interfaces for connecting to external SPI NAND flash, SPI NOR flash, or synchronous and asynchronous NAND flash to access data. It supports the following features:

- Supports one external CS (SPI NAND flash, SPI NOR flash, or NAND flash).

- Supports the SPI NOR flash, SPI NAND flash, and NAND flash.
- Supports five types of SPIs, including the standard SPI, dual-output/dual-input SPI, quad-output/quad-input SPI, dual I/O SPI, and quad I/O SPI.
- Supports the SPI NAND flash with the following specifications:
  - 2 KB or 4 KB page size
  - 64/128 pages/block
- Supports the NAND flash with the following specifications:
  - 2 KB, 4 KB, 8 KB, or 16 KB page size
  - 64/128/256/512 pages/block
  - 8-bit width
  - Components with the DDR interface or asynchronous interface, and Toggle 1.0/2.0, ONFI 2.3, and ONFI 3.0 components
- Supports the error checking and correction (ECC) function for the SPI NAND flash and NAND flash.
  - 8-bit/1 KB, 16-bit/1 KB, 24-bit/1 KB, 28-bit/1 KB, 40-bit/1 KB, and 64-bit/1 KB Bose-Chaudhuri-Hocquenghem (BCH) code ECC (1 KB means the 1 KB level but not exactly 1024 bytes.)
  - Enable and disable of the ECC function and ECC code generation
- Supports the randomizer only in non-ECC0 mode when the page size is 8 KB or 16 KB. It is disabled in other modes.

MMC/SD/SDIO Controller

Hi3798M V200 integrates three high-speed large-capacity SDIO 3.0/MMC 5.0 controllers to control the access to the MMC/SD card. Extended peripherals such as Bluetooth and Wi-Fi devices can be connected over the SDIO interface.

Two controllers support the 1-/4-bit mode, and the other one supports the 1-/4-/8-bit mode for booting from the eMMC.

1.2.5 Data Stream Interfaces

The data stream interfaces of Hi3798M V200 include the Ethernet port and transport stream interface (TSI).

Ethernet Port

Hi3798M V200 provides one Ethernet controller (ETH for short), integrates one 10 Mbit/s or 100 Mbit/s PHY, and provides a megabit Ethernet media access control (MAC) and a gigabit Ethernet MAC.

- One 10/100 Mbit/s PHY interface or one RGMII/RMII
- 10/100/1000 Mbit/s (gigabit MAC), half-duplex or full-duplex mode
- Embedded 10/100 Mbit/s PHY, supporting the EEE function
- Configurable destination MAC address filtering table, which filters the input frames of the Ethernet port
- Traffic control of the CPU interface, protecting the CPU against heavy traffic

TSI

Hi3798M V200 integrates a TSI controller, which has the following features:

- Parsing and demultiplexing of MPEG2 TSs complying with the standards of the ISO 13818-1 (GB 17975-1) system layer
- At most one external standard serial TS input and one external standard serial TS input/output
- Playback of 3-channel TSs from the memory
- Maximum 96 hardware PID channels, processing at most 5-channel TSs at the same time

1.2.6 Video Codec (HiVXE 2.0 Processing Engine)

Hi3798M V200 integrates the HD video and graphics codec that supports various protocols (H.265/VP9/H.264/AVS+/MVC/VC-1/MPEG-2/MPEG-4/AVS/VP6/VP8/JPEG/PNG), providing powerful video and graphics encoding and decoding capabilities.

- H.265/HEVC Main/Main 10 Profile@Level 5.1 high-tier, maximum 4K x 2K@60 fps decoding capability
- H.264/AVC BP/MP/HP@Level 5.1; H.264/AVC MVC, maximum 4K x 2K@30 fps decoding capability
- Maximum 4K x 2K@60 fps 10-bit VP9 decoding capability
- Maximum 1080p@60 fps VP6/8 decoding capability
- Maximum 1080p@60 fps MPEG-1 decoding capability
- Maximum 1080p@60 fps MPEG-2 SP@ML, MP@HL decoding capability
- MPEG-4 SP@Levels 0–3, ASP@Levels 0–5, GMC, short header format, maximum 1080p@60 fps decoding capability
- AVS Baseline Profile@Level 6.0, AVS-P16 (AVS+), maximum 1080p@60 fps decoding capability
- VC-1 SP@ML, MP@HL, AP@Levels 0–3, maximum 1080p@60 fps decoding capability
- Maximum 1080p@60 fps Real8/9/10 decoding capability
- Full HD JPEG Baseline decoding, up to 64 megapixels
- MJPEG Baseline decoding, maximum 1080p@40 fps decoding capability
- PNG decoding, maximum 64 megapixels
- H.265 MP@Level 5.1 and H.264 BP/MP/HP@Level 4.2 video encoding, maximum 1080p@30 fps encoding or 2-channel 720p@30 fps encoding capability
- JPEG Baseline encoding, maximum 1080p@30 fps encoding capability
- VBR or CBR mode for video encoding

1.2.7 Graphics and Display Processing (Imprex 2.0 Processing Engine)

Hi3798M V200 integrates the dedicated two dimensional engine (TDE), dedicated multi-layer graphics or video overlaying engine (hardware composer engine), and dedicated display processing engine.

- Hardware overlaying of multiple graphics and video inputs
- 3-layer on-screen display (OSD) and three video layers

- Maximum 4K x 2K image output
- Mosaic and multi-region display
- Mirroring
- 16-bit or 32-bit color depth
- Graphics and video rotation
- LetterBox and PanScan
- 3D video processing and display
- Multi-order vertical and horizontal scaling of videos and graphics as well as free scaling
- Low-delay display
- Enhanced full-hardware TDE
- Full-hardware anti-aliasing and anti-flicker
- Color space conversion (CSC) with configurable coefficients (including BT.2020)
- Image enhancement and noise reduction
- De-interlacing
- Sharpening
- Chrominance, luminance, contrast, and saturation adjustment
- Db/Dr processing for graphics and videos
- HDR

1.2.8 Audio/Video Interfaces

Hi3798M V200 integrates various audio/video input/output interfaces, providing rich audio/video input/output capabilities.

Video Output Interfaces

- One 4Kp60 or 1920 x 1080p@60 fps output+one SD output from the same source
- One HDMI 2.0a TX output, supporting HDCP 2.2/1.4, maximum 4K x 2K resolution
- One embedded digital-to-analog converter (DAC), supporting one composite video broadcast signal (CVBS) output

  Rovi and vertical blanking interval (VBI) video output

Audio Input and Output Interfaces

- Sony/Philips digital interface format (S/PDIF) audio output interface
- One embedded DAC, which supports audio-left and audio-right channels (output interface of the RCA type, low impedance, and imbalance)
- One inter-IC sound (I^2S) or pulse code modulation (PCM) digital audio inputs/output
- One HDMI TX audio output

1.2.9 Peripheral Interfaces

Hi3798M V200 integrates diverse peripheral interfaces for connecting to various peripherals or extending system functions.

IR Interface

Hi3798M V200 integrates a dedicated infrared (IR) remote control RX unit, which receives IR data through an IR interface and has the following features:

- Flexible configuration for decoding data in various formats
- Error check on received data
- IR remote wakeup
- One input interface

LED/Keypad Controller

Hi3798M V200 integrates the LED/keypad controller for controlling the LED display and key scanning.

USB Controller

Hi3798M V200 integrates two USB 2.0 controllers and supports one USB 3.0 controller.

- The USB 2.0 controller supports the host function and Android debug bridge (ADB) debugging (USB0).
- The USB 2.0 controller support the low-speed and high-speed modes and extended hub.
- The USB 3.0 controller is backward compatible with USB 2.0.

PCIe Controller

Hi3798M V200 integrates one PCIe controller (PCIe for short) for extending the Wi-Fi devices.

SATA Controller

Hi3798M V200 integrates one SATA 3.0 controller for connecting to the SATA hard disk or extending the eSATA device.

GPIO Controller

Hi3798M V200 integrates multiple groups of GPIO controllers. Each group provides eight programmable input/output pins.

- Each GPIO pin can be configured as an input or output.
- As an input pin, the GPIO can act as an interrupt source.
- As an output pin, the GPIO can be independently set to 1 or 0.

UART

Hi3798M V200 integrates three universal asynchronous receiver transmitters (UARTs) for debugging, controlling, or extending external devices, such as the Bluetooth and keyboard. One of them is a 2-line interface, and the other two are 4-line interfaces.

I²C Controller

Hi3798M V200 integrates three inter-integrated circuit (I^2C) controllers, which serve as standard master I^2C devices to transmit/receive data to/from the slave devices over the I^2C bus.

SCI

Hi3798M V200 integrates a smart card interface (SCI) controller and provides two SCIs that support the ISO/IEC 7816-3, ISO/IEC 7816-10 protocols and T0, T1, and T14 asynchronous transmission protocols. The CPU reads data from or writes data to the smart card through the SCI and implements serial-to-parallel conversion (when it reads data from the smart card) and parallel-to-serial conversion (when it writes data to the smart card).

1.2.10 Low-Power Control

Hi3798M V200 supports various low-power modes to dynamically reduce power consumption.

- Various system operating modes, including the normal mode, light standby mode, and deep standby mode
- Module-level low-power control
- DVFS based on CPU load monitoring
- AVS based on CPU timing monitoring
- Ultra-low-power standby design, including various standby wakeup modes, such as remote control wakeup and key wakeup

2 Boot Mode

After the chip is powered on, the system is reset. After the reset is deasserted, the CPU jumps to the internal BOOTROM space to execute the boot process. After the internal BOOTROM boot program is executed, if the external pin USB_BOOT is low level, the chip directly boots from the USB port; otherwise, the chip boots from an external memory.

Hi3798M V200 can store the U-boot program in any of the following off-chip memories:

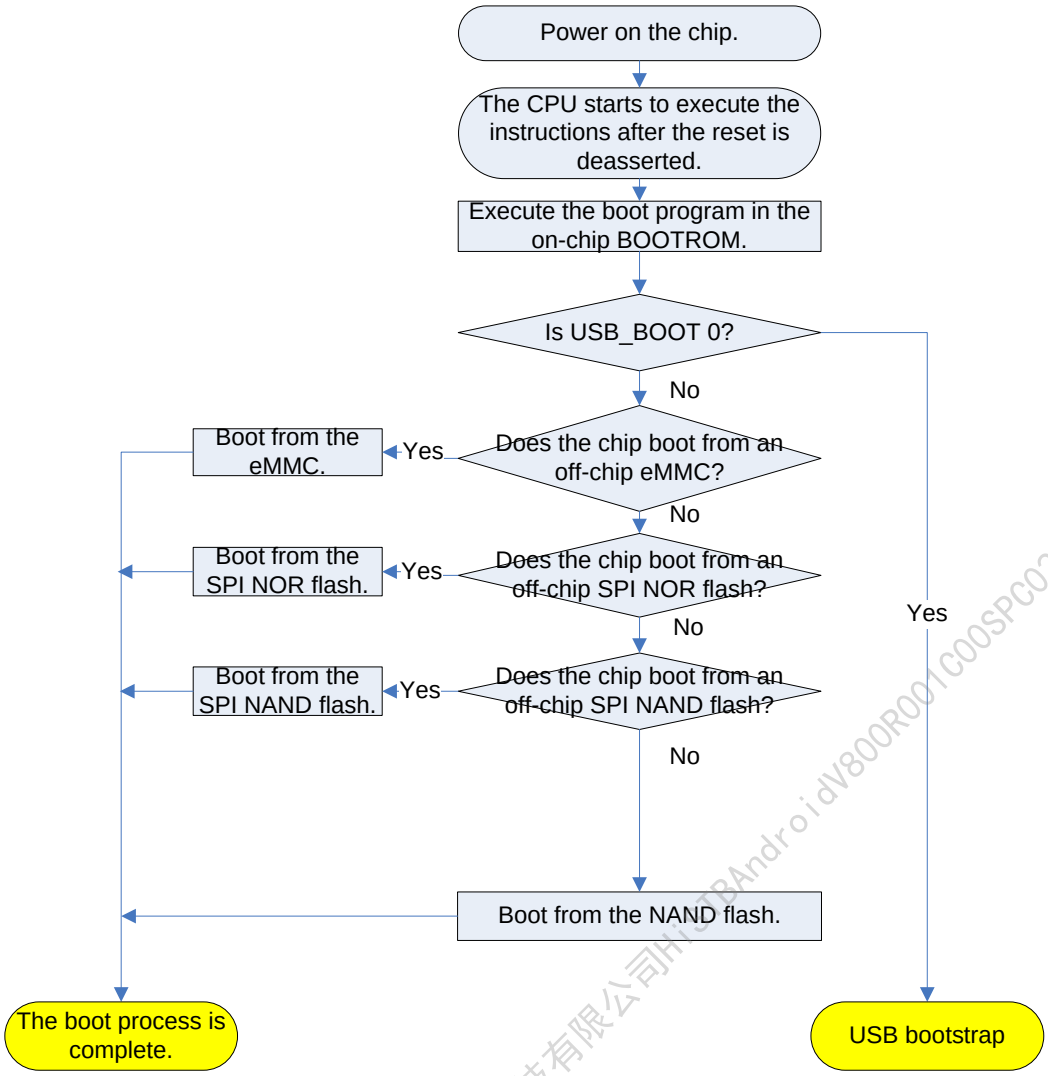
- SPI NOR flash
- Asynchronous NAND flash
- Synchronous NAND flash
- SPI NAND flash
- eMMC

CAUTION

The USB_BOOT pin is pulled high by using its internal resistor by default.

The boot_sel pin determines the flash memory from which the chip boots. Figure 2-1 shows the process.

Figure 2-1 Boot process



3 Address Space Mapping

Table 3-1 describes the address space mapping of Hi3798M V200.

Table 3-1 Address space mapping

Start Address	End Address	Object	Size (Unit: Byte)	Remarks
0x0000_0000	0x7FFF_FFFF	DRAM	2G	-
0x8000_0000	0xEFFF_FFFF	Reserved space	1.75G	
0xF000_0000	0xF000_1FFF	PCIe0 register space	8K	
0xF000_2000	0xF0FF_FFFF	Reserved space	16376K	
0xF100_0000	0xF100_FFFF	Generic interrupt controller (GIC) register space	64K	
0xF101_0000	0xF1FF_FFFF	Reserved space	16320K	
0xF200_0000	0xF4FF_FFFF	PCIe0 memory and configuration space	48M	
0xF500_0000	0xF7FF_FFFF	Reserved space	48M	
0xF800_0000	0xF800_0FFF	System control register	4K	-
0xF800_1000	0xF800_1FFF	IR register	4K	-
0xF800_2000	0xF800_2FFF	Timer 0/Timer 1 register	4K	-
0xF800_3000	0xF800_3FFF	LEDC register	4K	-
0xF800_4000	0xF800_4FFF	GPIO5 register	4K	-
0xF800_5000	0xF800_7FFF	Reserved space	12K	-
0xF800_8000	0xF800_8FFF	SEC timer 0/timer 1 register	4K	
0xF800_9000	0xF800_9FFF	SEC timer 2/timer 3 register	4K	
0xF800_A000	0xF83F_FFFF	Reserved space	4056K	-
0xF840_0000	0xF840_FFFF	8051 local RAM	64K	-

Start Address	End Address	Object	Size (Unit: Byte)	Remarks
0xF841_0000	0xF8A1_FFFF	Reserved space	6208K	
0xF8A2_0000	0xF8A2_0FFF	PERI_CTRL register	4K	-
0xF8A2_1000	0xF8A2_1FFF	IO_CONFIG register	4K	-
0xF8A2_2000	0xF8A2_2FFF	CRG register	4K	-
0xF8A2_3000	0xF8A2_3FFF	PMC register	4K	-
0xF8A2_4000	0xF8A2_8FFF	Reserved space	20K	
0xF8A2_9000	0xF8A2_9FFF	Timer 2/Timer 3 register	4K	-
0xF8A2_A000	0xF8A2_AFFF	Timer 4/Timer 5 register	4K	-
0xF8A2_B000	0xF8A2_BFFF	Timer 6/Timer 7 register	4K	-
0xF8A2_C000	0xF8A2_CFFF	WDG0 register	4K	-
0xF8A2_D000	0xF8A2_DFFF	WDG1 register	4K	-
0xF8A2_E000	0xF8A2_FFFF	Reserved space	8K	
0xF8A3_0000	0xF8A3_FFFF	MDDRC0 register	64K	-
0xF8A4_0000	0xF8A7_FFFF	Reserved space	256K	
0xF8A8_0000	0xF8A8_0FFF	SEC_CFG register	4K	-
0xF8A8_1000	0xF8A8_1FFF	Reserved space	4K	-
0xF8A8_2000	0xF8A8_2FFF	PASTC register (only opened in the internal version)	4K	
0xF8A8_3000	0xF8A8_FFFF	Reserved space	52K	
0xF8A9_0000	0xF8A9_FFFF	MKL	64K	-
0xF8AA_0000	0xF8AA_FFFF	Reserved space	64K	
0xF8AB_0000	0xF8AB_FFFF	OTP register	64K	-
0xF8AC_0000	0xF8AF_FFFF	Reserved space	256K	
0xF8B0_0000	0xF8B0_0FFF	UART0 register	4K	-
0xF8B0_1000	0xF8B0_1FFF	Reserved space	4K	-
0xF8B0_2000	0xF8B0_2FFF	UART2 register	4K	-
0xF8B0_3000	0xF8B0_3FFF	UART3 register	4K	-
0xF8B0_4000	0xF8B0_FFFF	Reserved space	48K	-
0xF8B1_0000	0xF8B1_0FFF	I^2C0	4K	-
0xF8B1_1000	0xF8B1_1FFF	I^2C1	4K	-
0xF8B1_2000	0xF8B1_2FFF	I^2C2	4K	-

Start Address	End Address	Object	Size (Unit: Byte)	Remarks
0xF8B1_3000	0xF8B1_7FFF	Reserved space	20K	-
0xF8B1_8000	0xF8B1_8FFF	SCI0 register	4K	-
0xF8B1_9000	0xF8B1_9FFF	SCI1 register	4K	-
0xF8B1_A000	0xF8B1_AFFF	SPI0 register	4K	
0xF8B1_B000	0xF8B1_FFFF	Reserved space	20K	
0xF8B2_0000	0xF8B2_0FFF	GPIO0 register	4K	-
0xF8B2_1000	0xF8B2_1FFF	GPIO1 register	4K	-
0xF8B2_2000	0xF8B2_2FFF	GPIO2 register	4K	-
0xF8B2_3000	0xF8B2_3FFF	GPIO3 register	4K	-
0xF8B2_4000	0xF8B2_4FFF	GPIO4 register	4K	-
0xF8B2_5000	0xF8B2_5FFF	Reserved space	4K	
0xF8B2_6000	0xF8B2_6FFF	GPIO6 register	4K	-
0xF8B2_7000	0xF8B2_7FFF	GPIO7 register	4K	-
0xF8B2_8000	0xF8B2_8FFF	GPIO8 register	4K	-
0xF8B2_9000	0xF8B2_9FFF	GPIO9 register	4K	-
0xF8B2_A000	0xF8B3_6FFF	Reserved space	48K	
0xF8B3_7000	0xF8B3_FFFF	Reserved space	36K	
0xF8B4_0000	0xF8B4_FFFF	GZIP register	64K	
0xF8B5_0000	0xF8BA_FFFF	Reserved space	384K	
0xF8BB_0000	0xF8BB_FFFF	System count register	64K	
0xF8BC_0000	0xF8C0_FFFF	Reserved space	320K	
0xF8C1_0000	0xF8C1_EFFF	TDE register	60K	-
0xF8C1_F000	0xF8C1_FFFF	TDE MMU register	4K	
0xF8C2_0000	0xF8C2_FFFF	Reserved space	64K	
0xF8C3_0000	0xF8C3_EFFF	Video decoder for high-definition (VDH) register	60K	
0xF8C3_F000	0xF8C3_FFFF	VDH MMU register	4K	
0xF8C4_0000	0xF8C4_EFFF	JPGD0 register	60K	-
0xF8C4_F000	0xF8C4_FFFF	JPGD0 MMU register	4K	-
0xF8C5_0000	0xF8C6_FFFF	Reserved space	128K	
0xF8C7_0000	0xF8C7_EFFF	PGD register	60K	-

Start Address	End Address	Object	Size (Unit: Byte)	Remarks
0xF8C7_F000	0xF8C7_FFFF	PGD MMU register	4K	-
0xF8C8_0000	0xF8C8_EFFF	Video encoding/decoding unit (VEDU) register	60K	-
0xF8C8_F000	0xF8C8_FFFF	VEDU MMU register	4K	-
0xF8C9_0000	0xF8C9_FFFF	JPEG encoder (JPGE) register	64K	-
0xF8CA_0000	0xF8CA_FFFF	Reserved space	64K	
0xF8CB_0000	0xF8CB_EFFF	VPSS0 register	60K	-
0xF8CB_F000	0xF8CB_FFFF	VPSS0 MMU register	4K	-
0xF8CC_0000	0xF8CC_EFFF	Video display processor (VDP) register	60K	-
0xF8CC_F000	0xF8CC_FFFF	VDP MMU register	4K	-
0xF8CD_0000	0xF8CD_FFFF	AIAO register	64K	-
0xF8CE_0000	0xF8CF_FFFF	HDMI_TX register	128K	-
0xF8D0_0000	0xF8D2_FFFF	Reserved space	192K	-
0xF8D3_0000	0xF8D3_0FFF	HDMI_TX PHY register	4K	
0xF8D3_0000	0xF91F_FFFF	Reserved space	4924K	
0xF920_0000	0xF923_FFFF	GPU register	256K	
0xF924_0000	0xF981_FFFF	Reserved space	6012K	
0xF982_0000	0xF982_FFFF	SDIO0 register	64K	-
0xF983_0000	0xF983_FFFF	SDIO2/eMMC/SD card register	64K	-
0xF984_0000	0xF984_FFFF	GMAC register	64K	-
0xF985_0000	0xF985_FFFF	Reserved space	64K	
0xF986_0000	0xF986_0FFF	PCIe0 protection control register	4K	
0xF986_1000	0xF986_4FFF	Reserved space	16K	
0xF986_5000	0xF986_5FFF	USB2 PHY01 register	4K	
0xF986_6000	0xF986_FFFF	Reserved space	40K	-
0xF987_0000	0xF987_FFFF	DMAC register	64K	
0xF988_0000	0xF988_FFFF	USB2 host0 open host controller interface (OHCI) register	64K	-

Start Address	End Address	Object	Size (Unit: Byte)	Remarks
0xF989_0000	0xF989_FFFF	USB2 host0 enhanced host controller interface (EHCI) register	64K	-
0xF98A_0000	0xF98A_FFFF	USB3_0 register	64K	-
0xF98B_0000	0xF98B_FFFF	Reserved space	64K	-
0xF98C_0000	0xF98F_FFFF	USB2 OTG0 register	256K	-
0xF990_0000	0xF990_FFFF	SATA register	64K	
0xF991_0000	0xF994_FFFF	Reserved space	256K	
0xF995_0000	0xF995_FFFF	FMC register	64K	-
0xF996_0000	0xF996_0FFF	USB2 PHY2 register	4K	
0xF996_1000	0xF99E_FFFF	Reserved space	572K	-
0xF99F_0000	0xF99F_0FFF	Multi-cipher MMU register	4K	-
0xF99F_1000	0xF99F_FFFF	Reserved space	60K	-
0xF9A0_0000	0xF9A0_FFFF	Multi-cipher register	64K	-
0xF9A1_0000	0xF9A1_FFFF	SHA1 (secure) register	64K	-
0xF9A2_0000	0xF9A2_FFFF	SHA2 (non-secure) register	64K	-
0xF9A3_0000	0xF9A3_0FFF	RSA register	4K	
0xF9A3_1000	0xF9BF_FFFF	Reserved space	1916K	
0xF9C0_0000	0xF9C0_FFFF	Personal video recording 0 (PVR0) register	64K	-
0xF9C1_0000	0xF9C2_FFFF	Reserved space	128K	-
0xF9C3_0000	0xF9C3_FFFF	ETH register	64K	-
0xF9C4_0000	0xF9C4_FFFF	SDIO1 register	64K	-
0xF9C5_0000	0xFE1F_FFFF	Reserved space	69M	-
0xFE20_0000	0xFE2F_FFFF	FMC memory space register	1M	
0xFE30_0000	0xFFFD_FFFF	Reserved space	29654K	
0xFFFE_0000	0xFFFE_FFFF	BOOTRAM register (in remap mode) or reserved (in remap clear mode)	64K	-
0xFFFF_0000	0xFFFF_FFFF	BOOTROM register (in remap mode) or BOOTRAM (in remap clear mode)	64K	-

4 Soldering Process Recommendations

4.1 Overview

[Objective]

This chapter provides the recommendations on basic settings of the zone temperatures when the surface mounting technology (SMT) of the HiSilicon chip is used on the client.

[Application Scope]

HiSilicon Hi3798M V200

[Basic Information]

All HiSilicon products provided for clients comply with the Restriction of Hazardous Substances (RoHS). In the part number format Hi*xxxx*RBCV*xxx*, the letter *R* indicates RoHS. These products are lead-free. The lead-free technology and mixing technology are used for process control when the HiSilicon chip is used for reflow soldering on the client.

[Process Control for Reflow Soldering]

The definitions are as follows:

- HiSilicon chip: All HiSilicon chips provided for customers are lead-free RoHS-compliant products.
- Lead-free technology: A technology in which the solder paste and all components (including the board, all ICs, capacitors, and resistors) are lead-free.

4.2 Requirements on Parameters of the Lead-Free Reflow Soldering Process

Figure 4-1 shows the curve of the lead-free reflow soldering process.

Figure 4-1 Curve of the lead-free reflow soldering process

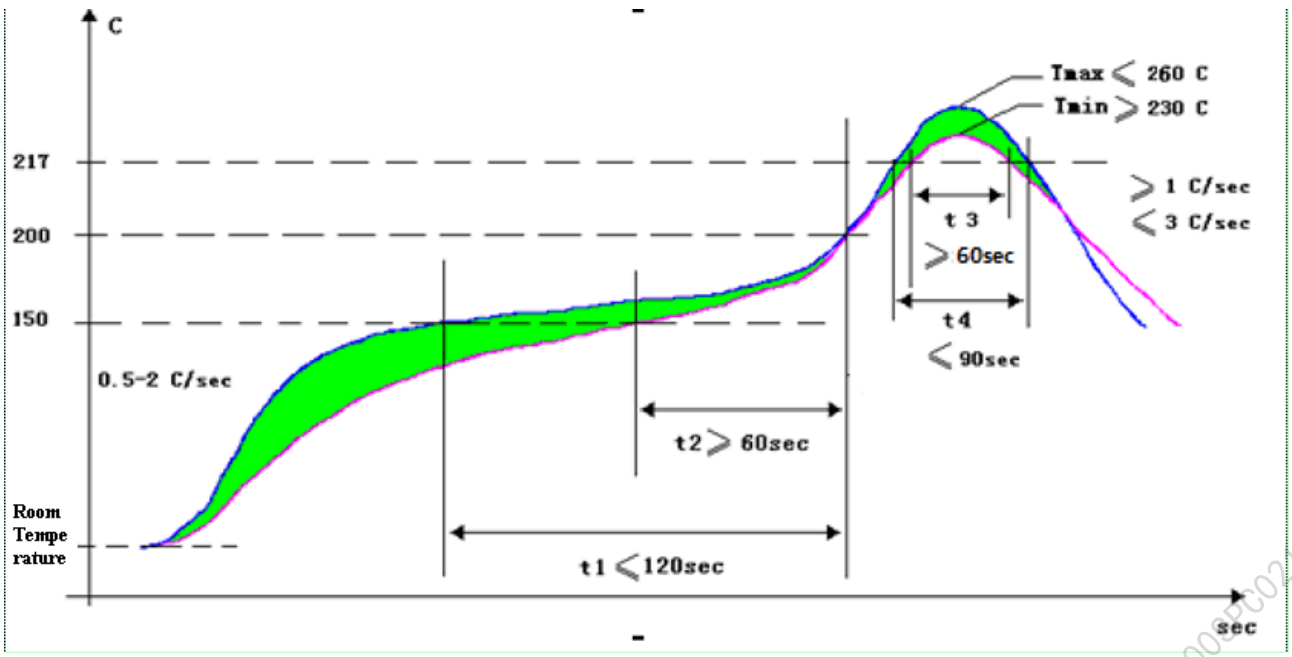


Table 4-1 describes parameters of the lead-free reflow soldering process.

Table 4-1 Parameters of the lead-free reflow soldering process

Zone	Duration	Heating Rate	Peak Temperature	Cooling Rate
Preheat zone (40°C–150°C or 104°F–302°F)	60s–150s	≤ 2.0ºC/s (≤ 36ºF/s)	-	-
Uniform temperature zone (150°C–200°C or 302°F–392°F)	60s–120s	< 1.0ºC/s (< 34ºF/s)	-	-
Reflow zone (greater than 217°C or 423°F)	60s–90s	-	230ºC–260ºC (446ºF–500ºF)	-
Cooling zone (Tmax to 180°C or 356°F)	-	-	-	1.0ºC/s (34ºF/s) ≤ Slope ≤ 4.0ºC/s (39ºF/s)

Note the following:

- Preheat zone: The temperature range is 40°C–150°C (104°F–302°F), the heating rate is about 2°C/s (36°F/s), and the duration of this temperature zone is 60s–150s.
- Uniform temperature zone: The temperature range is 150°C–200°C (302°F–392°F), the temperature is increased steadily, the heating rate is less than 1°C/s (34°F/s), and the zone duration is 60s–120s. (Note: Slow heating is required for this zone. Otherwise, improper soldering easily occurs.)
- Reflow zone: The temperature increases from 217°C (423°F) to Tmax, and then decreases from Tmax to 217°C (423°F). The zone duration is 60s–90s.

- Cooling zone: The temperature decreases from Tmax to 180°C (356°F). The maximum cooling rate is 4°C/s (39°F/s).
- It should take no more than 6 minutes for the temperature to increase from the 25°C (77°F) ambient temperature to 250°C (482°F).
- The values on the reflow soldering curve shown in Figure 4-1 are recommended values. The values need to be adjusted on the client as required.
- Typically, the duration of the reflow zone is 60s–90s. For the boards with great heat capacity, the duration can be prolonged to 120s. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 4-2 describes the temperature resistance standard for the lead-free package according to IPC/JEDEC 020D.

Table 4-2 Temperature resistance standard for the lead-free package according to IPC/JEDEC 020D

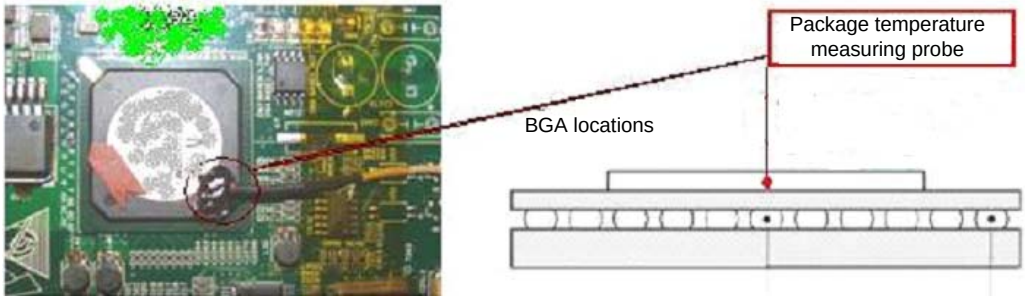
Package Thickness	Temperature 1 (Package Volume < 350 mm^3 or 0.02 $in.^3$)	Temperature 2 (Package Volume = 350–2000 mm^3 or 0.02–0.12 $in.^3$)	Temperature 3 (Package Volume > 2000 mm^3 or 0.12 $in.^3$)
< 1.6 mm (0.06 in.)	260°C (500°F)	260°C (500°F)	260°C (500°F)
1.6 mm to 2.5 mm (0.06 in. to 0.10 in.)	260°C (500°F)	250°C (482°F)	245°C (473°F)
> 2.5 mm (0.10 in.)	250°C (482°F)	245°C (473°F)	245°C (473°F)

The component soldering terminals (such as the solder ball and pin) and external heat sinks are not considered for volume calculation.

The method of measuring the reflow soldering process curve is as follows:

According to the JEP140 standard, to measure the package temperature, you are advised to place the temperature measuring probe of the thermocouple close to the chip surface if the chip package is thin, or to drill a hole on the package surface and place the temperature measuring probe of the thermocouple into the hole if the chip package is thick. The second method is recommended for all components because of the requirement on quantizing the component thickness. However, this method is not applicable if the chip package is too thin to drill a hole. See Figure 4-2.

Figure 4-2 Measuring the package temperature



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature measuring probe close to pins.

4.3 Requirements of Mixing Reflow Soldering

Lead-free components must be properly soldered during mixing reflow soldering. Table 4-3 describes mixing reflow soldering parameters.

Table 4-3 Mixing reflow soldering parameters

Zone		Lead BGA	Lead-free BGA	Other Components
Preheat zone (40°C–150°C or 104°F–302°F)	Duration	60s–150s		
	Heating up slope	< 2.5°C/s (37°F/s)		
Uniform temperature zone (150°C–183°C or 302°F–361°F)	Duration	30–90s		
	Heating up slope	< 1.0°C/s (34°F/s)		
Reflow zone (greater than 183°C or 361°F)	Peak temperature	210°C–240°C (410°F–464°F)	220°C–240°C (428°F–464°F)	210°C–245°C (410°F–473°F)
	Duration	30s–120s	60s–120s	30s–120s
Cooling zone (Tmax to 150°C or 302°F)	Cooling down slope	1.0ºC/s (34ºF/s) ≤ Slope ≤ 4.0ºC/s (39ºF/s)		

NOTE

The preceding parameter values are provided based on the soldering joint temperature. The maximum and minimum soldering joint temperatures for the board must meet the requirements described in Table 4-3.

When the soldering curve is adjusted, the package thermal resistance requirements on the board components must be met. For details about the requirements on package thermal resistance, see the IPC/JEDEC J-STD-020D standard. For details about the method of measuring the package temperature, see the JEP 140 standard.

Table 4-4 describes the thermal resistance standard for the lead package according to the IPC/JEDEC 020D standard.

Table 4-4 Thermal resistance standard for the lead package

Package Thickness	Temperature 1 (Package Volume < 350 mm^3 or 0.02 $in.^3$)	Temperature 1 (Package Volume ≥ 350 mm^3 or 0.02 $in.^3$)
< 2.5 mm (0.10 in.)	235°C (455°F)	220°C (428°F)
≥ 2.5 mm (0.10 in.)	220°C (428°F)	220°C (428°F)

The component soldering terminals (such as the solder ball and pin) and external heat sinks are not considered for volume calculation.

According to the JEP 140 standard, the method of measuring the temperature of the package soldered with the mixing technology is the same as that for measuring the temperature of the package soldered with the lead-free technology. For details, see section 4.2 "Requirements on Parameters of the Lead-Free Reflow Soldering Process."

5 Moisture-Sensitive Specifications

5.1 Overview

[Objective]

This chapter defines the usage principles for moisture-sensitive ICs to ensure that ICs are properly used.

[Application Scope]

All HiSilicon products for external customers

[Terminology]

- Floor life: longest period during which a HiSilicon chip can be stored in the workshop below 30°C (86°F) and 60% relative humidity (RH), that is, the time from moisture barrier bag (MBB) unpacking to reflow soldering
- Desiccant: a material for absorbing moisture and keeping the product dry
- Humidity indicator card (HIC): a card that indicates the humidity status
- Moisture sensitivity level (MSL): a level for measuring the moisture degree. The MSL of this product is 3.
- MBB: a vacuum bag for protecting products against moisture
- Solder reflow: reflow soldering
- Shelf life: normal storage period of a product with the MBB

5.2 HiSilicon Moisture-Proof Packaging

5.2.1 Basic Information

The vacuum packaging materials include:

- An HIC
- An MBB
- Desiccant

Figure 5-1 Vacuum packaging materials

5.2.2 Incoming Inspection

When the vacuum bag is unpacked before SMT in the factories of customers or outsourcing vendors:

- If the largest indicator dot of the HIC is not in blue or khaki, rebake the product by referring to Table 5-2.
- If the 10% RH dot of the HIC is in blue or khaki, the product is dry. In this case, replace the desiccant and pack the product into a vacuum bag.
- If the 10% RH dot of the HIC is not in blue or khaki and the 5% RH dot is in red or light green, the product has become damp. In this case, rebake the product according to Table 5-2.

5.3 Storage and Usage

[Storage Environment]

You are advised to use vacuum packaging for the product and store it below 30°C (86°F) and 60% RH.

[Shelf Life]

Normal storage period of a product with the MBB

Below 30°C (86°F) and 60% RH, the shelf life of the product with vacuum packaging is less than or equal to 12 months.

[Floor Life]

Table 5-1 describes the floor life below 30°C (86°F) and 60% RH.

Table 5-1 Floor life

MSL	Floor Life (Out of Bag) at Factory Ambient ≤ 30°C (86°F)/60% RH or As Stated
1	Unlimited at 30°C (86°F) or lower and at most 85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, the product must be reflowed within the time limit specified on the label.

[Usage of Moisture-Sensitive Products]

- If the product has been exposed to air for more than 2 hours at 30°C (86°F) or lower and at most 60% RH, rebake it and pack it into a vacuum bag.
- If the product has been exposed to air for no more than 2 hours at 30°C (86°F) or lower and at most 60% RH, replace the desiccant and pack the chip into a vacuum bag.

For details about other storage and usage rules, see the JEDEC J-STD-033A standard.

5.4 Rebaking

[Applicable Product]

All moisture-sensitive ICs of HiSilicon

[Application Scope]

All moisture-sensitive ICs that need to be rebaked

[Rebaking Reference]

Table 5-2 Rebaking reference

Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
≤ 1.4 mm (0.06 in.)	2a	3 hours	11 hours	5 days
	3	7 hours	23 hours	9 days
	4	7 hours	23 hours	9 days
	5	7 hours	24 hours	10 days

Body Thickness	Level	Baking at 125°C (257°F)	Baking at 90°C (194°F) ≤ 5% RH	Baking at 40°C (104°F) ≤ 5% RH
	5a	10 hours	24 hours	10 days
≤ 2.0 mm (0.08 in.)	2a	16 hours	2 days	22 days
	3	17 hours	2 days	23 days
	4	20 hours	3 days	28 days
	5	25 hours	4 days	35 days
	5a	40 hours	6 days	56 days
≤ 4.5 mm (0.18 in.)	2a	48 hours	7 days	67 days
	3	48 hours	8 days	67 days
	4	48 hours	10 days	67 days
	5	48 hours	10 days	67 days
	5a	48 hours	10 days	67 days

Note the following:

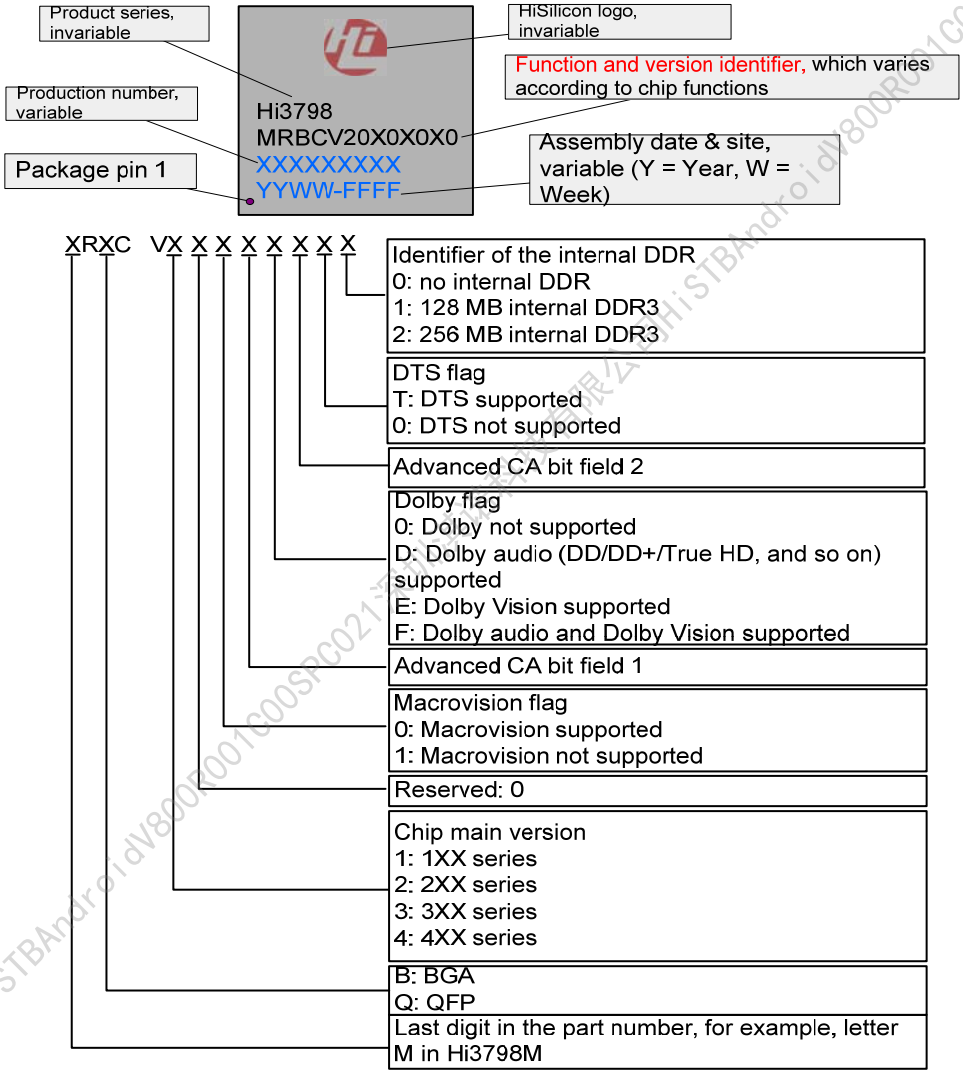
- Table 5-2 lists the minimum rebaking time required for damp products.
- Low-temperature rebaking is recommended.
- For details, see the JEDEC standard.

6 Ordering Information

Figure 6-1 illustrates the mark naming convention of Hi3798M V200.

Hi*XXXX* indicates the 6-digit product model before the part number.

Figure 6-1 Chip mark naming convention



The letter *X* in the part number indicates a digit that may vary and is only for internal use. For details about the corresponding rules of the advanced CA bit fields, consult HiSilicon technical engineers.

Table 6-1 Packages

Part Number	Package Type	Package Dimension	Pitch
Hi3798 MRBC V20XXXXXX	TFBGA	14 mm x 14 mm (0.55 in. x 0.55 in.)	0.65 mm (0.03 in.)

For example, if the part number is Hi3798MRBCV2010D000, the chip supports Dolby but not Macrovision (Rovi) and DTS and has no internal DDR SDRAM.

CAUTION

According to the technical agreement between HiSilicon and providers of third-party software, HiSilicon has no rights and is not obliged to provide technical samples of the third-party software for other parties. Therefore, if the third-party software or chips that are provided for only authorized users are involved (including but not limited to DD+ and DTS), ensure that you have obtained authorization from the third party when you place an order for the HiSilicon chip.

7 Acronyms and Abbreviations

A	
AAF	anti-aliasing digital filter
AC	alternating current
ACC	automatic contrast control
ACD	auto command done
ACL	access control list
ACLUT44	alpha 4 and color lookup table 4
ACLUT88	alpha 8 and color lookup table 8
ACLUTn	alpha n and color lookup table n
ACM	automatic color management
ACT	activation
ADAC	audio digital-to-analog converter
ADC	analog-to-digital converter
ADDR	address
AES	Advanced Encryption Standard
AF	adaptation field
AGC	automatic gain control
AGU	address generation unit
AHB	advanced high-performance bus
ALU	arithmetic logic unit
AMBA	advanced microcontroller bus architecture
AMP	asymmetric multi-processing
AO	audio output

AP	auto precharge
APB	advanced peripheral bus
API	application programming interface
AQ	asynchronism queue
AREF	auto refresh
ARGB	alpha red green blue
ARGB1555	alpha 1 bit red 5 bits green 5 bits blue 5 bits
ARGB4444	alpha 4 bits red 4 bits green 4 bits blue 4 bits
ARGB8565	alpha 8 bits red 5 bits green 6 bits blue 5 bits
ARGB8888	alpha 8 bits red 8 bits green 8 bits blue 8 bits
ARM	ARM
ARP	Address Resolution Protocol
ASCII	American Standard Code for Information Interchange
ATA	advanced technology attachment
ATAH	ATA host controller
ATE	acceptance test environment
ATR	answer to reset
AV	audio & video
AXI	advanced eXtensible interface
AYCbCr	alpha YCbCr
AYCbCr8888	alpha YCbCr8888

B

BA	bank address
BA	buffer assigner
BER	bit error rate
BGA	ball grid array
BGP	Border Gateway Protocol
BIST	build-in self test
BL4/BL8	burst length is 4/burst length is 8
BLOCK	block

BM	buffer management
BMC	bi-phase mark coding
BRC	bank-row- column
BRG	bridge
BS	barrel-shift
BVACT	bottom vertical active area
BVBB	bottom vertical back blank
BVFB	bottom vertical front blank
BW	bandwidth

C

CA	conditional access
CAR	committed access rate
CAS	column active select
CAS	channel associated signaling
CBC	cipher block chaining
CBR	constant bit rate
CC	continuity counter
CCITT	International Telegraph And Telephone Consultative Committee
CDR	clock data recovery
CFB	cipher feedback
CFG	configuration register
CGMS	copy generation management system
CL	CAS latency
ClassI	class I
ClassII	class II
CLK	clock
CLUT	color lookup table
CMD	command
CML	current mode logic
CMU	clock multiply unit
CODEC	coder decoder

COEF	coefficient
CoS	class of service
CPU	central processing unit
CRC	cyclic redundancy check
CRS	completion retry request
CS	chip select
CSA	common scrambling algorithm
CSC	color space conversion
CVBS	composite video blanking synchronization
CW	cipher word

D

DAC	digital-to-analog converter
DATE	digital part of analog TV encoder
DAV	DMA of audio and video
DBA	dynamic bandwidth assign
DC	direct current
DCKO	-
DCRC	data CRC error
DCT	discrete cosine transform
DDC	digital down convert
DDR	double data rate SDRAM
DDRC	DDR controller
DEC	decoder
DECC	data ECC
DEMUX	de-multiplexing
DHCP	Dynamic Host Configuration Protocol
DHD	display high definition
DLL	delay locked loop
DMA	direct memory access
DMAC	direct memory access controller
DOZE	doze
DRTO	data read timeout

DRM	digital rights management
DSD	display standard definition
DSP	digital signal processor
DTO	data transfer over
DTV	digital TV
DVB	digital video broadcasting
DVB-C	digital video broadcasting cable
DVD	digital versatile disc
DVI	digital video interactive (Intel)
DW	data width

E

E2E	end to end
EAV	end of active video
EB	eviction buffer
EBE	end-bit error
EBI	external bus interface
ECB	electronic codebook
ECC	error checking and correction
ECRC	end-to-end 32-bit CRC
ECS	embedded CPU subsystem
EDO	enhanced data out
EHCI	Enhanced Host Controller Interface
EMAC	Ethernet MAC
EMC	electromagnetic compatibility
EOP	end of packet
EP	end-to-end TLP is poisoned
ERR	error
ES	element stream
ESD	electro static discharge
ETH	Ethernet
ETU	elementary time unit

F

FCB	frame control block
FCS	frame check sequence
FE	fast Ethernet
FEC	forward error correction
FID	function identifier
FIFO	first in first out
FIQ	fast interrupt request
FIR	finite impulse response
FLASH	flash memory
FPGA	field programmable gate array
FRUN	FIFO underrun/overrun error

G

GB	guo biao
GE	gigabit Ethernet
GIC	generic interrupt controller
GIF	graphics interchange format
GMII	gigabit media independent interface
GND	ground
GPIO	general purpose input/output
GPON	gigabit-capable passive optical network
GPU	graphics processing unit
GTC	GPON transmission convergence

H

H2P	AHB bus translate into APB bus
HAC	Huffman AC
HACT	horizontal active area
HDC	high definition
HDR	high-dynamic range
HDMI	high definition multimedia interface

HF	horizontal filter
HFB	horizontal front blank
HGU	home gateway
HL	high level
HP	high performance
HPW	horizontal pulse width
HW	highway
I	
I^2C	inter-integrated circuit
I^2S	inter-IC sound
IBIS	I/O buffer information specification
ICMP	Internet Control Message Protocol
ICU	image capture unit
ID	identity
IDCT	inverse discrete cosine transform
IDLE	idle
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGMP	Internet Group Management Protocol
INS	instruction
INT	interrupt
IO	input output
IOCFG	input output configuration
IP	Internet Protocol
IPG	inter-packet gap
IPTV	Internet Protocol television
IPv6	Internet Protocol version 6
IR	infrared remoter
IRQ	interrupt request line
ISO	International Standard Organization
ISR	interrupt service routine

ITCM	instruction tightly coupled memory
ITU	International Telecommunications Union
ITU-R	International Telecommunication Union-Radiocommunication Sector
ITU-T	International Telecommunication Union-Telecommunication Standardization Sector
IV	initialization vector

J

JEDEC	Joint Electron Device Engineering Council
JESD79	JEDEC Standard Document 79
JPEG	Join Picture Expert Group
JTAG	Joint Test Action Group

L

LAN	local area network
LateCollision	late collision
LCD	liquid crystal display
LDO	low dropout regulator
LED	light emitting diode
LFB	line fill buffer
LL	low level
LLI	linked list item
LMR	load mode register
LOS	loss of signal
LP	low performance
LRB	line read buffer
LS	late start time
LSN	logic sector number
LSW	LAN switch
LUT	lookup table
LVCMOS	low voltage complementary metal oxide semiconductor transistor

M

MAC	media access control
MAP	address mapping
MAU	multiply accumulate unit
MAX	maximum
MCU	multi-point control unit
MDDRC	multi-port DDR/SDR controller
MDIO	management data input/output
MEM	memory
MII	media independent interface
MIN	minimum
MIS	management-information-system
ML	main level
MLC	multi-level cell
MLF	malformed
MMC	multi-media card
MMU	memory management unit
MOD	modulation
MP	main profile
MPCP	Multi-Point Control Protocol
MPI	MPEG physical interface
MSB	most significant bit
MSG	message
MSL	moisture sensitivity level
MTU	maximum transmission unit

N

NA	not applicable
NADDR	next address
NANDC	NAND flash controller
NAPT	network address port translation
NAT	network address translation
NEC	Nippon Electric Company

NFC	NAND flash controller
NTSC	National Television System Committee
O	
OAM	operation, administration and maintenance
ODT	on-die termination
OFB	output feedback
OFST	offset
OHCI	Open Host Controller Interface
ONT	optical network termination
ONU	optical network unit
OOB	out-of-band
OP	operating mode
OpenGL	-
OpenVG1.1	-
OTG	on-the-go
P	
P2P	point to point
PackageYUYV	package YUYV
PAD	packet assembler/disassembler
PAL	phase alternation line
PCB	physical control block
PCBd	physical control block downstream
PCI	Peripheral Component Interconnect
PCIE	PCI express
PCM	pulse code modulation
PCR	program clock reference
PES	packetized elementary stream
PGD	PNG and GIF decoder
PFI	payload FCS identifier

PHY	physical sublayer & physical layer
PID	packet identifier
PLI	payload length indicator
PLL	phase-locked loop
PLOAM	physical layer OAM
PMC	packet memory controller
PMU	power management unit
PNG	portable network graphics
PON	passive optical network
POR	power on reset
POTS	plain old telephone service
PP	page program
PPM	parts per million
PPPoE	point-to-point protocol over ethernet
PRBS	pseudo-random binary sequence
PSRAM	pseudo static random access memory
PTS	presentation time stamp
PUSI	payload unit start indicator
PVR	personal video record
PWM	pulse width modulation

Q

QAM	quadrature amplitude modulation
QinQ	802.1q in 802.1q
QoS	quality of service

R

RANK	rank
RB	ready or busy
RBC	row-bank-column
RC	readable only and self cleaning after reading
RCRC	response CRC error

RD	read
RE	response error
REQ	request
RES	resume
RF	radio frequency
RGB	red green blue
RGB444	red 4 bits green 4 bits blue 4 bits
RGB555	red 5 bits green 5 bits blue 5 bits
RGB565	red 5 bits green 6 bits blue 5 bits
RGB888	red 8 bits green 8 bits blue 8 bits
RH	relative humidity
RIP	Routing Information Protocol
RIS	remote installation services
RISC	reduced instruction set computer
RMII	reduced media independent interface
RO	read only
ROM	read-only memory
ROP	raster operation
RPT	report
RS	reed solomon
RST	reset
RSZ	resize
RTL	register transfer logic
RTO	response timeout
RW	read and write
RX	reception
RXDR	receive FIFO data request

S

SATA	serial advanced technology attachment
SBE	start-bit error
SBU	single business unit
SC	system controller

SCD	start code detect
SCI	smart card interface
SCL	serial clock line
SCR	system clock reference
SCU	snoop control unit
SD	secure digital
SDA	serial data and address
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SECC	-
Semi-Planar	-
SerDes	serializer/deserializer
SET	secure electronic transaction
SF	switch fabric
SFD	start frame delimiter field
SFU	single family unit
SIO	sonic input/output
SIR	session initiation request
SLA	service level agreement
SLC	single-level cell
SLEAD	simple lead
SLEADE	simple lead end
SLIC	subscriber line interface circuit
SMP	symmetric multi-processing
SNAP	sub network access point
SNR	signal-to-noise ratio
SoC	system on chip
SOP	start of PES
SP	simple profile
SPDIF	Sony/Philips digital interface
SPI	serial peripheral interface

SPS	seamless-pause-start
SQ	synchronization queue
SR	self-refresh
SRAM	static random access memory
SSMC	static memory controller
SSP	synchronous serial protocol
SSTL	stub series terminated logic
STA	status
STA	static timing analysis
STAT	status
SW	software item
SYNC	synchronization

T

TAR	target
TC	traffic class
TCM	tightly coupled memory
TCONT	transmission container
TCP	Transmission Control Protocol
TDE	two dimension engine
TDM	time division multiplexing
TEI	transmit error indicator
TIMER	timer
TLP	transaction layer packet
TPIT	TS packet index table
TS	target and source
TS	transport stream
TT	teletext
TV	television
TVACT	top vertical active area
TVBB	top vertical back blank
TVFB	top vertical front blank
TXDR	transmit FIFO data request

U

UART	universal asynchronous receiver transmitter
UC	unexpected completion
UDP	User Datagram Protocol
UI	user interface
ULPI	UTMI+ low-pin interface
UNI	user network interface
UR	unsupported request
USB	universal serial bus
UTMI	USB 2.0 transceiver macrocell interface
UXGA	ultra extended graphics array

V

VACT	vertical active area
VAHB	video advance high-performance bus
VBB	vertical back blank
VBI	vertical blanking interval
VBR	variable bit rate
VC	virtual channel
VCO	voltage controlled oscillator
VCOEF	vertical coefficient
VCXO	voltage control crystal oscillator
VDH	video decoder high definition
VEDU	video encoder unit
VER	version
VF	vertical filter
VFB	vertical front blank
VFMW	video firmware
VGA	video graphics array
VHB	video high-performance bus
VI	video input

VIC	vector interrupt controller
VID	VLAN ID
VIU	video input unit
VLAN	virtual local area network
VLC	variable length code
VLD	variable length decoding
VO	video output
VoIP	voice over IP
VDP	video display processor
VSD	video for standard definition
W	
W1C	write 1 to clear 0
WB	write buffer
WBC	write back channel
WC	write to clear
WDG	watchdog
WDT	watchdog timer
WFE	wait for event
WFI	wait for interrupt
WIP	write in progress
WO	write only
WRA	wrap
WRED	weighted random early drop
WRR	weighted round robin
WSS	wide screen signaling
X	
X2H	AXI bus translate into AHB bus
X2P	AXI bus translate into APB bus
Y	
YC	luma and chroma

YCbCr	YCbCr
YCbCr400MB	YCbCr400 macro block
YCbCr420MB	YCbCr420 macro block
YCbCr422	YCbCr422
YCbCr422MB	YCbCr422MB
YCbCr422MBH	YCbCr422 macro block horizontal
YCbCr422MBV	YCbCr422 macro block vertical
YCbCr444MB	YCbCr444 macro block
YCbCr888	YCbCr888
YUV	YUV
YUV400	YUV400
YUV420	YUV420
YUV422	YUV422
YUV444	YUV444

Z

ZME	zoom engine
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short