Application Report
08/2007, revised 05/2008

Minimum Hold Time on $\overline{SHUTDOWN}$ for TPA3123D2

Don Dapkus Applications Engineer – Audio Products

ABSTRACT

It has been reported that the TPA3120D2, TPA3122D2, and TPA3123D2 can enter a mode where no output signal is present, even though the SHUTDOWN-z terminal is held high. The root cause for this is if the start-up sequence of the IC is disrupted, the IC will get in a mode where no output is present. The way to prevent this is to insure the minimum negative-going pulse width applied to the SHUTDOWN-z terminal is at least 300 ms when using a 1 μF BYPASS capacitor.

PROBLEM ANALYSIS

The TPA3123D2 is a 25-W stereo single-ended output class-D amplifier. In order to eliminate pops and clicks, the IC has very complicated depop circuitry. This circuitry places some additional constraints on the system design.

When the TPA3123D2 is running normally, and the SHUTDOWN-z terminal is pulled low, the amplifier begins its shutdown sequence which is:

- MUTE the outputs (switching is commanded to 50% duty cycle)
- Discharge the BYPASS capacitor to ground thru a BYPASS voltage dependent current source
- Once the BYPASS voltage is discharged, stop the outputs from switching and enter the low-current shutdown mode

Under normal operation, if the TPA3123D2 is in shutdown the outputs are not switching. As the SHUTDOWN-z terminal is transitioned to logic high, the following start-up sequence occurs:

- A level-sensitive comparator looks for a rising of the SHUTDOWN-z terminal
- Once SHUTDOWN-z is high, start the outputs switching and slowly ramp the duty cycle to 50% to charge the output blocking capacitor without generating any pops using the modulated BYPASS voltage as a reference
- Once the BYPASS voltage reaches its final value (which corresponds to the outputs switching at 50% duty), a comparator triggers a latch which enables the channel to come out of MUTE and start playing audio

The problem can occur if the SHUTDOWN-z terminal is not asserted long enough for the BYPASS voltage to be partially discharged. Thus, when the SHUTDOWN-z terminal is pulled to logic high, the edge-triggered comparator on BYPASS never receives a rising edge (since BYPASS is still charged), and the IC ends up in a mode waiting for BYPASS to rise, even though BYPASS is already at its final value.

In order to prevent this problem, the minimum negative-going pulse width that can be applied to the SHUTDOWN-z is calculated as follows:

$$T_{PW} = 170\text{msec} + \text{CBYPASS}*20\text{k}\Omega$$

CONCLUSION

Normal operation will occur when a negative-going pulse of greater than 300 ms (nominal case for 1 μF BYPASS capacitor) is applied to the SHUTDOWN-z terminal.

TPA3121D2 and TPA3124D2 and later part numbers do not have the 300 ms restriction on the shutdown timing.