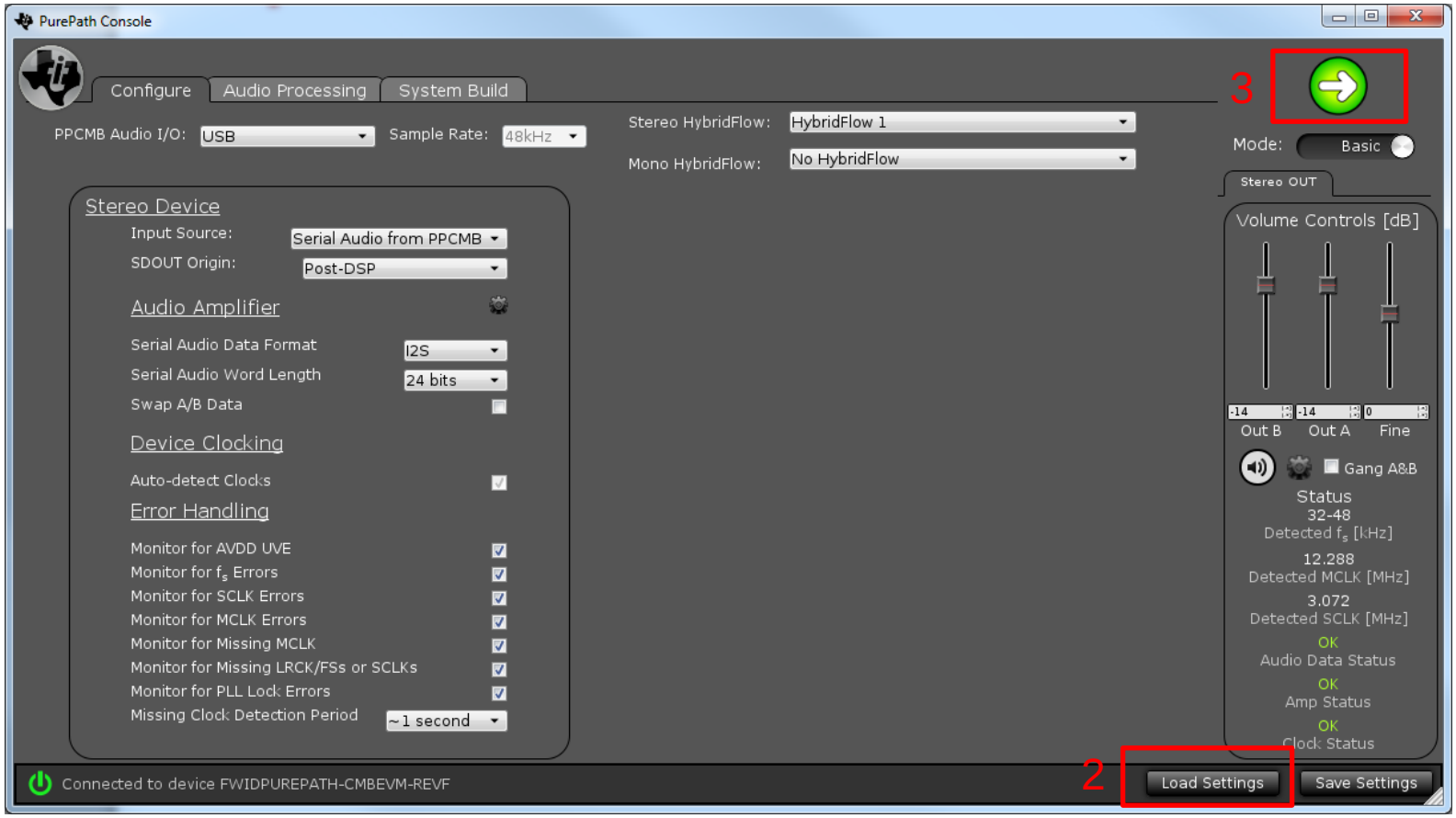
How to Dump CFG / Header File

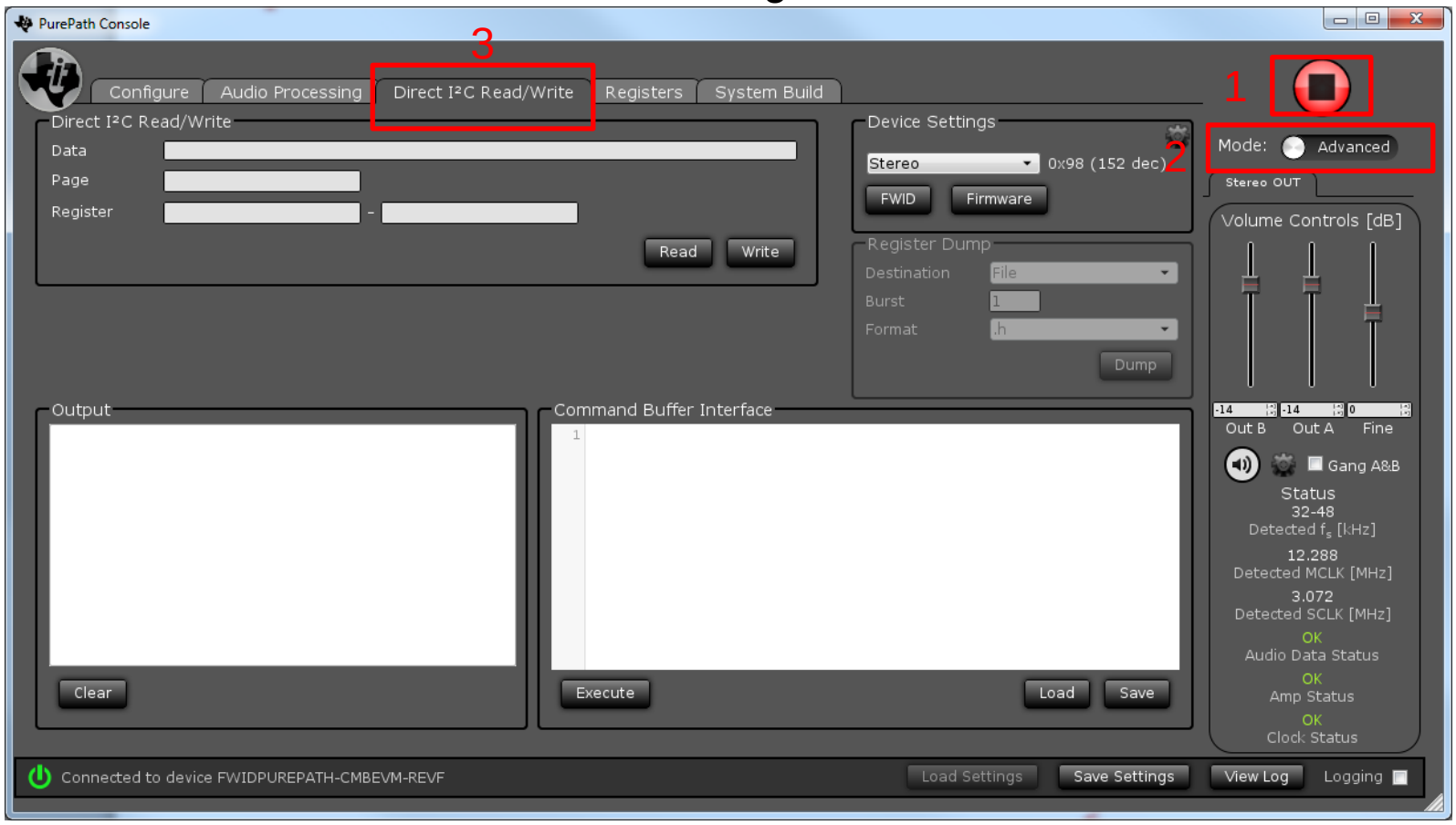
Step 1

1. Make sure PPCMB is connected to PC.
2. Load your xml file into PPC2.
3. Click download button to start running the hybrid flow.



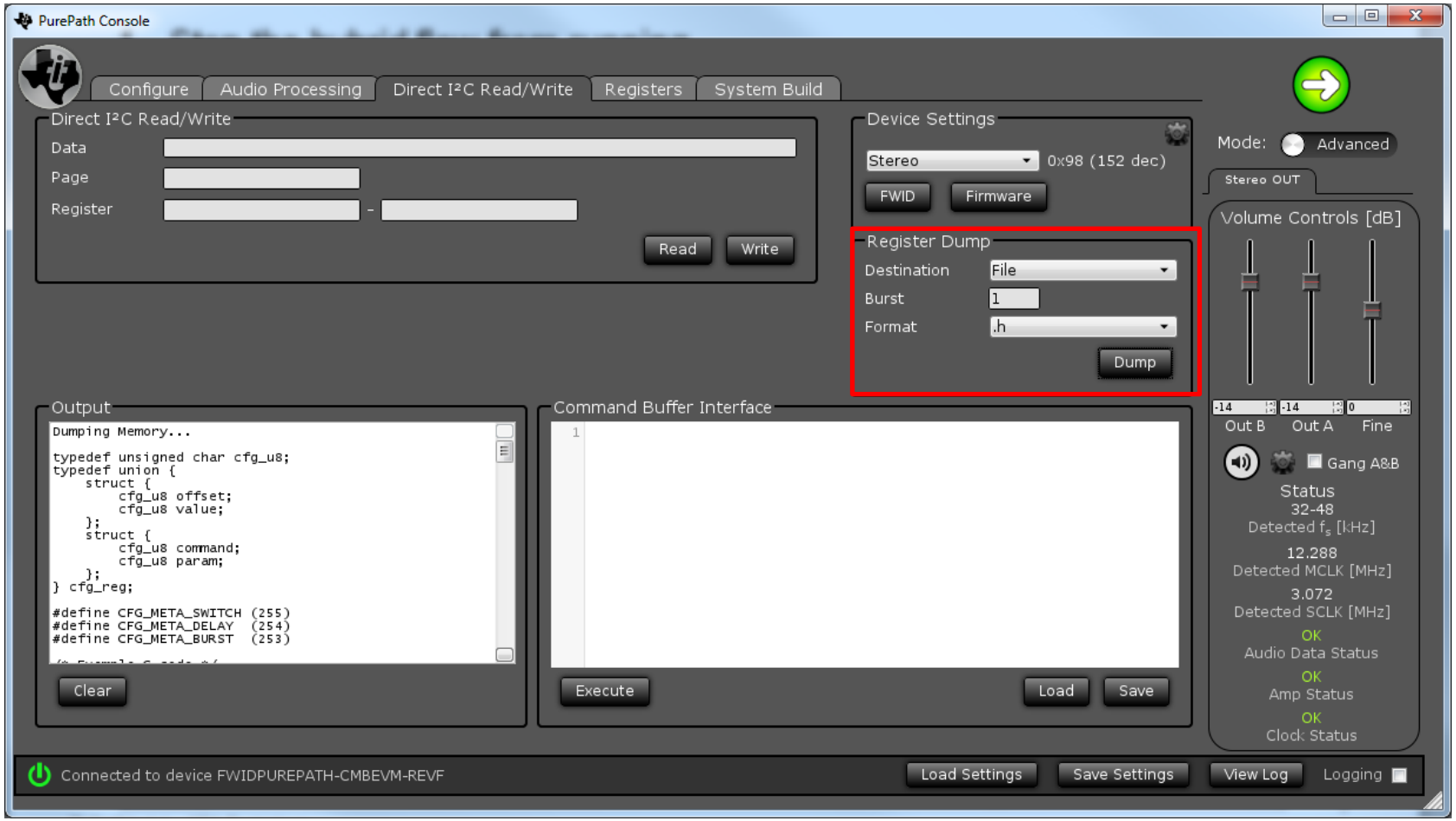
Step 2

1. Stop the hybrid flow from running.
2. Switch to Advanced mode.
3. Choose “Direct I2C Read / Wrte“ Page.



Step 3

1. Select the right destination, burst length and format in the Register Dump.
2. Click the dump button to start dumping.



Step 4

1. Fix the P0-R42 value if it is set to 0x00.

HF1_burst1_fix.cfg

```
64 w 98 19 00
65 w 98 1a 80
66 w 98 1b 00
67 w 98 1c 00
68 w 98 1d 00
69 w 98 1e 00
70 w 98 1f 04
71 w 98 20 00
72 w 98 21 00
73 w 98 22 00
74 w 98 23 01
75 w 98 24 00
76 w 98 25 00
77 w 98 26 f3
78 w 98 27 04
79 w 98 28 02
80 w 98 29 00
81 #w 98 2a 00    #Anglog Mute
82 w 98 2a 11
83 w 98 2b 1f
84 w 98 2c 00
85 w 98 2d 00
86 w 98 2e 00
87 w 98 2f 00
```

hf1-burst1_fix.h

```
100     { 0x22, 0x00 },
101     { 0x23, 0x01 },
102     { 0x24, 0x00 },
103     { 0x25, 0x00 },
104     { 0x26, 0xf3 },
105     { 0x27, 0x04 },
106     { 0x28, 0x02 },
107     { 0x29, 0x00 },
108     /*{ 0x2a, 0x00 },  Ananlog Mute */
109     { 0x2a, 0x11 },
110     { 0x2b, 0x1f },
111     { 0x2c, 0x00 },
112     { 0x2d, 0x00 },
113     { 0x2e, 0x00 },
114     { 0x2f, 0x00 },
115     { 0x30, 0x00 },
116     { 0x31, 0x00 },
117     { 0x32, 0x00 },
118     { 0x33, 0x00 },
119     { 0x34, 0x00 },
120     { 0x35, 0x00 },
121     { 0x36, 0x00 },
122     { 0x37, 0x00 },
123     { 0x38, 0x00 },
```

P0-R3 and P0-R42(0x2a)

8.4.2.3 P0-R3

Mute Channel B [4] (R/W)	00000000
This bit issues soft mute request for the Channel B. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - 0 - - - -
Mute	- - - 1 - - - -
Mute Channel A [0] (R/W)	**00000000**
This bit issues soft mute request for the Channel A. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - - - - - 0
Mute	- - - - - - - 1

8.4.2.29 P0-R42

Channel B DAC Data Path [5:4] (R/W)	00000001
These bits control the Channel B audio data path connection.	
Zero data (mute)	- - 0 0 - - - -
Channel B data	- - 0 1 - - - -
Channel A data	- - 1 0 - - - -
Reserved (do not set)	- - 1 1 - - - -
Channel A DAC Data Path [1:0] (R/W)	**00000001**
These bits control the Channel A audio data path connection.	
Zero data (mute)	- - - - - - 0 0
Channel A data	- - - - - - 0 1
Channel B data	- - - - - - 1 0
Reserved (do not set)	- - - - - - 1 1