Design Considerations

Digital Input Open loop Mid-Power Class-D Amplifiers

General Design Considerations

- **Reliability**
  - High Frequency Decoupling should be very close to device pin.
  - Capacitor Voltage rating ≈ 1.45 × PVDD
  - RC-Snubber should be as close as possible to the output pin.
  - BST cap path should be kept small.
- **Thermal**
  - Recommended Via Pattern (in datasheet) should be followed.
  - Have thermal vias around the IC GND pins.
  - Good connection between Thermal PAD & PCB.
  - Open spacing around the device close to GND pins.
  - When possible, use bottom layer as ground plane for thermal dissipation.
- **Other**
  - Impedance matching on digital signals.
  - GND isolation between adjacent traces.
  - Thick & short traces for outputs.

Design Considerations

- Recommended Layout TSSOP device:

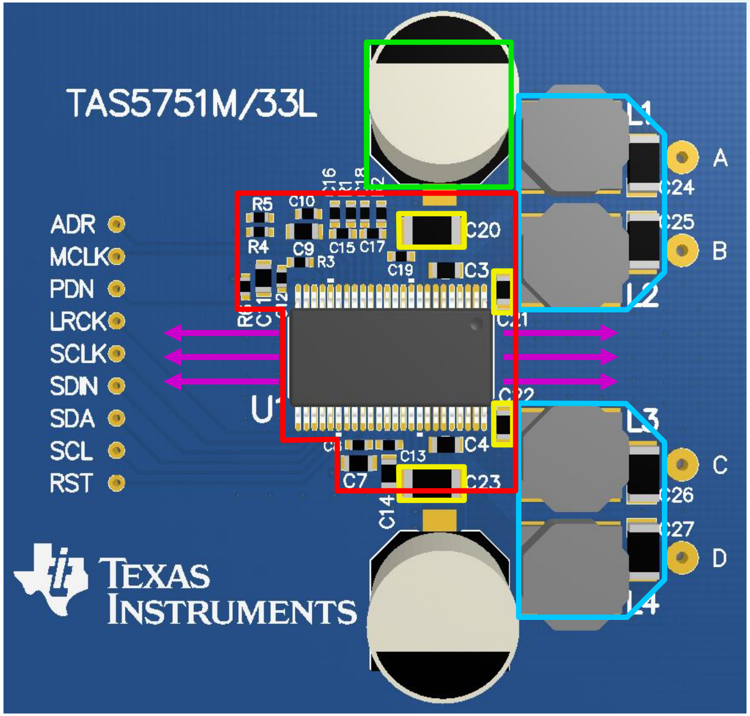
IC + base components

LC Filter

Bulk Capacitors

BST Capacitors

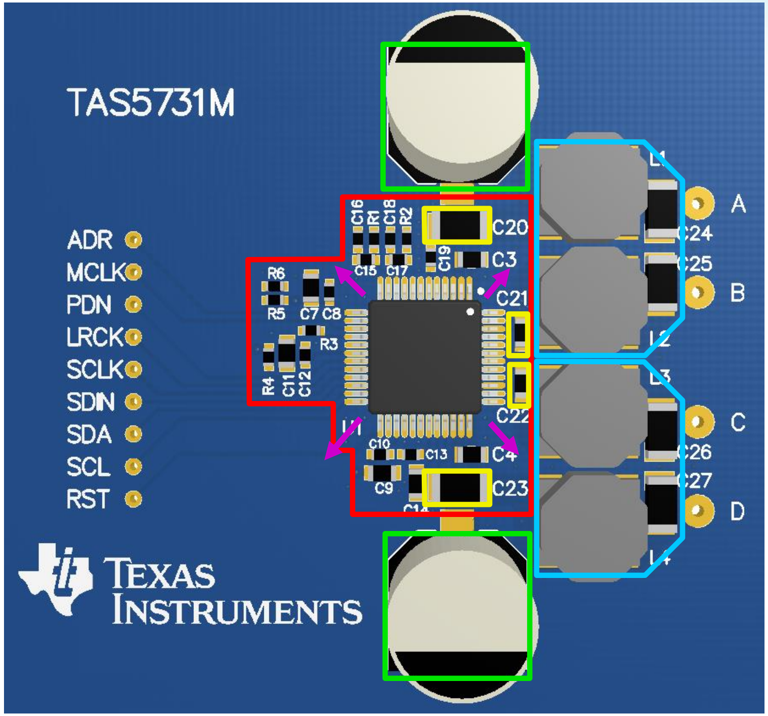
Thermal Flow



Design Considerations

- Recommended Layout QFP device:

- IC + base components
- LC Filter
- Bulk Capacitors
- BST Capacitors
- Thermal Flow

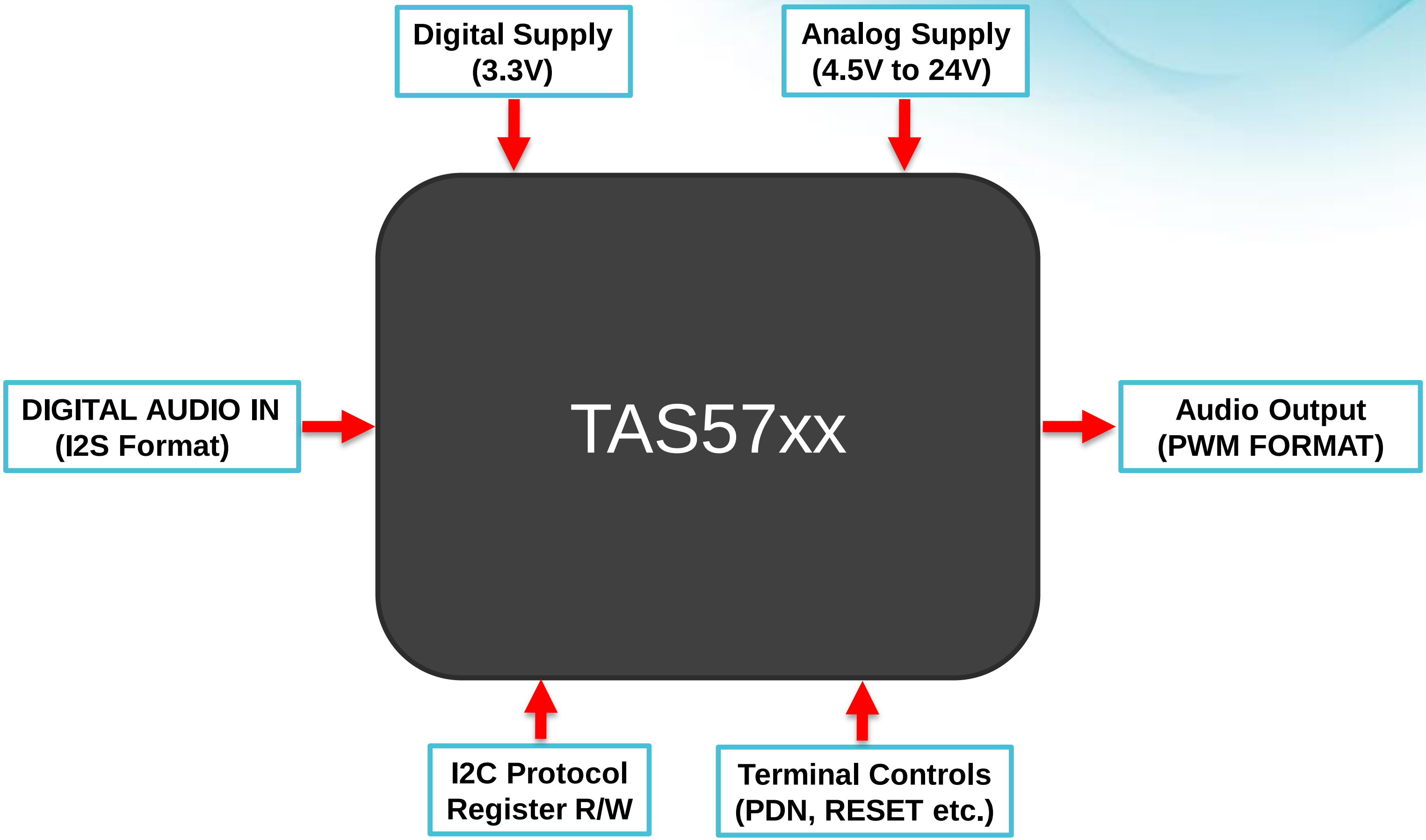


INTERNAL ONLY

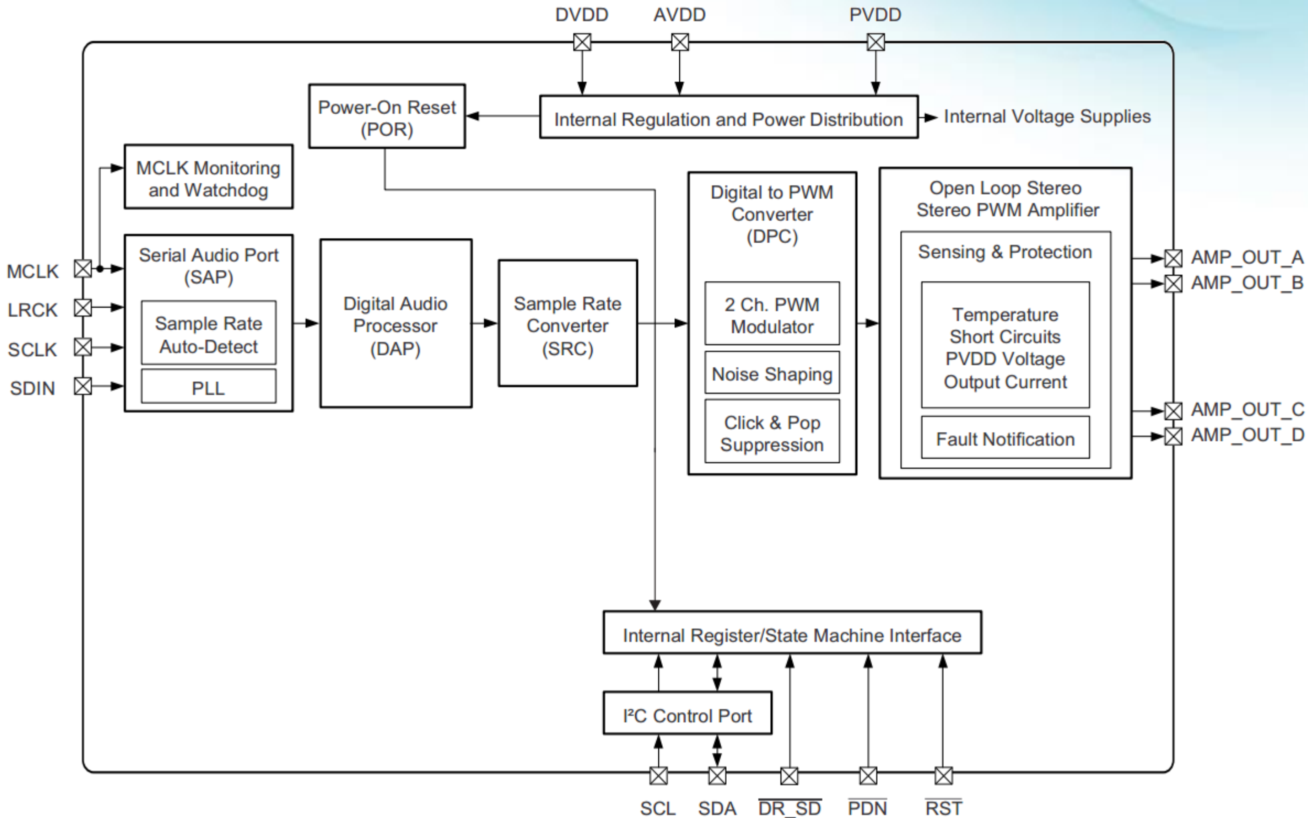
TAS57xx DAP Overview

Digital Input Open loop Mid-Power Class-D Amplifiers

Black Box View



TAS57xx Functional Block Diagram



TAS57xx Definition

- A Texas Instrument's **digital-input**, **medium-power** (10W to 50W) class of **efficient Class-D** audio amplifiers, which have a wide-range of digital **audio processing** capability. These are commonly found in TV's, Laptop's, Soundbars and other consumer gadgets

DAP Variations:

→ Fs Rate
  →Fs Min Supported 8KHz - 32KHz
  →Fs Max Supported 48KHz - 192KHz
→ SE Mode (2.1) support.
→ DRC/AGL Implementation (1-Band or 2-Band etc..)
→ No. of EQ's available per channel.
→ Ternary Modulation support.
→ Multiple I2C Slave Address support.
→ Sub-Woofer Channel.

Output-Stage Variations:

→ Architecture: Open-Loop or Closed-Loop
→RDs-ON
→ Supply Range
  → Min 4.5V - 12V
  → Max 18V - 26V
→Output-Power rating.
→ Pinout (48-Pin to 64-pin)
→ Package type (QFP, TSSOP)
→ Integrated Head-Phone.
→ Minimum Load Impedance.

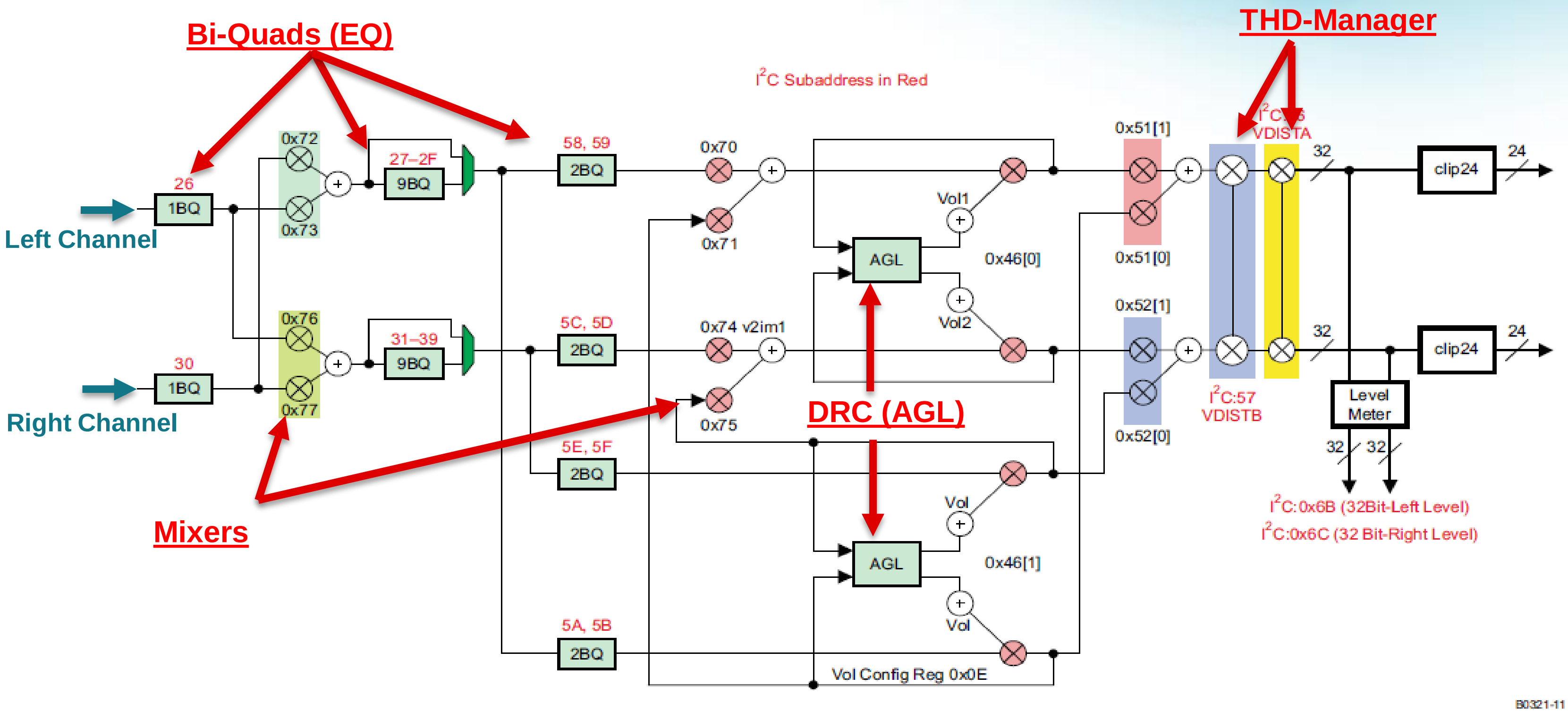
TAS57xx Digital Audio Processing

- **TAS57xx are I2C slave devices.**
  – Several TAS57xx devices have the option of multi-slave address, where the device address is set by a ASEL pin.
  – Standard (100KHz) & Fast (400KHz) I2C rates are supported.

- **TAS57xx devices have a fixed I2C register map.**
  – Registers are used to set the device in different configurations and configure the DAP flow.
  – Error-Register can be polled to check for any error conditions such as clock-error’s, Over Temperature, Over-Current, Under-Voltage etc..

- **TAS57xx devices mostly have a DAP**
  – Input Mixer, Bi-Quads, DRC, Output Mixer, THD Manager, etc..

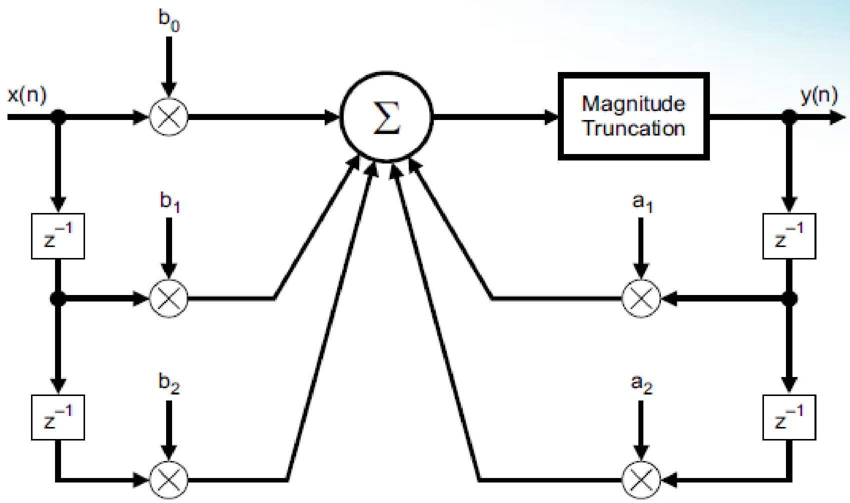
TAS57xx Example DAP flow



Bi-Quad (EQ) – Concept

- Digital Processing can be used to modify signal properties.
- Transformation is applied through digital filters. (Can be of two types, IIR & FIR).
- Transformation in digital domain is very attractive, since equivalent analog filter implementation would need several components (also subject to component tolerances)
- Very simply, the input x(n) is applied to a digital filter to yield output y(n). The Digital filter's transfer function determines the output y(n).
- A 2nd order IIR filter is referred to as a “Bi-Quad”- (short for Bi-Quadratic), which refers to the fact that the transfer function of 2nd order IIR filter is a polynomial of 2nd order.

Bi-Quad (EQ) – Formulae



$$y[n] = \underline{bo * x[n]} + \underline{b1 * x[n-1]} + \underline{b2 * x[n-2]} - \underline{a1 * y[n-1]} - \underline{a2 * y[n-2]}$$

$$Y(z) = b0 * x(z) + b1 * X(z)*Z^{-1} + b2 * X(Z)\, Z^{-2} - a1 * Y(Z) *Z^{-1} - a2 *Y(Z) * Z^{-2}$$

$$Y(z)/X(z) = H(z) = [\, (bo + b1*Z^{-1} + b2*Z^{-2})\,] / [\, (1 + a1*z^{-1} + a2*z^{-2})\,]$$

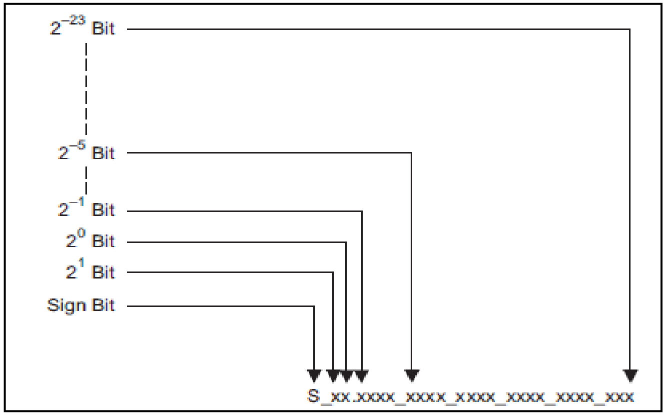
Bi-Quad (EQ) – Register Mapping

Experience your TI

- TAS5717 has dedicated registers to perform EQ-function for each Bi-Quad (14 Bi-Quads for each channel)
- Previously we saw that the transfer function of the digital filter determines the type of filtering applied.
- Basically, all we are looking to do is program the five coefficients a0, a1, b0, b1 & b2 to specify the type of filtering we require.
- An extract from the data-sheet for register 0x26 (corresponding to the 1st Bi-Quad on left-channel) is shown below. We notice that the length of the register is 20-bytes, spilt into 5-chunks (one for each coefficient).
- Further, note that the default value is a0=1 & all other coefficients = 0, which implies output y(n) = input x(n). (Note: Fixed Point Arithmetic)

0x26	ch1_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

Bi-Quad (EQ) – Coefficient Conversion



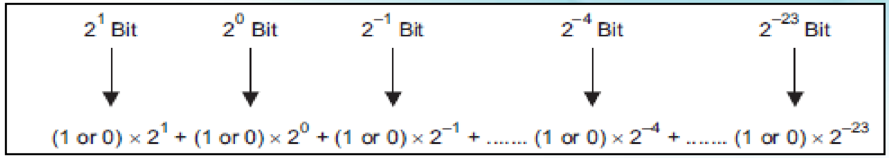
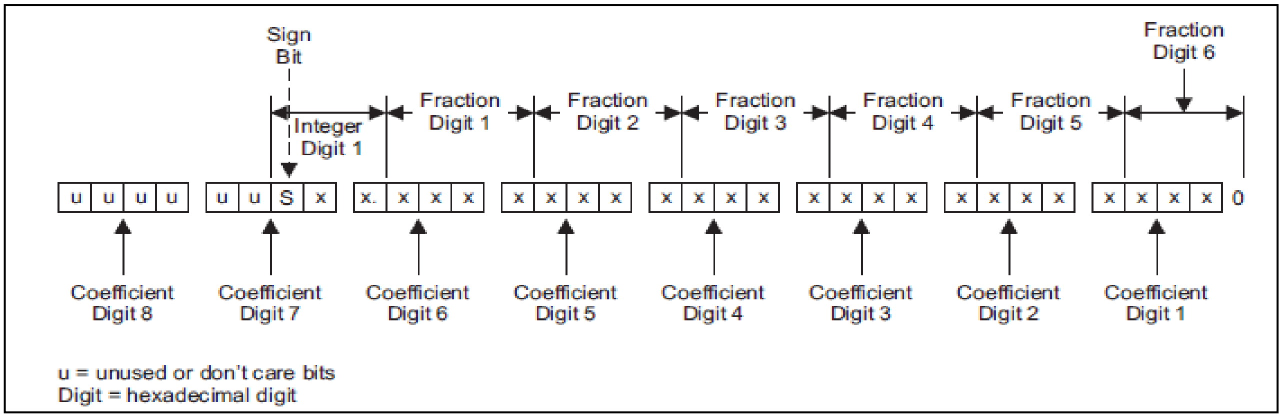


Table 1. Sample Calculation for 3.23 Format

db	Linear	Decimal	Hex (3.23 Format)
0	1	8,388,608	80 0000
5	1.77	14,917,288	00E3 9EA8
–5	0.56	4,717,260	0047 FACC
X	$L = 10^{(X/20)}$	D = 8388608 × L	H = dec2hex (D, 8)



Bi-Quad (EQ) – Use Case Examples

- **Some EQ-Use cases:**
  - Compensate speaker frequency response variations, and achieve a flat response.
  - Bass/Treble Boost or attenuation using shelving filter.
  - Notch filter to reject power-supply related hum noise (50Hz/60Hz) .
  - High-Pass (DC-block) and Low-Pass filtering.
    - This property is used in 2-band DRC to spilt the audio band into two bands (using high-pass & low-pass)

Bi-Quad (EQ) – response of a TV speaker.

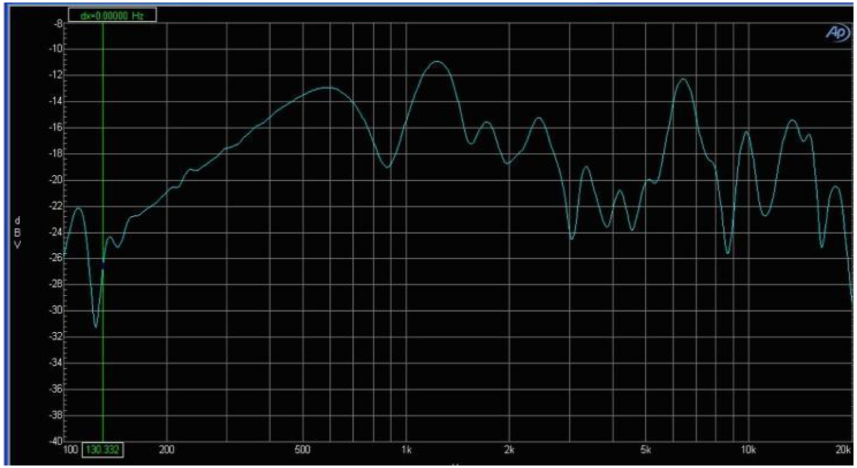


Image-Source: http://i.cmpnet.com/audiodesignline/2008/03/qft_fig1.jpg

→ Choice of TV speakers is driven by cost & space considerations.

→ As seen in this plot, speaker response typically varies a lot across audible frequency range.

→ This can significantly impact the perceived audio-quality,. (High-end , good quality speakers are typically ones with a maximally flat-response.)

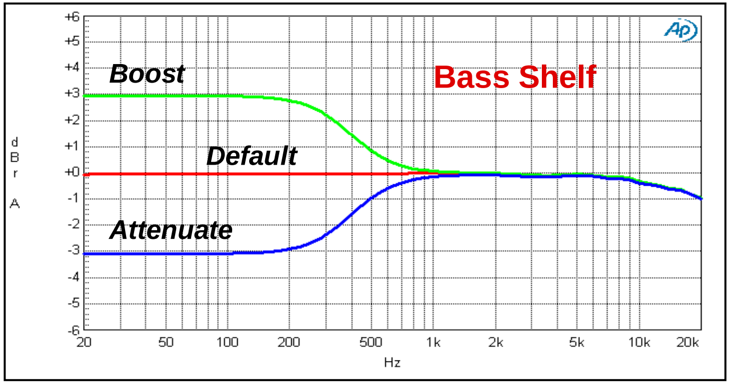
→ Using Auto-Eq, tool the inverse response & corresponding register coefficients can be generated.

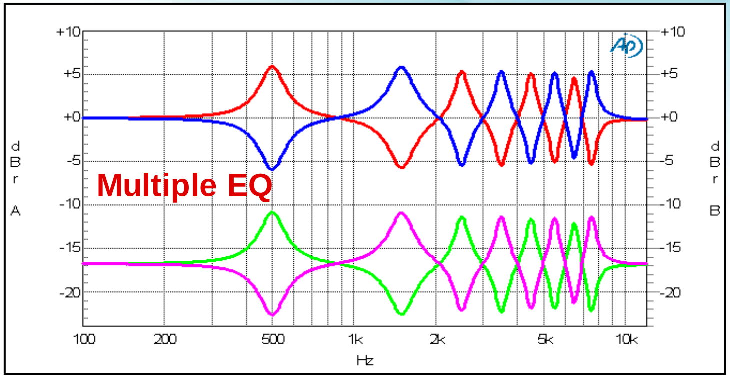
Bi-Quad (EQ) – response of a TV speaker.

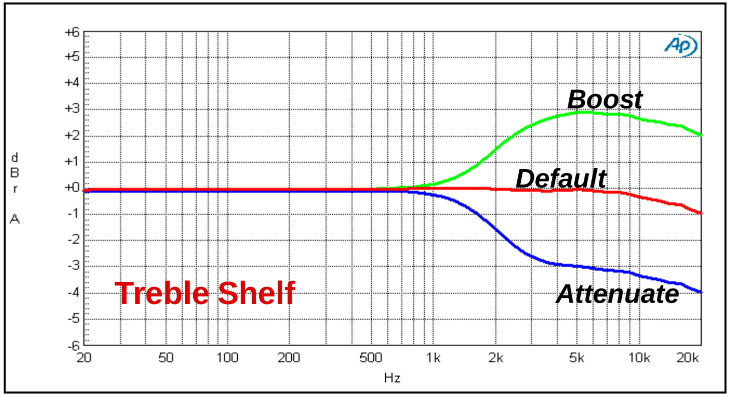
- The Ideal frequency response of a speaker is a flat line from 20Hz to 20KHz.
  - However, real-world speakers have a widely varying frequency response.
  - The audio output from these speakers without any audio processing is usually not of the highest perceived quality, as many frequencies can be attenuated.

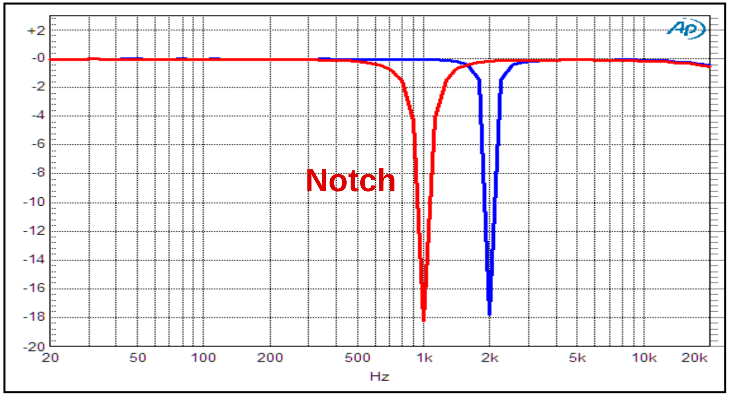
- The process of compensating the speaker-response to make it close to a desired response is called “Equalization” or “EQ”. Some use-cases
  - Compensate speaker frequency response variations, and achieve a flat response.
  - Bass/Treble Boost or attenuation using shelving filter.
  - Notch filter to reject power-supply related hum noise (50Hz/60Hz) .
  - High-Pass (DC-block) Low-Pass filtering.

Bi-Quad (EQ) – Example Plots

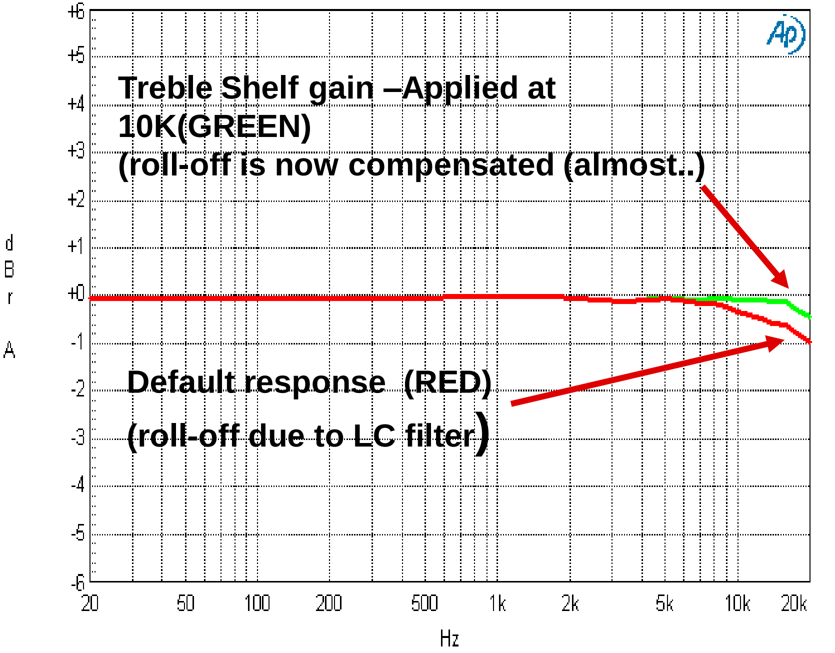




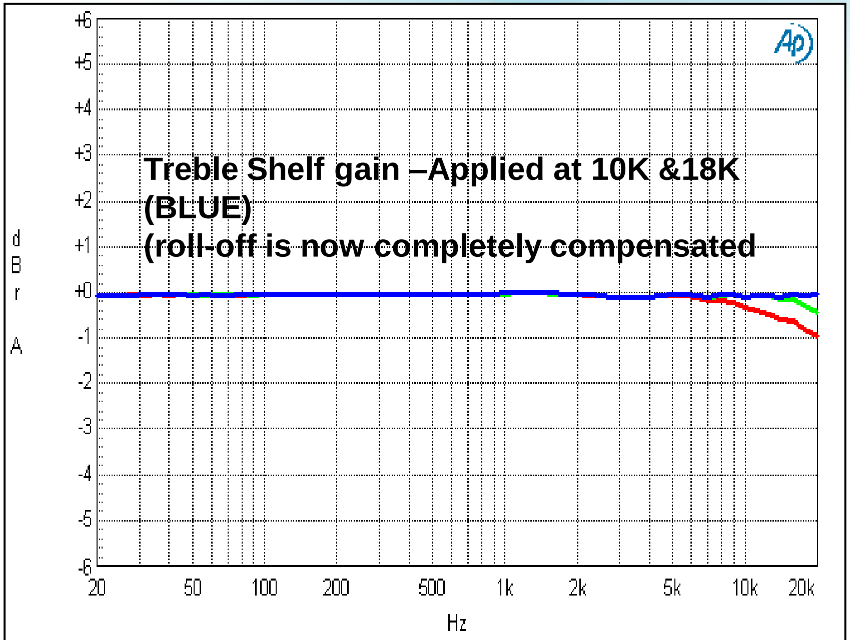




Bi-Quad (EQ) – Compensating roll-off



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Anlr.Level A	Left	Default
2	1	Green	Solid	3	Anlr.Level A	Left	10K_0.5dB_TShelf



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	3	Anlr.Level A	Left	Default
2	1	Green	Solid	3	Anlr.Level A	Left	10K_0.5dB_TShelf
7	1	Blue	Solid	3	Anlr.Level A	Left	(10K_0.5dB) + (18K_0.5dB)

DRC/AGL

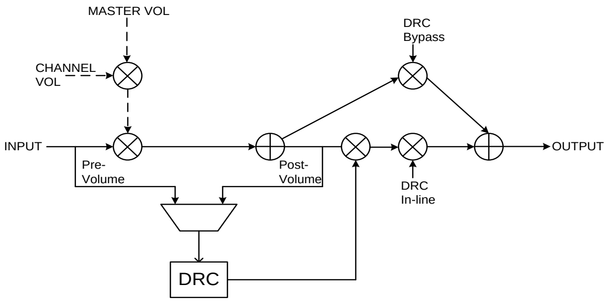
Experience your TI

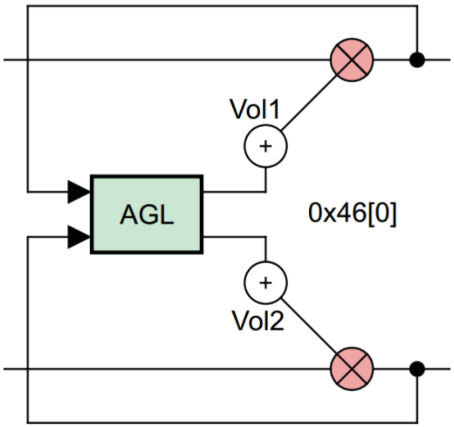
- **What is Dynamic Range?**
  - Difference between Max Signal & Min Signal. (i.e. Peak – Noise).
  - DRC is then simply the process of compressing this range.

- **Why compress the range?**
  - Prevent Clipping & Distortion.
  - Protection of speaker, from damage due to large transients.

- **What is multi-band DRC?**
  - Audio band is 20Hz to 20KHz. Simplest form of DRC is single-band DRC.
  - However, in 1-band DRC, compression is applied over the entire audio band (Bass, Mid & High frequency regions).
    - For example, if an explosion sound (bass freq) is compressed, then mid-band (dialogue) also gets compressed.
  - For better control, multi –band DRC can be implemented, where the audio is split into different bands. Each band has its dedicated DRC block.
  - The different bands are therefore are decoupled from compression processing of the other.

DRC AND AGL COMPARISON

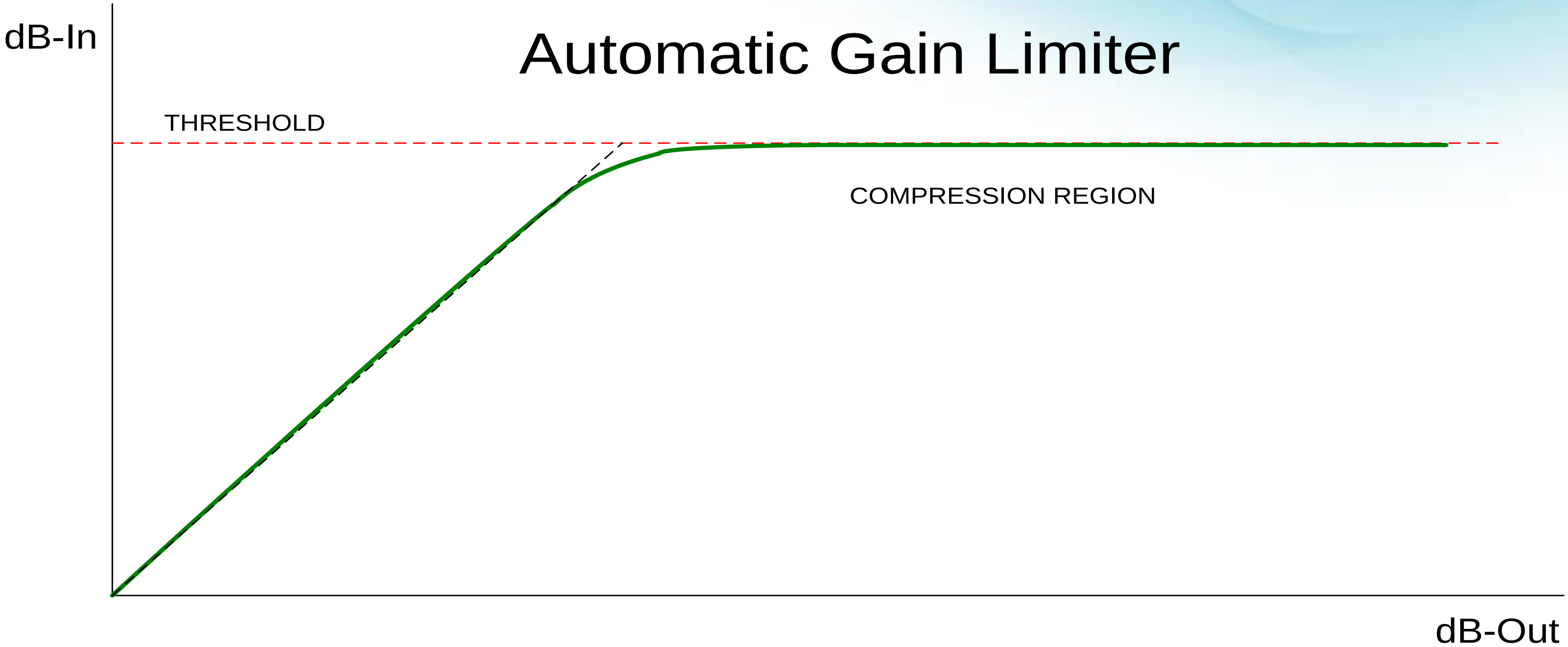




DRC
- Feed-forward
- Adjustable compression ratio
- Settings:
    - Threshold
    - Compression ratio
    - Energy filter
    - Attack time
    - Release time

AGL
- Feed-back
- Fixed compression ratio
- Settings:
    - Threshold
    - Softening filter
    - Attack time
    - Release time

COMPRESSION WITH AGL



- DRC: TAS5731M-TAS5711
- AGL: TAS5751M-TAS5733L

AGL FORMULA

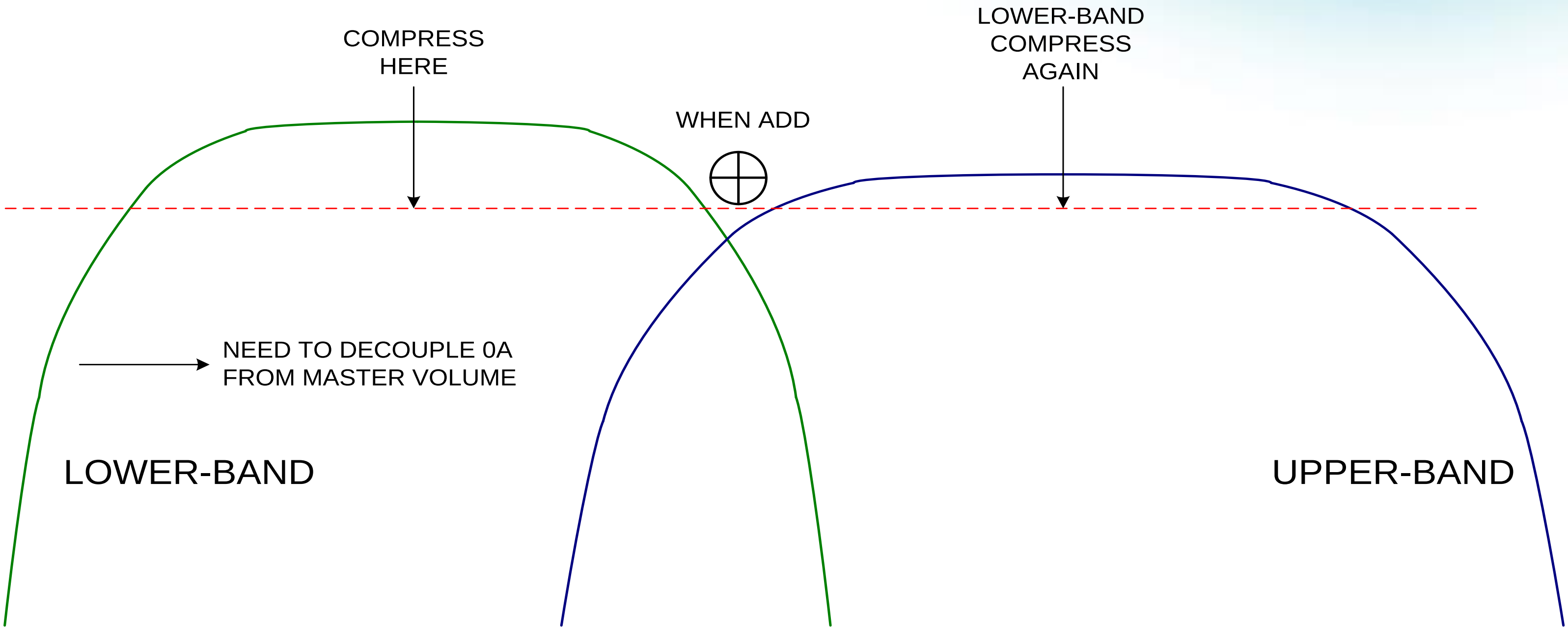
- **SOFTENING FILTER ALPHA (AEA)**
  - DRC1 (lower-band) AEA is 3B. Upper 4 bytes are AEA. Lower 4 bytes are AEO.
  - DRC2 (upper-band) AEA is 3E. Upper 4 bytes are AEA. Lower 4 bytes are AEO.
  - AEA = 1 – e^(-1000/(fs* User_AE)) --- 3.23 format
  - e ~ 2.718281828
  - Fs = sampling frequency
  - User_AE = duration in mS – user input
- **SOFTENING FILTER OMEGA (AEO)**
  - AEO = 1 – AEA --- 3.23 format
- **ATTACK RATE**
  - Attack and release rates are programmed in 3C for lower-band DRC1 and 3F for upper-band DRC2. Upper 4 bytes are AA.
  - Attack rate = 2*(AA + Release rate) --- 9.17 format
  - AA = 1000*User_Ad/Fs
  - User_Ad = attack duration in mS – user input
- **RELEASE RATE**
  - Attack and release rates are programmed in 3C for lower-band DRC1 and 3F for upper-band DRC2. Lower 4 bytes are Release Rate.
  - Release rate = 1000*User_Rd/Fs --- 9.17 format
  - User_Rd = release duration in mS – user input
  - NOTE: The release duration (User_Rd) should be longer that attack duration (User_Ad)
- **ATTACK THRESHOLD**
  - Attack threshold is programmed in 40 for lower-band DRC1 and 43 for upper-band DRC2.
  - When the signal is below the threshold, ALG is not applied. When the signal is above the threshold AGL is applied.
  - Attack Threshold = dB level – user input --- 9.23 format

Two-Band DRC/AGL

- By using a high-pass filter, audio signals above a “cut-off” value can be passed – lets call it band-1. By using a low-pass filter at the <u>same</u> cut-off frequency, the other band (band-2) can be passed.

- This cut-off frequency is called **crossover-frequency**, and the two bands can now be processed separately with independent DRC settings *(The high-pass & low-pass filters are implemented by using dedicated Bi-Quads.)*

WHY DECOUPLE VOLUME – SERIES



PROCEDURES – 2 BANDS

- Determine crossover
- Check THD+N at operating set points: PVDD, load, 0dBFS, 0dB gain – record power and THD+N
- Choose parallel or series
- Change to maximum system gain
- Either small attack time (little steps) and large softening time (long integration time) or large attack time (many steps) and small softening time (short integration time)

ADJUSTING HIGHER BAND

- Set input to 1kHz
- Turn on compression – AGL
- Turn off Softening filter – oscillation
  - 00 08 00 00 00 00 00 00 (α = 1 and ω = 1 – α)
- Adjust the attack time
- Adjust the release time
- Adjust the pre and/or post scales if necessary
- Add softening filter
- Tuning AGL is similar to tuning EQ – it will take time

ADJUSTING LOWER BAND

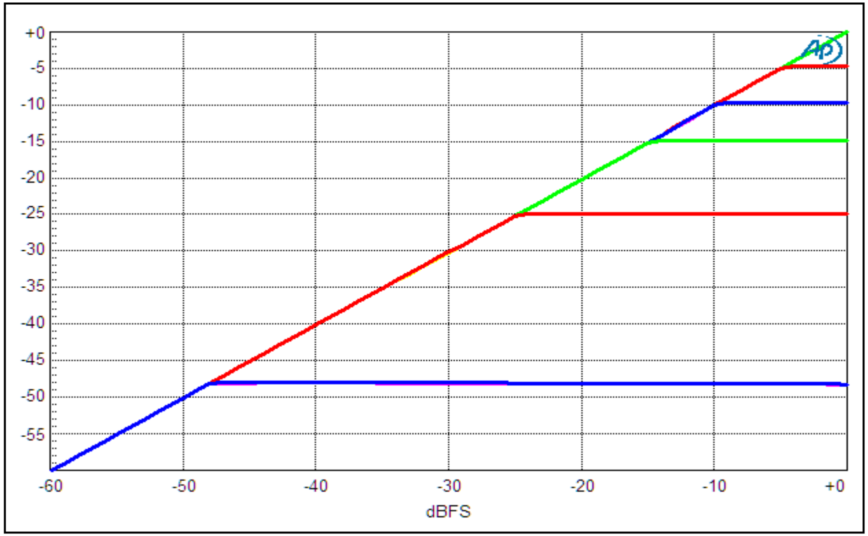
- Set input to 100 Hz
- Turn on compression – AGL
- Turn off Softening filter – oscillation
  - 00 08 00 00 00 00 00 00 (α = 1 and ω = 1 – α)
- Adjust the attack time
- Adjust the release time
- Adjust the pre and/or post scales if necessary
- Add softening filter
- Tuning AGL is similar to tuning EQ – it will take time

Elements of DRC

- TAS57xx implementation of DRC in the form of AGL, (Automatic Gain Limiter).
- The different settings of DRC control are:
  - Threshold (Value beyond which audio is compressed/limited)
  - Attack time (Step-Size, i.e. time DRC takes to reach threshold)
  - Release time (Step-Size, i.e. time DRC takes to reach threshold)
  - Softening filter (Sharpness of the compression-knee)

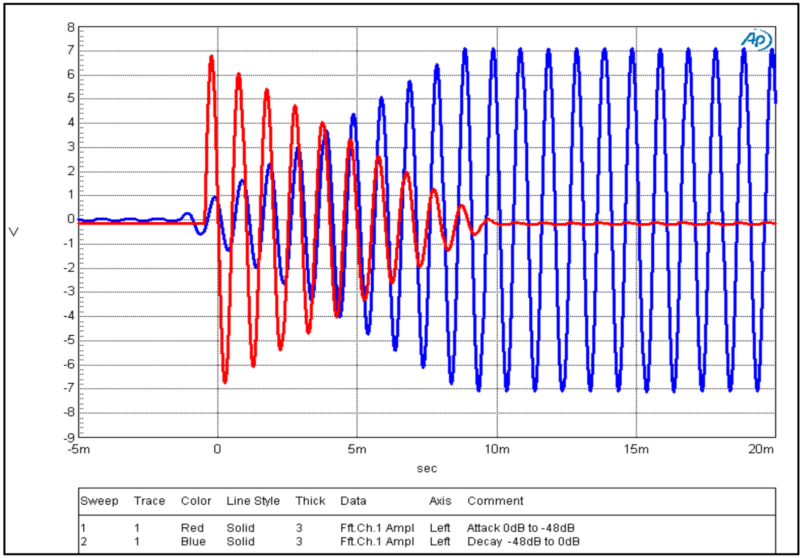
DRC - Threshold

- Plot shows the output level (y-axis) vs. input level (x-axis).
- With no DRC, the line is a 1:1 ratio, all the way upto full-scale input.
- Different threshold settings are plotted, at each threshold level, the output can be seen to be limited.



DRC - Attack & Decay time

- Plot below shows DRC attack (RED) & decay (BLUE).
- For attack case, a very low threshold was set (-40dB or lower??), and then a large audio signal was provided. The DRC compresses the audio to threshold level in ~10ms.
- After audio was in this compression range, threshold was instantaneously raised to 0dB. The DRC immediately starts releasing (BLUE) and audio reaches full level in ~10ms

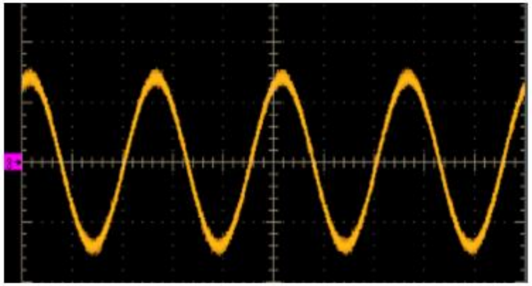


FINAL ADJUSTMENTS

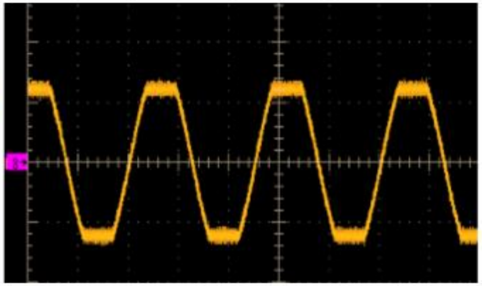
- Listening test
- Fine tune – small changes to:
  - Scales
  - Attack time
  - Softening time
  - Release time

THD Manager (Pre and Post Scaling)

- The THD manager can be used to achieve digitally the specified THD levels without voltage clipping.
- This allows user to achieve the same THD (for example, 10% THD) for different power levels (15 W/10 W/5W) with same PVCC level.



PVDD = 15.7 V
P_O = 6 W
No Clipping



PVDD = 15.7 V
P_O = 6 W
Clipped (10% THD)

Pre-Scaler (Reg. 0x57) is used to achieve clipping.
Post-Scaler (Reg. 0x56) is used to scale power-level at desired clipping.

THD Manager: AGL/DRC Re-tuning

- At 0dBFs (max input signal volume of system) enable AGL/DRC
- Check if AGL/DRC is engaged
- If not engaged increase the channel gain (before AGL/DRC block) until AGL/DRC becomes engaged (it most likely would be engaged)
- Once engaged adjust AGL/DRC threshold until desire level is achieved

Mixers

- Mixers are configured by selecting the gain that each input will be contributing to the mixed signal. this gain is set with a coefficient that ranges from 0 (no input) to 1 (full input). This coefficient must be written into the register in 3.23 format:

  - 0 → 0x 00 00 00 00
  - 1 → 0x 00 80 00 00
  - 0.5 → 0x 00 40 00 00