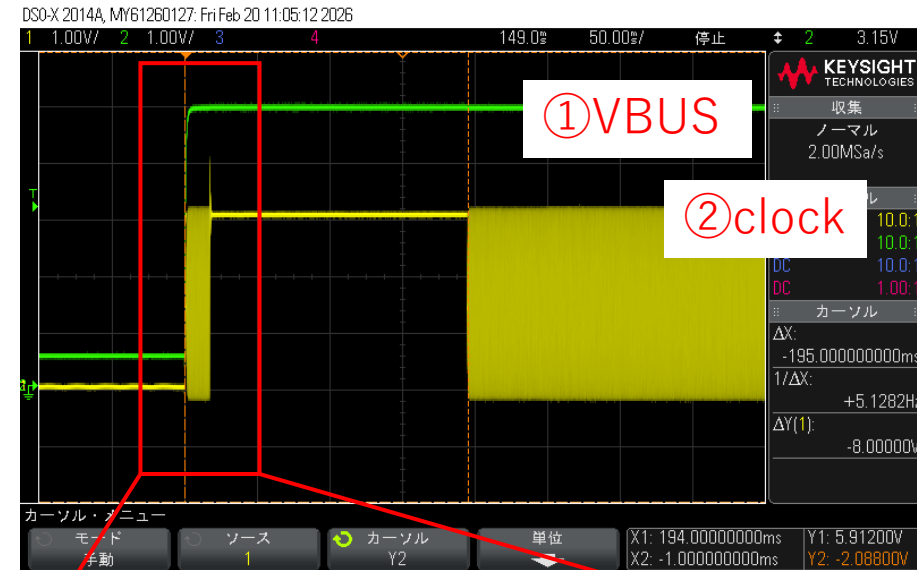
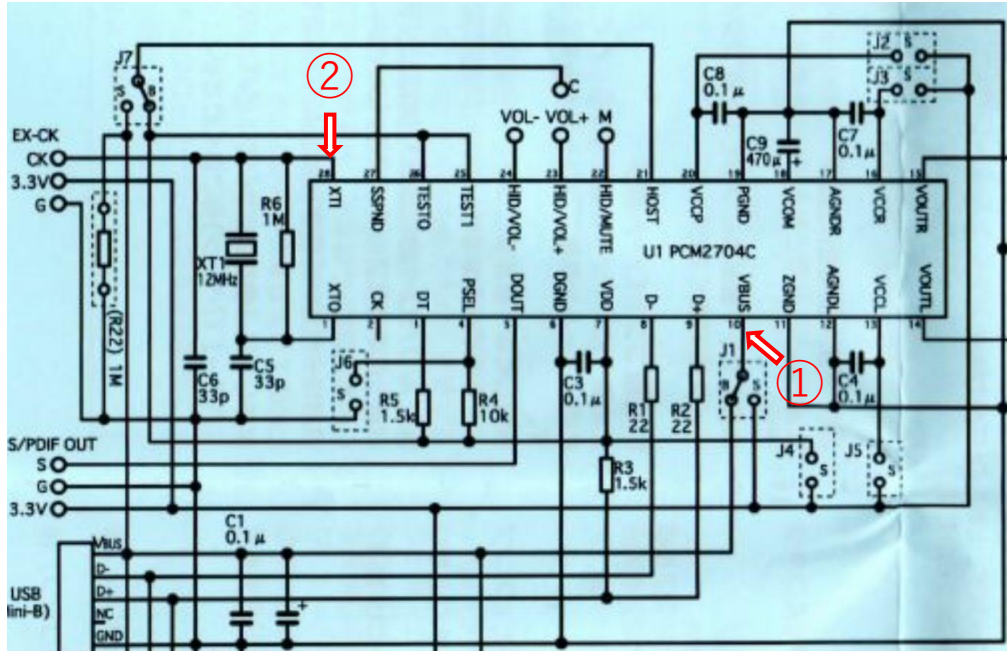
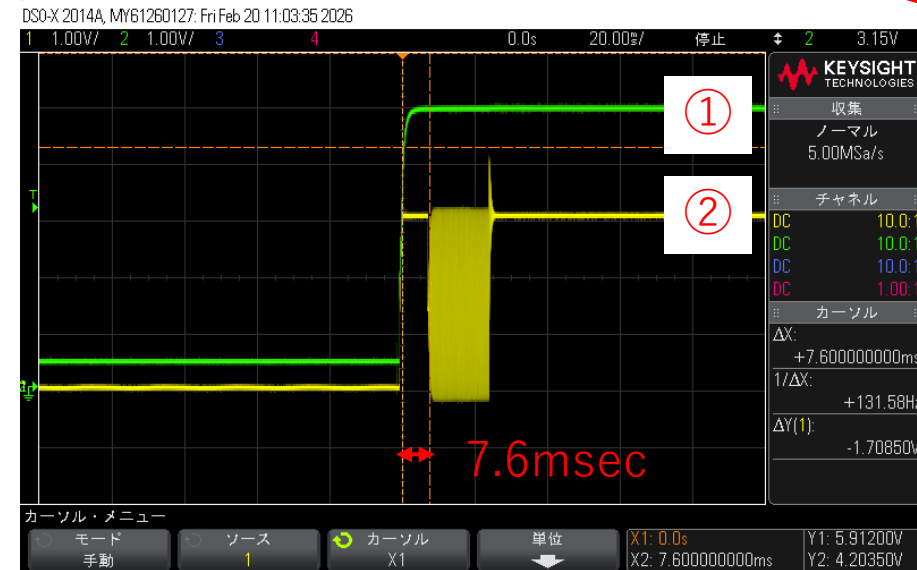


Rising up behavior of crystal resonator

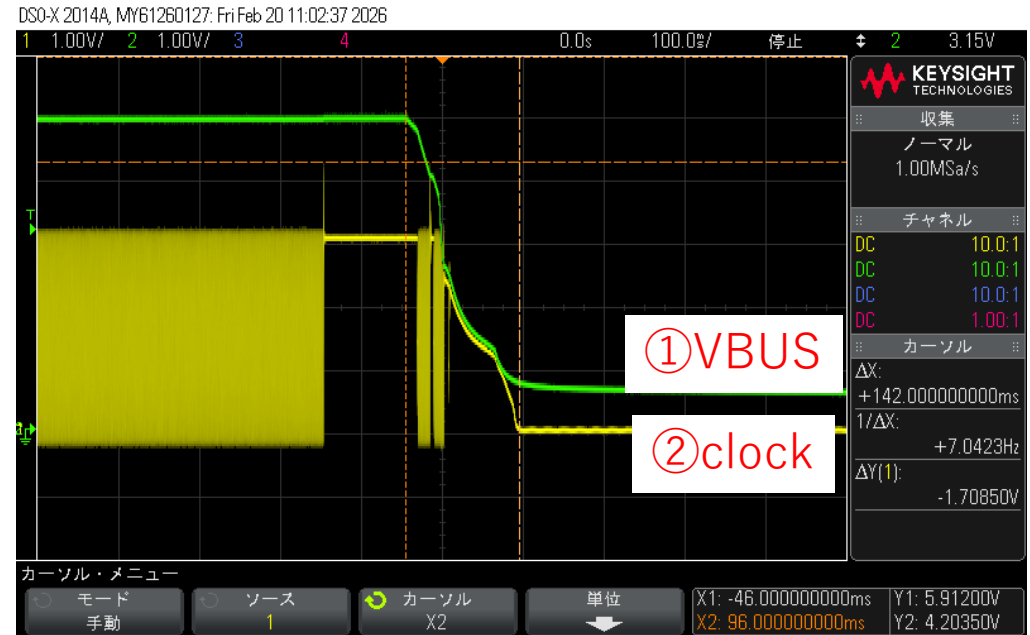
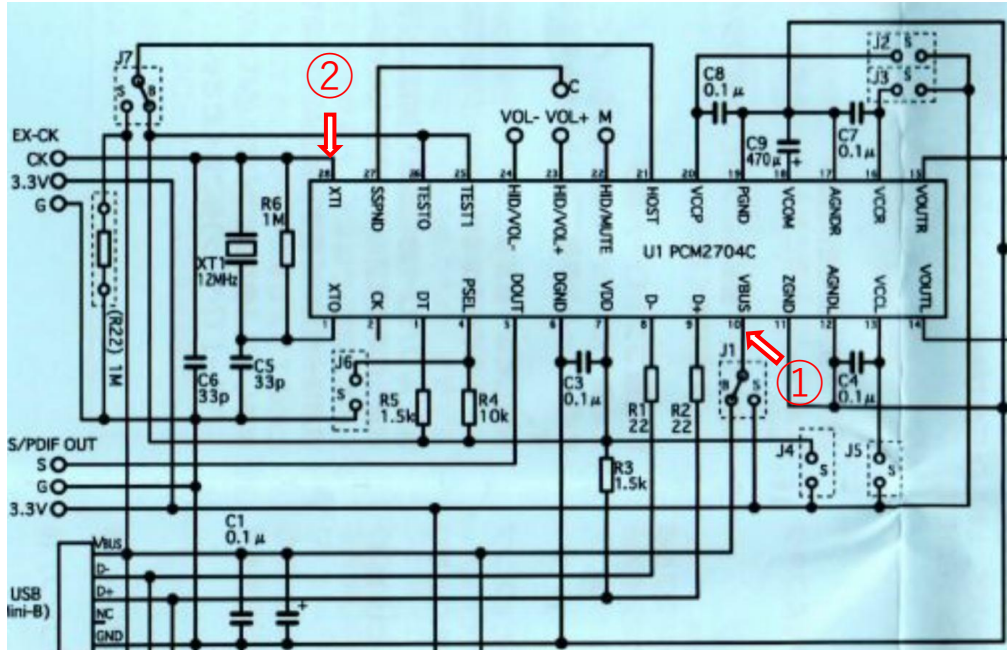


Question 1)
 the case of Power-ON, 7.6msec after VBUS rising up,
 clock start to generate and stop for the moment then
 start again.
 Does this behavior correct?

According to the datasheet, internal reset is 700us.
 Should clock be started before internal reset release?



Rising down behavior of crystal resonator



Question 2)

the case of Power-OFF, before VBUS rising off, clock stop for a moment then start again.

Does this behavior correct?