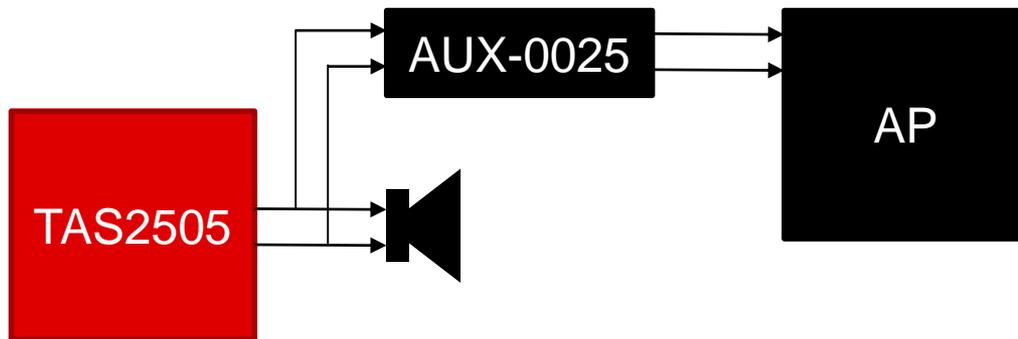


TAS2505 Test Setup

Applications Engineering
January 2024

Analog Input Test Setup

- AP configuration:
 - Analog balanced output 1 CH.
 - Analog balanced input 1 CH, AES17 (20 kHz) low-pass.
- EVM HW configuration:
 - SPKP & SPKM connected to speaker or test load.
 - AUX-0025 filter connected in parallel to the load, and then to AP input.
 - + output from AP connected to LEFT IN (black jack)
 - - output from AP connected to RIGHT IN (red jack)



Analog Input Test Setup

- EVM SW configuration:
 - Enable AINL & AINR. P0x01 R0x09 = 0x03.
 - Route AINL to MixerP & AINR to MixerM. P0x01 R0x0c = 0x90 or 0x60.
 - Unmute Class-D. P0x01 R0x30 = 0x10.
 - Enable Class-D. P0x01 R0x2d = 0x02.

w 30 00 01

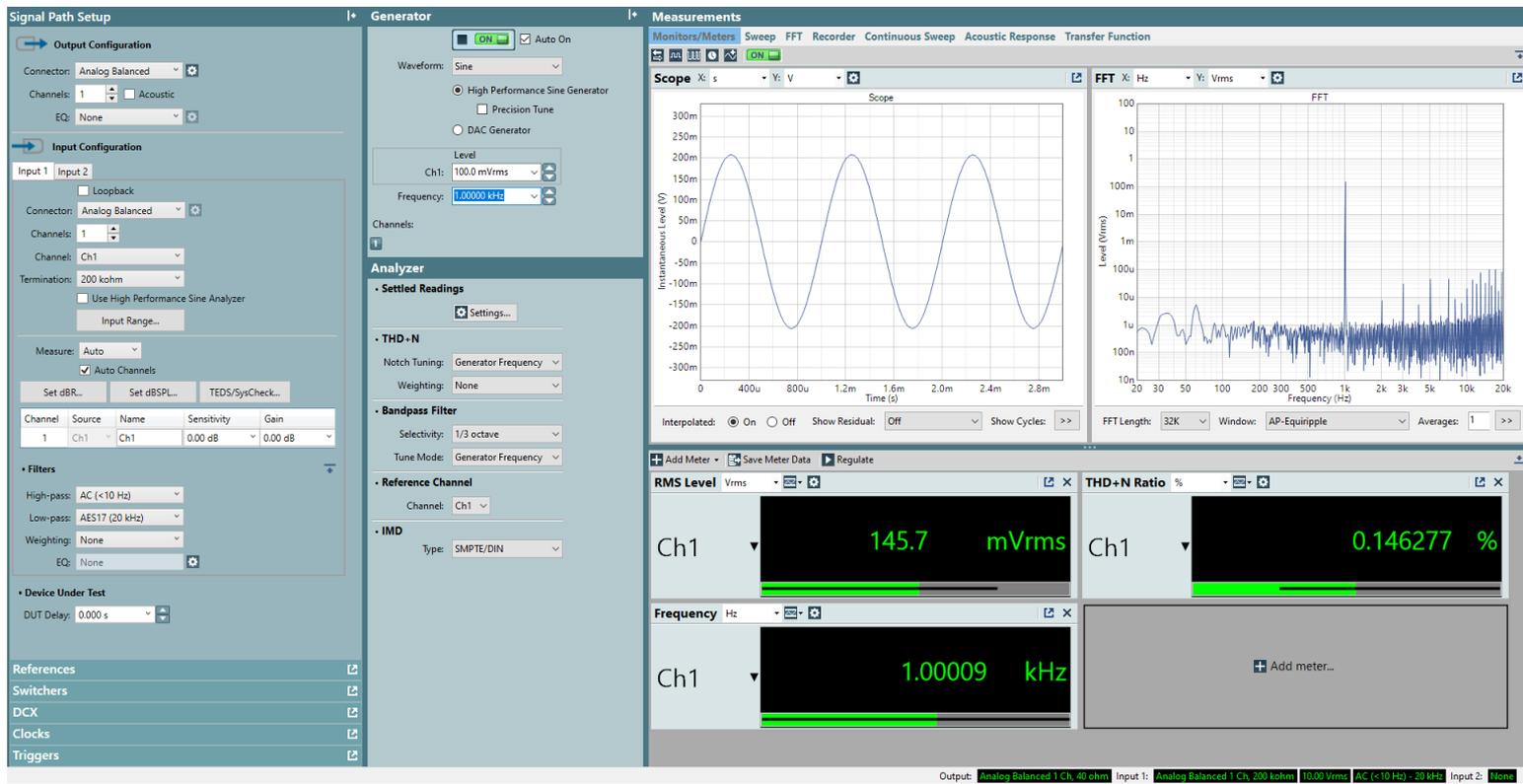
w 30 09 03

w 30 0c 90

w 30 30 10

w 30 2d 02

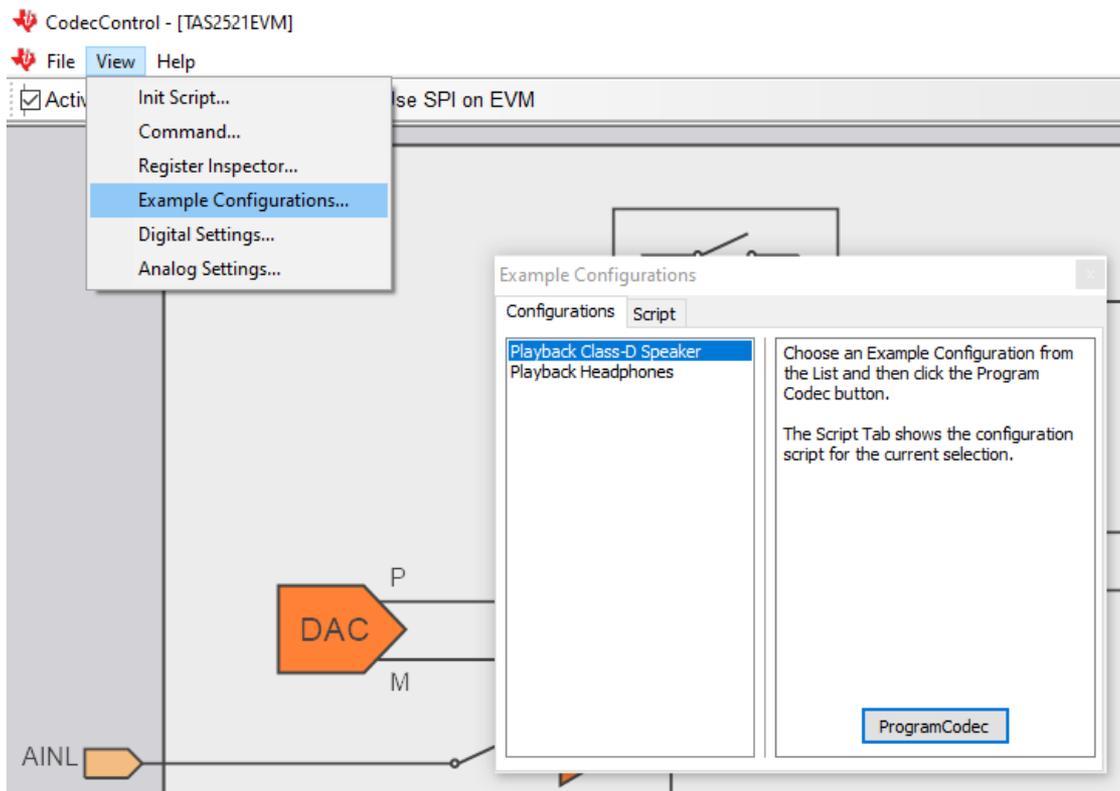
Analog Input Test Result



Digital Input Test Setup

- AP configuration:
 - Digital serial output. 2CH, I2S format, MCLK output as 12.288MHz, 3.3V, 48kHz frame rate, 32bit word width
 - Analog balanced input 1 CH, AES17 (20 kHz) low-pass.
- EVM HW configuration:
 - SPKP & SPKM connected to speaker or test load.
 - AUX-0025 filter connected in parallel to the load, and then to AP input.
 - MCLK, BCLK, FSYNC and DATA1 connected to J6, J7, J9 and J10.
- EVM SW configuration:
 - View -> Example Configurations... -> Playback Class-D Speaker -> ProgramCodec

Digital Input Test Setup



Digital Input Test Setup

Output Settings (Digital Serial Transmitter)

Configuration: Serial Transmitter Open... Save...

• Audio

Single Data Line (TDM)
 Multiple Data Lines

Channels: 2 MSB First

Format: I2S

Justification: Left Justified

Frame Pulse: One Subframe

Frame Clk: Invert Shift Left

Word Width: 32

Bit Depth: 24 Dither

• Clocks

Master Clk Source: Internal

Master Clk Rate: 12.2880 MHz

MClk Output: On Invert

Bit & Frame Dir: Out

Frame Clk Rate: 48.0000 kHz

MClk/FClk Ratio: 256

• Bit Clock Edge Sync

Outs: Rising

Ins: Rising

• Logic

Level: 3.3 V

Outputs: ON

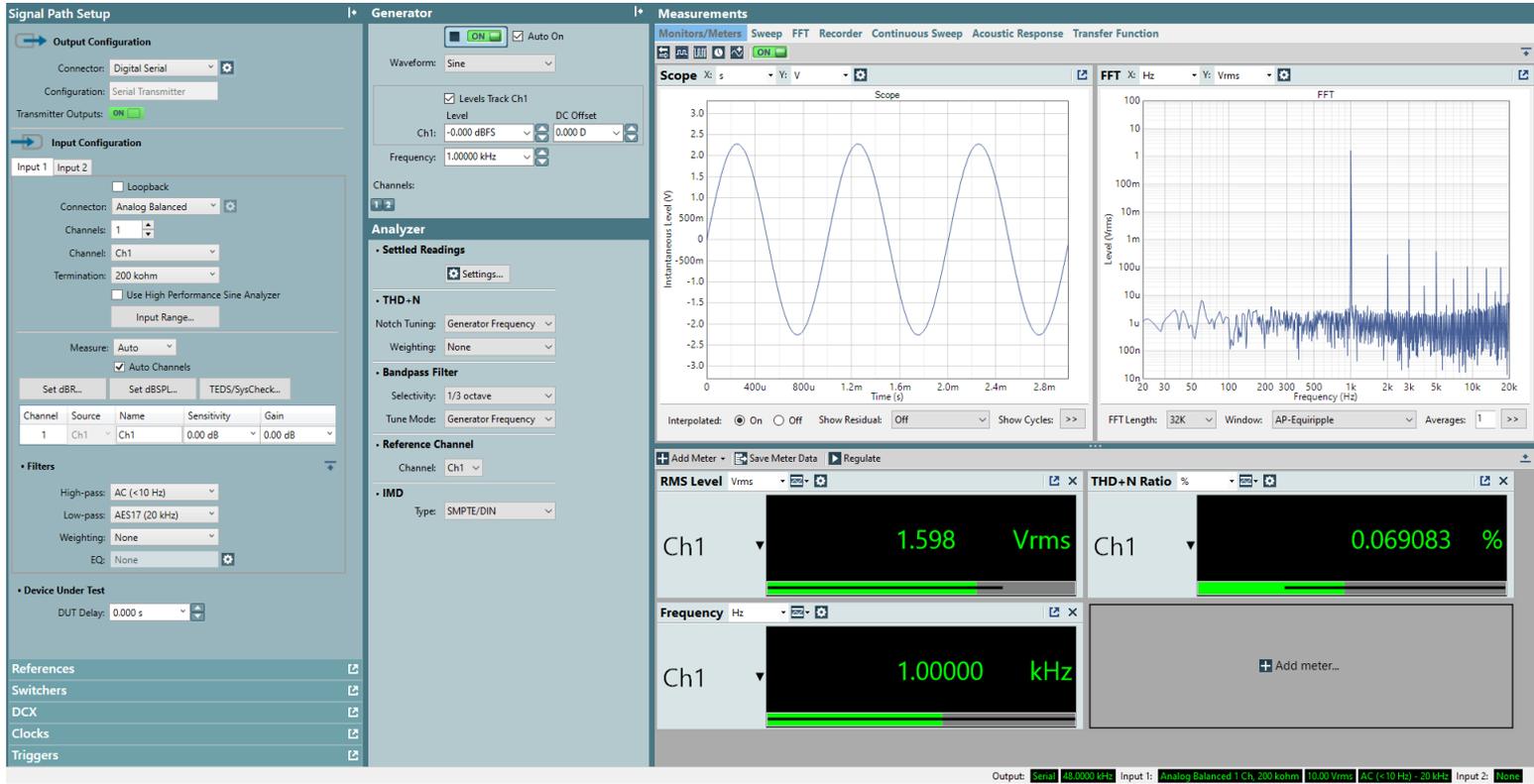
• Frequency

Scale Freq By: Output SR

The timing diagram shows three signals: BitClk (a high-frequency square wave), Frame (a low-frequency square wave), and Data1 (a signal with two channels). The first channel, Ch1, is labeled 'MSB' and 'LSB'. The second channel, Ch2, is labeled 'MSB' and 'Ch2'. A vertical dashed line indicates a specific time point.

Close Help

Digital Input Test Result



Output: Serial 48.0000 kHz Input 1: Analog Balanced 1 Ch, 200 kohm 1.000 Vrms AC (<10 Hz) -20 kHz Input 2: None