TAS2563 PDM

Applications Engineering – Low Power Audio & Actuators

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Block Diagram

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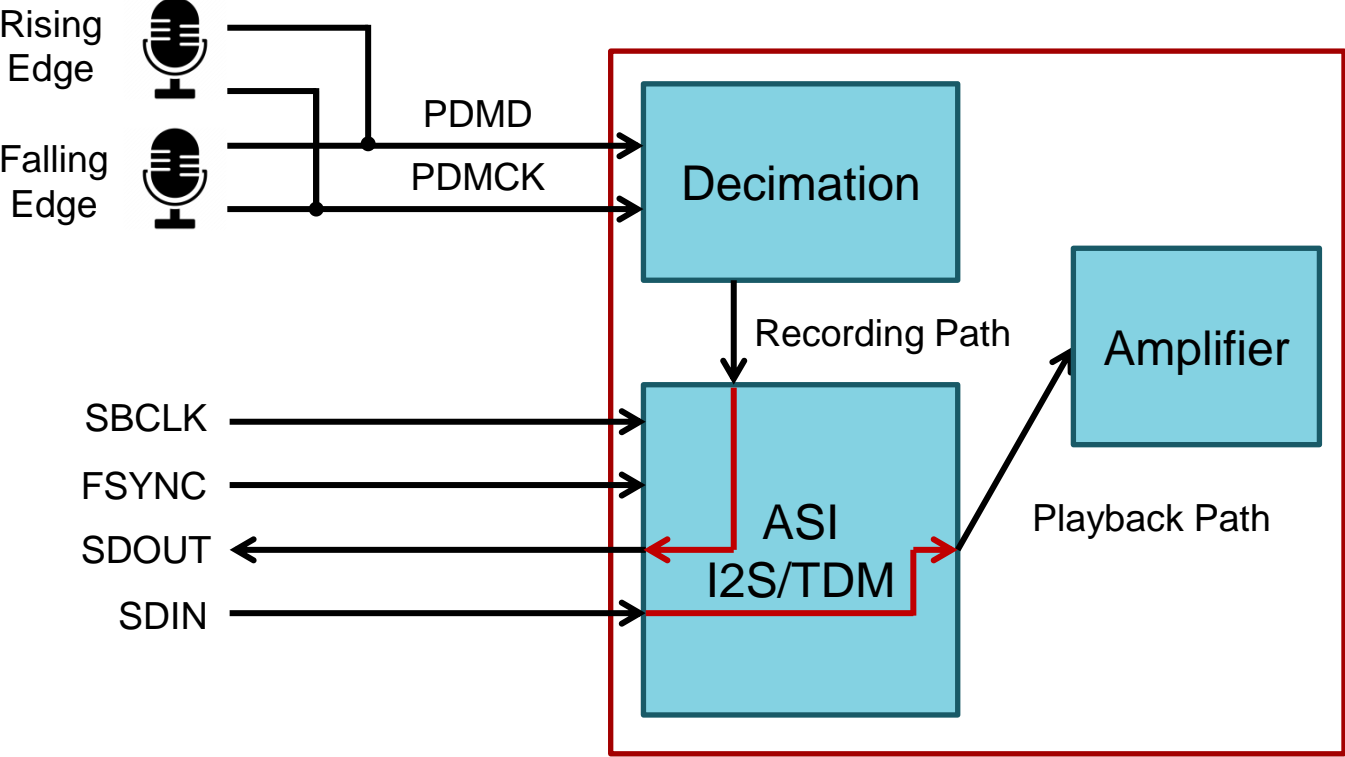
Configuration and Processing

- PDMCK is derived from SBCLK

- PDMCK can be configured:
  - 3.072MHz or 6.144MHz
  - Master or Slave (Output or Input)

- PDMD can be configured:
  - Mic1 and Mic2 paths can be assigned to rising or falling edge of PDMCK
  - Mic1 and Mic2 paths can be enabled/disabled individually

- -110dB to 30dB gain available for PDM Mic data

- Default SDOUT data is:
  - Mic1 on slot 0
  - Mic2 on slot 1
  - Echo Reference on slot 2

ASI Record Channel selection:

○ Audio In & Audio Out

○ Temperature & Excursion
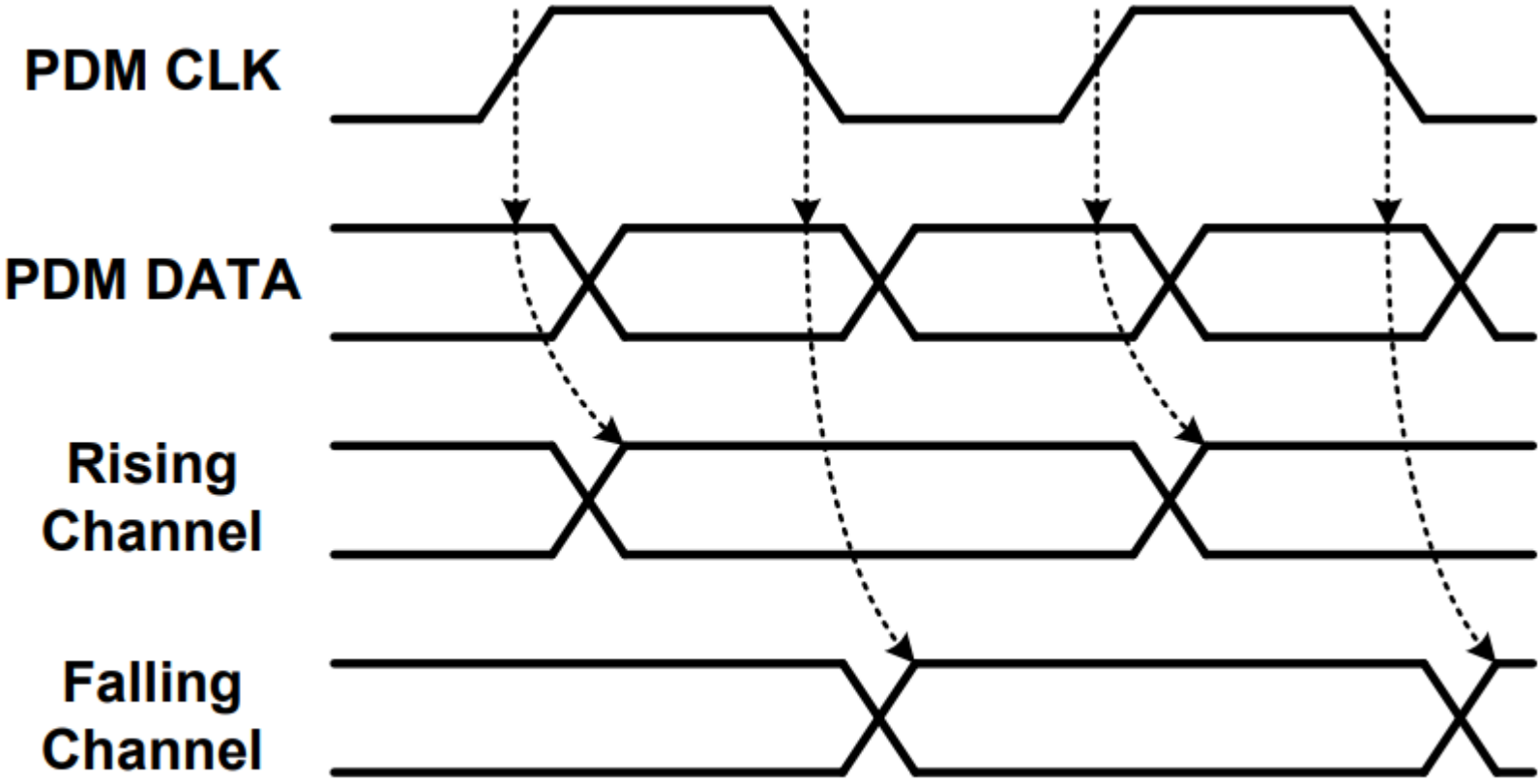
● PDM Mic & Echo Reference

○ I Sense & V Sense

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PDM Clock Diagram

Figure 58. PDM Waveform

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PDM Configuration Registers – B0 P0

65	PDM_CONFIG0												
		7								RSVD	1'b0	R	Reserved
			6							PDM_GATE_PAD0	1'b1	RW	Clock gating for master mode PAD0 0b = Disabled 1b = Enabled
				5						PDM_RATE_PAD0	1'b0	RW	PDM data ratefor PAD0 0b=3.072MHz 1b=6.144MHz
					4					DIS_PDM_MIC_CLK_ERR_PAD0	1'b0	RW	Disable PDM mic clock error on PAD0 detection 0b=Clock error detection is enabled 1b=Clock error detection is disabled
						3				PDM_PAD0_CAP_EDGE	1'b0	RW	Capture edge of PDM mic data for PAD0 0b=mic1 captured on posedge. Mic2 captured on negedge 1b=mic1 captured on negedge. Mic2 captured on posedge
							2			PDM_MIC2_EN	1'b0	RW	Control for PDM MIC2 path 0b=Disable the MIC2 path 1b=Enable the MIC2path
								1		PDM_MIC1_EN	1'b0	RW	Enable the PDM MIC1 path 0b=Disable the MIC1 path 1b=Enable the MIC1 path
									0	PDM_MIC_SLV	1'b1	RW	device in PDM MIC SLAVE or MASTER 0b=Device is in PDM MIC master mode 1b=Device is in PDM Slave mode

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PDM Configuration Registers – B0 P0

66	DIN_PD & PDM_CONFIG3													
		7							DIN_PD[14]		1'b0	RW	Weak pull down for SDIN2
														0b = Disabled
														1b = Enabled
			6						DIN_PD[13]		1'b0	RW	Weak pull down for SDOUT2
														0b = Disabled
														1b = Enabled
				5					RSVD		1'b0	R	Reserved
					4				wk_pulldown_pdmd_pad0		1'b0	RW	control for pulldown of pdmd_pad0
														0b=Disable the pulldown control
														1b=Enable the pulldown control
						3			wk_pulldown_pdmck_pad0		1'b0	RW	control for pulldown of pdmck_pad0
														0b=Disable the pulldown control
														1b=Enable the pulldown control
							2	1	0	RSVD		3'b000	R	Reserved

PDM Configuration Script

- w 98 00 00   # Go to page 0

- w 98 7F 00   # Go to book 0

- w 98 00 00   # Go to page 0

- # Disable PDMCK Gating for Master Mode

- # PDM data rate = 3.072MHz

- # Mic1 positive edge, Mic2 negative edge

- # Enable Mic1 and Mic2 path

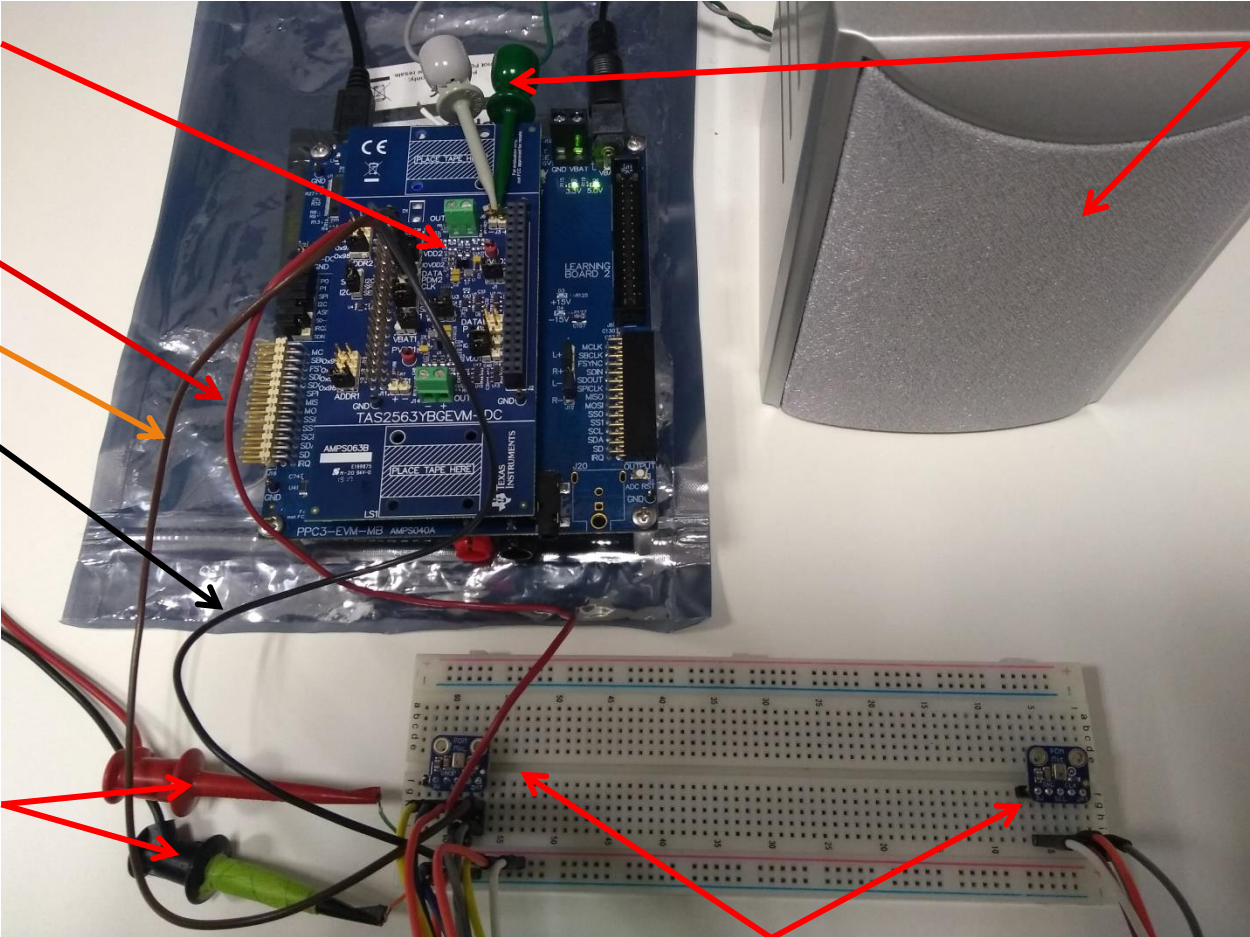- # PDM Master Mode

- w 98 41 06

- w 98 42 18

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Hardware Setup

Device Under Test

PDMCK

PDMD

GND

3V source for DMICs

Speaker

Digital Microphones

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Digital Microphone Connections
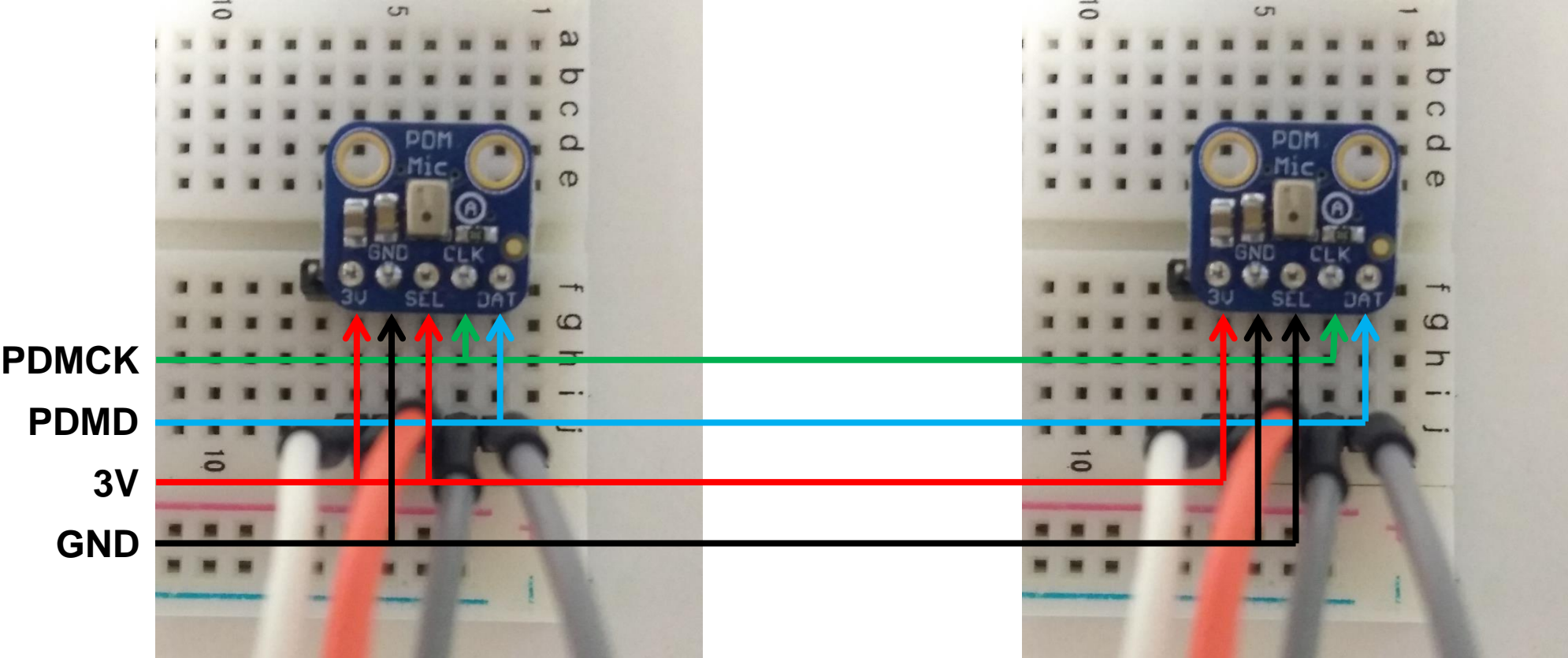
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PPC3

PDM Mic Gain is set from Tuning and Audio Processing -> SmartAmp settings

PPC3

PDM Mic data selected at End System Integration panel

Modify SDOUT Data Slots

- SDOUT data arrangement can be modified by using register 0x0b, 0x0c and 0x0d

- Register 0x0b controls data from mic2
  - LSBits select the slot, based on 8-bit counting:
    - w 98 0b 44 enables mic2 data and selects slot1 for 32-bit slot length
    - w 98 0b 42 enables mic2 data and selects slot1 for 16-bit slot length
    - w 98 0b 40 enables mic2 data and selects slot0 for 32-bit or 16-bit slot length

- Register 0x0c controls data from mic1
  - LSBits select the slot, based on 8-bit counting:
    - w 98 0c 44 enables mic1 data and selects slot1 for 32-bit slot length
    - w 98 0c 42 enables mic1 data and selects slot1 for 16-bit slot length
    - w 98 0c 40 enables mic1 data and selects slot0 for 32-bit or 16-bit slot length

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