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About This Manual

This manual describes the operation and instruction set of the Digital Signal Processor Core inside the TAS3xxx Digital Audio Processor Devices.

How to Use This Manual

This document contains the following chapters:

Chapter 1 – Overview of the TAS3xxx Audio Digital Signal Processor (DSP) Architecture
Chapter 2 – TAS3xxx DSP Data and Coefficient Formats
Chapter 3 – General Flow for Processing Digital Audio
Chapter 4 – TAS3xxx DSP Instruction Set

This manual is intended to be used by the developer to as a reference guide to programming DSP assembly language in any TAS3xxx Device from Texas Instruments. It is recommended to read through this manual as written for a firm understanding of the DSP core and its associated assembly language instruction set.

Additional Documentation

- TAS3xxx Data Manuals
- General TAS3xxx Application Notes
- PurePath Studio™ Graphical Development Environment User’s Guide
- TAS3xxx Firmware Programmers Reference Guide

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TAS3xxx Audio DSP Architecture Overview

1.1 TAS3xxx DSP Architecture Components:

The TAS3xxx Digital Signal Processor Core is a fixed-point computational engine consisting of an arithmetic unit, a single cycle hardware multiplier, a 76 bit accumulator, data, coefficient memory, and delay memory blocks. The architecture is optimized for programming digital audio processing blocks such as IIR filters, FIR filters, volume control, tone controls, mixers, DRC, loudness, etc. The TAS3xxx DSP Core contains the following components:

- **Data RAM**: Used as temporary storage for digital audio data
- **Coefficient RAM**: Contains filter or gain coefficients that can be multiplied by audio data
- **Register B**: Storage for data to be transformed by one of the following operations: barrel shifting, negation, absolute value, or pass through operation
- **Register L**: Storage for data to be transformed by one of the following operations: Log₂, Anti-Log₂, negation, absolute value, or pass through operation
- **Register MD**: Storage for 48 bit data to be multiplied
- **Register MC**: Storage for 28 bit coefficient data to be multiplied
- **Register BR**: Storage for result of operations performed on the contents of Register B
- **Register LR**: Storage for result of operations performed on the contents of Register L
- **Register MR**: Storage for result of multiplication of data contained in register MD and MC
- **ACC**: 76 bit Accumulator
- **Register DI**: Digital Input data from serial audio port (SAP) input or analog to digital converter (ADC) inputs. Data Ram memory mapped so that the lower three Least Significant bits decode the input channels
- **Register DO1-DO8**: An 8 register block for outputting data to the TAS3xxx Output SAP, or to digital to analog converters (DAC).
- **Register LFS**: The two least significant bits of the Digital input data that provide the programmer with a way to dither the audio (used in conjunction with Register B)
- **Register DLYI**: Input register used as an interface to the Delay RAM which provides a mechanism for delaying the audio data
- **Register DLYO**: Output register from delay RAM

Figure 1-1 shows the TAS3xxx DSP audio processing architecture.
TAS3xxx DSP Core Architecture

Figure 1-1 TAS3xxx DSP Core Architecture
2.1 Arithmetic Logical Unit Operand and Audio Encoding

Figure 2-1 shows the input data word structure of the arithmetic logic unit (ALU). Eight bits of overhead or guard bits are concatenated to the upper end of the 24 bit digital audio data word, and sixteen bits of computational precision or noise bits are concatenated to the lower end of the 24 bit digital audio data word. The incoming digital data words are positioned with the most significant bit abutting the 8-bit overhead/guard boundary regardless of if the digital data is represented by 16, 20, or 24 bits. The sign bit, bit 39, indicates that all incoming audio samples are treated as signed data samples.

![24 Bit Digital Input](image)

Figure 2-1: Input Data Word Structure of ALU Unit

The arithmetic engine is a 48-bit (25.23 format) processor consisting of a general-purpose 76-bit arithmetic logic unit and function specific arithmetic blocks. Multiply operations (excluding the function-specific arithmetic blocks) always involve 48-bit words and 28-bit coefficients. (The 28 bit coefficients are typically user defined and programmed via the I²C bus) If a group of products is to be added together, the 76-bit product of each multiplication is applied to a 76-bit adder, where a DSP-like multiply-accumulate operation takes place. Additionally, biquad filter computations use the Multiply-Accumulate operation to maintain precision in the intermediate computational stages.

The memory banks include a dual-port Data RAM for storing intermediate results, a Coefficient RAM for storing filter coefficients, a delay RAM for delaying the processed audio, and a fixed program ROM.

To maximize the linear range of the 76-bit ALU, saturation logic is used. In multiply-accumulate computations, intermediate overflows are permitted, and it is assumed that subsequent terms in the computation flow correct the overflow condition. This logic is detailed below in Figure 2-2.
2.2 Digital Audio Output Number Formats in TAS3xxx DSP Core

The Digital Audio Processor is a 48-bit signed fixed point arithmetic processing machine. The computed data is in 2’s complement format with the most significant bit being the sign bit and the lower 47 bits being the data bits. Mixer gain operations are implemented by multiplying a 48-bit signed data value by a 28-bit signed gain coefficient. The 76-bit signed product is then truncated to a signed 48-bit number. Add operations are implemented by a concatenating 28 bit signed offset coefficient to a 48-bit signed data value. In most cases, if the addition results in overflowing the 48-bit signed number format, saturation logic is used. This means that if the summation results in a positive number that is greater than 0x7FFF FFFF FFFF, the number is set to 0x7FFF FFFF FFFF. Likewise, if the summation results in a negative number that is less than 0x8000 0000 0000, the number is set to 0x8000 0000.

2.2.1 28 Bit 5.23 Number Format

All mixer gain coefficients are 28-bit coefficients using a 5.23 number format. Numbers formatted as 5.23 numbers have 5 bits to the left of the implied binary point and 23 bits to the right of the implied binary point. This is shown in the figure 2-3.

The decimal value of the 5.23 format number can be found by following the weighting as illustrated in figure 2-4. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case, every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 2-4 applied to obtain the magnitude of the negative number.

$$\text{Coefficient Decimal Value} = \frac{4}{2^4} + \frac{3}{2^3} + \frac{2}{2^2} + \frac{2}{2^1} + \frac{1}{2^0} + \frac{-1}{2^{-1}} + \frac{-2}{2^{-2}} + \ldots + \frac{-2^{22}}{2^{-23}}$$
Gain coefficients, entered via the \textsuperscript{I2C} bus, must be entered as 32-bit binary numbers. The format of the 32-bit number is shown below.

\textbf{Figure 2-5: \textsuperscript{I2C} Format for Coefficients}

As the above figure shows, the hexadecimal value of the integer part of the gain coefficient cannot be concatenated with the hex value of the fractional part of the gain coefficient to form the 32-bit \textsuperscript{I2C} coefficient. The reason is that the 28-bit coefficient contains five bits of integer, and thus the integer part of the coefficient occupies all the one hex digit and the most significant bit of the second hex digit. In the same way, the fractional part occupies the lower three bits of the second hex digit, and then occupies the other five hex digits (with the eight digit being the zero-valued most significant hex digit).

\subsection*{2.2.2 48-Bit 25.23 Number Format}

All level adjustment and threshold coefficients are 48-bit coefficients using the 25.23 number format. Numbers formatted as 25.23 numbers have 25 bits to the left of the implied decimal point and 23 bits to the right of the implied decimal point. This format is shown in figure 2-6.

\textbf{Figure 2-6: 48 Bit 25.23 Number Format}

The decimal value of the 25.23 format number can be found by following the weighting shown in the figure 2-7 below. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case, every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 2-7 applied to obtain the magnitude of the negative number.
Data Decimal Value = $2^4 + 2^3 + 2^2 + 2^1 + 2^0 + \ldots + 2^{-22} + 2^{-23}$

**Figure 2-7: 25.23 to Decimal Number Conversion Formula**

Two 32 bit words must be sent over the $i^2$C bus to download a level or threshold coefficient into the TAS3xxx Device. The alignment of the 48 bit, 25.23 formatted coefficient in the 8 byte $i^2$C word is shown in figure 2-8.

**Figure 2-8: $i^2$C Format for Data**

$u$ = unused or don’t care bits
Digit = hexadecimal digit
2.2.3 TAS3xxx Digital Audio Scaling

The TAS3xxx digital audio processing is designed so that noise produced by filter operations is maintained below the smallest signal amplitude of interest, as shown in the figure below. This low noise level is achieved by increasing the prevision of the signal representation substantially above the number of bits that are absolutely necessary to represent the input signal.

Additional precision, in the form of overflow bits, is used to permit the value of intermediate calculations to exceed the input precision without clipping. The TAS3xxx Digital Audio Processor achieved both of these important performance capabilities by using a high performance digital audio processing architecture with a 48 bit data path, 28 bit filter coefficients, and a 76 bit Accumulator.

![Figure 2-9: TAS3xxx Digital Audio Scaling](image)

2.3 DSP Program Counter

The DSP program counter (PC) is automatically set to 0 on startup and on completion of an LRCLK (Fs) frame. The PC is advanced by the DSP clock, whose frequency is dependent on the sample rate (Fs) and the serial data mode.

For a standard I²S input at Fs = 48 kHz, and Master Clock (MCLK) of 12.288 MHZ, the DSP clock runs at approximately 135 MHz. This means that there are ~2816 DSP cycles per sample available for processing.
3.1 Audio Processing Flow

The TAS3xxx audio processing is normally done on a sample-by-sample bases at rate equal to the sampling frequency \( F_s \). The general flow of the TAS3xxx processing scheme is shown in Figure 3-1.

1. Digital audio data from either Serial Audio Port (SAP) or Analog-to-Digital Converter (ADC) is input
2. Digital audio data is processed by DSP
3. Processed digital audio is output to SAP, Digital to Analog Converter, or S/PDIF
4. Real-time control from user is provided by \( \text{i}^2\text{C} \) using embedded M8051 Microcontroller Unit (MCU)

![Figure 3-1. General TAS3xxx Audio Process Flow](image-url)

3.1.1 Digital Audio Data Input

The TAS3xxx Family of Devices offer both digital audio data inputs (SDIN1, SDIN2, etc…) and Analog-to-Digital converted audio data. In most applications, these audio inputs are stereo inputs from an external source. The digital data is input to the DSP through Register DI. These inputs can be immediately processed, or stored in Data RAM for later processing in the cycle.

**Note:** Refer to the respective TAS3xxx Data Manuals for exact input and output options available.
3.1.2 Audio Data Processing

Immediately after the data leaves Register DI, it is normally processed by a series of blocks programmed in TAS3xxx DSP assembly language. For the non-experienced DSP assembly language programmer, a high level graphical drag and drop tool is available from Texas Instruments. For more information about this tool, refer to the PurePath Studio™ Graphical Development Environment User’s Guide. These processing blocks are normally common audio blocks such as IIR filters, volume control, tone control, Dynamic Range Compression (DRC), loudness, delay, mixers, and other commonly used blocks. Because the TAS3xxx DSP is fully programmable, the only limitation to the number of processing blocks is the available hardware resources (DSP Program RAM, DSP Coefficient RAM, and DSP Data RAM) and the developer’s imagination.

A simple example of an audio processing block is shown in Figure 3-2. This example is a 4 input mixer that provides real-time control of the mixer gains by way of the I^2C coefficients GAIN1, GAIN2, GAIN3, and GAIN4.

![Figure 3-2: Example Audio Processing Block Diagram](image)

An example of the TAS3xxx assembly code used to implement this four input mixer is shown in Table 3-1. It is assumed that the Inputs to the processing block (MIX_IN1_D, MIX_IN2_D, MIX_IN3_D, and MIX_IN4_D) have had the previous block outputs stored to them prior to this example. Likewise, the data output from this block (MIX_OUT_D) is available for further processing after the completion of this block.
Table 3-1: Example Audio Processing Block DSP Assembly Code

3.1.3 Output of Processed Audio Data

The TAS3xxx architecture supports both digital and analog outputs. Immediately after the completion of the programmable audio processing blocks, the audio is available via the outputs (Registers DO1-DO8). Although there are no constraints on which Output Register are used for the output data variables, a programmer may find it useful to use all the available output registers for more efficient code. Table 3-2 shows an example of optimized use of the Input and Output Data Registers.

Note: Refer to the respective TAS3xxx Data Manuals for exact input and output options available

Table 3-2: Optimized DSP Assembly Code

3.1.4 Real-Time Control of Audio Processing

Real-Time control of audio processing is provided by a hardware based \( I^2C \) interface of the TAS3xxx device. The \( I^2C \) interface is facilitated by a TAS3xxx hardware block that interfaces with the embedded M8051 Microcontroller. This communication is accomplished though the \( I^2C \) slave interface in which the external system controller is the master \( I^2C \) device and the TAS3xxx is the \( I^2C \) slave device. Legal Master and Slave Addresses are available in the respective TAS3xxx Data Manuals.

The smallest \( I^2C \) transaction in a command is four bytes. The M8051 Microcontroller is (by default) programmed so that the maximum number of bytes in an \( I^2C \) command is 20 bytes. This facilitates sending five filter coefficients at a time since one of the main audio components is an IIR Biquad filter that requires five filter coefficients (four bytes per coefficient). In the case of the four input mixer...
component shown in the example above, the four gain values (GAIN1, GAIN2, GAIN3, and GAIN4) can be send from the system controller to the TAS3xxx Device with one I²C write containing 16 bytes.

3.2 Advanced Audio Processing Features of the TAS3xxx DSP Core

The TAS3xxx DSP includes the following functions in the core:

- Single Cycle 48 bit by 28 bit Multiply
- 76 bit Addition
- Multiply-Accumulate Capability
- Approximate Log₂ and Anti-Log₂ mathematical operations

These features are explained in the following sections.

3.2.1 Single Cycle Multiply

There is no explicit multiply instruction in the TAS3xxx DSP instruction set. For this purpose, a 48 bit by 28 bit multiply operation is implicitly performed every DSP clock cycle and is controlled by the data loaded into registers MC and MD. The output of each multiply is stored in Register MR after two DSP clock cycles.

**Note:** If the contents of MC and MD are not changed, the MR register contains the same value.

3.2.2 76 Bit Addition

The 76 bit addition block has two input operands, A and B. Operand A can be from the 76 bit accumulator register or the 48 bit BR register. Operand B can be from the 48 bit LR register or from the 76 bit MR register or 76-bit ZERO register.

When a 48 bit data value is used as an operand, three automatic transformations done to convert the data into a 76 bit value.

- The original 48 bit adder data is input from either BR or LR.
- 28 zeros are concatenated following the Least Significant Bit of the 48 bit data
- The result of the concatenation is arithmetically shifted right by five bits, and signed extended

The following figure graphically shows the automatic transformation that occurs to each 48 bit data register.
STEP 1: Original 48-Bit Adder Input Data from BR or LR

48 bits

S b46 b45 b44 b43 b42 b41 b40

STEP 2: Concatenate 28 Zeroes in LSB

76 bits

48 bits

28 bits of 0

S b46 b45 b44 b43 b42 b41 b40 0 0 0

STEP 3: Arithmetic Shift Right Five Bits

76 bits

S S S S S S b46 b45 b44 b43 b42 b41 b40 0 0 0 0

23 bits of 0

LSB

Figure 3-3: Automatic 48 bit to 76 bit conversion

The 76 bit result of the addition is then clipped from a 76 bit result into a 48 bit data value. This process is shown in Figure 3-6.

ADD Output Algorithm to Get to 48-Bit Space

76 bits

decimal

S b74 b73 b72 b71 b70 b69

b47 b46 b45 b44

b25 b24 b23 x x x

Lower 23 bits

LSB

if S = 1 and (if SUM of lower 23 bits <= 0)
then b23 = b23 + 1;

if S = 1 and (if SUM of lower 23 bits = 0)
then "do nothing";

if S = 0
then "do nothing"

if S = 1 and any adjacent lower bits = 0
then output MAX NEGATIVE 25.23 number;

if S = 0 and any adjacent lower bits = 1
then output MAX POSITIVE 25.23 number;

Figure 3-4: 76 bit Clip to a 48 bit data value
3.2.3 Multiply-Accumulate

Figure 3-7 shows how the developer can implement a multiply-accumulate operation using the TAS3xxx DSP assembly language.

![Diagram](image_url)

Figure 3-5: Multiply-Accumulate implementation via TAS3xxx DSP Assembly Code

Example:
Load 0x333333333333 into MD
Load 0x00033333 into MC
Clear ACC
ADD ACC + MR
Store output of ADD into B
Store B into Data Memory

\[
\begin{align*}
333333333333 & \rightarrow MD \\
X \ 00033333 & \rightarrow MC \\
0000\text{A3D66666666666}C20 & \quad \text{(output stored in MR)}
\end{align*}
\]

The value stored in the 48-bit data memory is shown in the diagram.
3.2.4 Log$_2$ and Anti-Log$_2$ Operations

Log$_2$ and Anti-Log$_2$ operations are normally used to scale data so that processing can be performed without clipping. The following figure shows how these operations are performed in the TAS3xxx DSP Core.

\[
\text{Actual Log}_2(1/4) = -2
\]

TAS3108 DAP Hardware approximation

\[\text{Log}_2_{\text{approx}}(1/4) = 2^{-0} + 2^{-1} + 2^{-3} + 2^{-6} = 1.9375\]

Note that input data must be scaled when input to LOG function. This could be SHL(24) in this example.

Log in 48 bit spaced is normalized input from 0 to 1 using 32 bit precision.

Log output is in 5-4 precision unsigned number aligned in 25.23 database.

Antilog operation

1's complement

Sets offset from 25 bit MSB

\[\text{LOG}_2(0.25) = 1.9375\] (output is non-signed)

\[\text{ALOG}_2(1.9375) = 4\]

\[\text{SHR}(4) = 0.26\]

Figure 3-6: TAS3xxx DSP Log$_2$ and Anti-Log$_2$ Implementation
4.1 DSP Instruction Word Format

The TAS3xxx Family of Digital Audio Processors uses a 54 bit instruction word which can simultaneously load two operands from Data RAM and Coefficient RAM, store the result, and perform two parallel arithmetic operations. Figure 4-1 shows the format of the 54 bit DSP Instruction word.

The instruction word is broken down into five sections. ALU Stage 1, ALU Stage 2, Memory Operation Stage 1, Memory Operation Stage 2, and Memory Operation Stage 3

ALU Stage 1 executes mathematical features that transform the contents of the B and L registers into the desired values that are send to the ALU.

ALU Stage 2 executes the arithmetic logic instructions to the specified input operands and returns the result.

Memory Operation Stage 1 loads the contents of the selected Data RAM Register into the specified register.

Memory Operation Stage 2 loads the contents of the selected Coefficient RAM Register into the specified register.

Memory Operation Stage 3 stores the contents of the specified register back into Data or Coefficient RAM, or into Register B, L, or MD.

<table>
<thead>
<tr>
<th>ALU Stage 1</th>
<th>ALU Stage 2</th>
<th>Memory Operation Stage 1 (Data RAM Loads)</th>
<th>Memory Operation Stage 2 (Coefficient RAM Loads)</th>
<th>Memory Operation Stage 3 (Data &amp; Coefficient RAM Stores)</th>
</tr>
</thead>
<tbody>
<tr>
<td>53</td>
<td>49</td>
<td>42</td>
<td>27</td>
<td>14</td>
</tr>
<tr>
<td>48</td>
<td>41</td>
<td>26</td>
<td>13</td>
<td>0</td>
</tr>
</tbody>
</table>

*Figure 4-1: TAS3xxx DSP Instruction Word Format*
4.2 DSP Assembly Language Instruction Set

The following tables outline the DSP Assembly Instructions for the TAS3xxx Family of Devices for each stage of the Digital Signal Processor core. Details about each of the instructions are available in the sections that follow.

### 4.2.1 ALU Stage 1 Instruction Set

**Table 4-1: ALU Stage 1 Instruction Set**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
<th>Functional Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABS (reg)</td>
<td>Absolute Value</td>
<td>Performs Absolute value on data in (reg)</td>
</tr>
<tr>
<td>NEG (reg)</td>
<td>Performs 2's Complement</td>
<td>Negates data in (reg)</td>
</tr>
<tr>
<td>LOG2 (reg)</td>
<td>Base Two Logarithm</td>
<td>Performs Base Two Log of data in (reg)</td>
</tr>
<tr>
<td>ALOG2 (reg)</td>
<td>Base Two Anti-Logarithm</td>
<td>Performs Base Two Anti-Log of data in (reg)</td>
</tr>
<tr>
<td>SHR (bits)</td>
<td>Logical Shift Right</td>
<td>Shifts data in Register B right by (bits) bits</td>
</tr>
<tr>
<td>SHL (bits)</td>
<td>Shift Left</td>
<td>Shifts data in Register B left by (bits) bits</td>
</tr>
<tr>
<td>CLRACC</td>
<td>Clear Accumulator</td>
<td>Clears Accumulator Register</td>
</tr>
<tr>
<td>THRU (reg)</td>
<td>Transfer Register to next stage</td>
<td>Copies Register B to BR, and Register L to LR</td>
</tr>
<tr>
<td>JMP (reg)</td>
<td>Absolute Jump</td>
<td>Used in conjunction with PCADDR</td>
</tr>
<tr>
<td>BOC</td>
<td>Branch when A Comp to B = 1</td>
<td>Used in conjunction with PCADDR</td>
</tr>
<tr>
<td>BNC</td>
<td>Branch when A Comp to B = 0</td>
<td>Used in conjunction with PCADDR</td>
</tr>
<tr>
<td>STOP</td>
<td>Stop Program Counter</td>
<td>Parameter of PCADDR: PCADDR(Label)</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td></td>
</tr>
</tbody>
</table>

### 4.2.2 ALU Stage 2 Instruction Set

**Table 4-2: ALU Stage 2 Instruction Set**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
<th>Functional Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLRACC</td>
<td>Clear Accumulator</td>
<td>Clears Accumulator Register</td>
</tr>
<tr>
<td>ADD (a,b,c,d)</td>
<td>Add operands a and b w/clip c, store in reg d</td>
<td>Adds a to b and stores in register d with clip parameter c</td>
</tr>
<tr>
<td>COMP (reg1, reg2)</td>
<td>Compare registers 1 and 2</td>
<td>Compares operands [ACC or BR] to [LR or MR]</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td></td>
</tr>
</tbody>
</table>

### 4.2.3 Memory Operations Stage 1 Instructions

**Table 4-3: Memory Operation Stage 1 Instruction Set**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
<th>Functional Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD (addr, reg)</td>
<td>Load</td>
<td>Loads value from Data Ram at addr to reg</td>
</tr>
<tr>
<td>LDC (addr, reg)</td>
<td>Load when A Comp to B = 1</td>
<td>Loads value from Data Ram at addr to reg when compare = 1</td>
</tr>
<tr>
<td>LNC (addr, reg)</td>
<td>Load when A Comp to B = 0</td>
<td>Loads value from Data Ram at addr to reg when compare = 0</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td></td>
</tr>
</tbody>
</table>
4.2.4 Memory Operations Stage 2 Instructions

Table 4-4: Memory Operation Stage 2 Instruction Set

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
<th>Functional Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD (addr, reg)</td>
<td>Load</td>
<td>Loads value from Coefficient Ram at addr to reg</td>
</tr>
<tr>
<td>LDC (addr, reg)</td>
<td>Load when A Comp to B = 1</td>
<td>Loads value from Coef Ram at addr to reg when compare = 1</td>
</tr>
<tr>
<td>LNC (addr, reg)</td>
<td>Load when A Comp to B = 0</td>
<td>Loads value from Coef Ram at addr to reg when compare = 0</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td>-</td>
</tr>
</tbody>
</table>

4.2.5 Memory Operations Stage 3 Instructions

Table 4-5: Memory Operation Stage 3 Instruction Set

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
<th>Functional Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST (reg, DATA, addr)</td>
<td>Store register to Data RAM</td>
<td>Stores value in reg to Data RAM at address addr</td>
</tr>
<tr>
<td>ST (reg, COEF, addr)</td>
<td>Store register to Coefficient RAM</td>
<td>Stores value in reg to coef RAM at address addr</td>
</tr>
<tr>
<td>PCADDR</td>
<td>Assign Label</td>
<td>Used in conjunction with JMP, BOC, or BNC</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td>-</td>
</tr>
</tbody>
</table>
4.3 Detailed Description of TAS3xxx DSP Instruction Set

4.3.1 ABS (reg)

Description:
This instruction computes the absolute value of the data in Register B or Register L. The result of this instruction is available in the BR or LR register on the start of the next DSP clock cycle.

Syntax:

<table>
<thead>
<tr>
<th>Syntax</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABS(B)</td>
<td>00001</td>
</tr>
<tr>
<td>ABS(L)</td>
<td>01110</td>
</tr>
</tbody>
</table>

Example 1: ABS(B) | NOP | NOP | NOP | NOP

Register B:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Register Contents After Instruction Execution</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFFF FE80 0000 47 0</td>
<td>0xFFF FE80 0000 47 0</td>
</tr>
</tbody>
</table>

Register BR:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Register Contents After Instruction Execution</th>
</tr>
</thead>
<tbody>
<tr>
<td>47 Don’t Care 0</td>
<td>47 0</td>
</tr>
</tbody>
</table>

Example 2: ABS(L) | NOP | NOP | NOP | NOP

Register L:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Register Contents After Instruction Execution</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000 0180 0000 47 0</td>
<td>0x0000 0180 0000 47 0</td>
</tr>
</tbody>
</table>

Register LR:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Register Contents After Instruction Execution</th>
</tr>
</thead>
<tbody>
<tr>
<td>47 Don’t Care 0</td>
<td>47 0</td>
</tr>
</tbody>
</table>
4.3.2 ADD (rega, regb, para, regd)

**Description:**

This instruction adds Register `rega` to Register `regb`. The 76 result of addition is clipped by the parameter `para` and is then stored in register `regd`. Register `rega` can be the ACC or BR. Register `regb` can be Register (LR, MR, or ZERO). `para` can be either no clip, a 32 bit clip, or a 28 bit clip (NONE, CLIP32, or CLIP28). Register `regd` can be Register (ACC, B, DLYI, L, MC, MD or DO1, DO2, ..., DO8)

<table>
<thead>
<tr>
<th>Syntax:</th>
<th>Opcode:</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD(ACC,LR,CLP32,DO1)</td>
<td>011 1001</td>
</tr>
<tr>
<td>ADD(ACC,LR,CLP32,DO2)</td>
<td>011 1010</td>
</tr>
<tr>
<td>ADD(ACC,LR,CLP32,DO3)</td>
<td>011 1011</td>
</tr>
<tr>
<td>ADD(ACC,LR,CLP32,DO4)</td>
<td>011 1100</td>
</tr>
<tr>
<td>ADD(ACC,LR,CLP32,DO5)</td>
<td>110 1111</td>
</tr>
<tr>
<td>ADD(ACC,LR,CLP32,DO6)</td>
<td>110 0010</td>
</tr>
<tr>
<td>ADD(ACC,LR,CLP32,DO7)</td>
<td>110 0011</td>
</tr>
<tr>
<td>ADD(ACC,LR,CLP32,DO8)</td>
<td>110 0011</td>
</tr>
<tr>
<td>ADD(ACC,ZERO,NONE,B)</td>
<td>101 0000</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO1)</td>
<td>111 0001</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO2)</td>
<td>111 0010</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO3)</td>
<td>111 0011</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO4)</td>
<td>111 0100</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO5)</td>
<td>110 1101</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO6)</td>
<td>110 0101</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO7)</td>
<td>110 0101</td>
</tr>
<tr>
<td>ADD(BR,LR,CLP32,DO8)</td>
<td>110 0100</td>
</tr>
<tr>
<td>ADD(BR,LR,NONE,B)</td>
<td>000 1010</td>
</tr>
<tr>
<td>ADD(BR,LR,NONE,L)</td>
<td>000 1011</td>
</tr>
<tr>
<td>ADD(BR,LR,NONE,MC)</td>
<td>000 1100</td>
</tr>
<tr>
<td>ADD(BR,LR,NONE,MD)</td>
<td>000 1001</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO1)</td>
<td>010 1111</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO2)</td>
<td>010 1100</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO3)</td>
<td>010 1101</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO4)</td>
<td>010 1000</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO5)</td>
<td>110 1100</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO6)</td>
<td>101 1100</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO7)</td>
<td>101 1101</td>
</tr>
<tr>
<td>ADD(BR,MR,CLP32,DO8)</td>
<td>111 0000</td>
</tr>
<tr>
<td>ADD(BR,MR,NONE,ACC)</td>
<td>000 0101</td>
</tr>
<tr>
<td>ADD(BR,MR,NONE,B)</td>
<td>000 0010</td>
</tr>
<tr>
<td>ADD(BR,MR,NONE,DLYI)</td>
<td>000 0111</td>
</tr>
<tr>
<td>ADD(BR,MR,NONE,L)</td>
<td>000 0011</td>
</tr>
<tr>
<td>ADD(BR,MR,NONE,MC)</td>
<td>000 0100</td>
</tr>
<tr>
<td>ADD(BR,MR,NONE,MD)</td>
<td>000 0001</td>
</tr>
<tr>
<td>ADD(BR,ZERO,CLP32,B)</td>
<td>101 1011</td>
</tr>
<tr>
<td>ADD(BR,ZERO,NONE,B)</td>
<td>101 1000</td>
</tr>
<tr>
<td>ADD(BR,ZERO,NONE,L)</td>
<td>101 1001</td>
</tr>
<tr>
<td>ADD(BR,ZERO,NONE,MC)</td>
<td>101 1010</td>
</tr>
<tr>
<td>ADD(BR,ZERO,NONE,MD)</td>
<td>101 0111</td>
</tr>
</tbody>
</table>
Example 1:   NOP | ADD(BR,MR,CLP32,DO3) | NOP | NOP | NOP

Register MR:   Register BR

Register Contents Before Instruction Execution: 0x0000 0000 001C
Register Contents After Instruction Execution: 0x0000 0000 001C

Register DO3:

Register Contents Before Instruction Execution: 0x0000 0000 001C
Register Contents After Instruction Execution: 0x0000 0000 001C
4.3.3 **ALOG2**

**Description:**

This instruction computes the approximate inverse Base 2 Logarithm of the data in Register L. The result of this instruction is available in the Register LR on the start of the next DSP clock cycle.

The input is in base 2 log space (5.4 precision unsigned number) with a range of 0.0000 to 31.9375. The output is in linear space (25.23 precision unsigned number).

**Note:** The base 2 anti-logarithm is only available for the contents of Register L.

**Syntax:** ALOG2(L)  
**Opcode:** 00100

**Example 1:** ALOG2(L) | NOP | NOP | NOP | NOP

<table>
<thead>
<tr>
<th>Register L:</th>
<th>Register LR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents Before Instruction Execution</td>
<td>Register Contents Before Instruction Execution</td>
</tr>
<tr>
<td>0x0000 0DF8 0000</td>
<td>Don’t Care</td>
</tr>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>Register Contents After Instruction Execution</td>
</tr>
<tr>
<td>0x0000 0DF8 0000</td>
<td>0x0000 0200 0000</td>
</tr>
</tbody>
</table>

**Example 2:** ALOG2(L) | NOP | NOP | NOP | NOP

<table>
<thead>
<tr>
<th>Register L:</th>
<th>Register LR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents Before Instruction Execution</td>
<td>Register Contents Before Instruction Execution</td>
</tr>
<tr>
<td>0x0000 0078 0000</td>
<td>Don’t Care</td>
</tr>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>Register Contents After Instruction Execution</td>
</tr>
<tr>
<td>0x0000 0078 0000</td>
<td>0x0000 0400 0000</td>
</tr>
</tbody>
</table>
4.3.4 **BOC**

**Description:**
This instruction executes a conditional branch to *label* if the value of operand A is equal to the value of operand B. This results when a compare instruction of these operands results in a logic 0.

The PCADDR instruction is always used with the BOC instruction

**Note:** When a BOC is performed, no other instructions (Except NOPs) are allowed on that cycle

**Syntax:**

```plaintext
BOC
```

**Opcode:** 10011

**Example 1:**

```plaintext
BOC | NOP | NOP | NOP | PCADDR(BRANCH_PT)
    | NOP | NOP | NOP | NOP
    | NOP | NOP | NOP | NOP
    | NOP | NOP | NOP | NOP
    | < other processing(optional) >
    BRANCH_PT | NOP | NOP | NOP | NOP
```

**Register PC:**

**If Operand A = Operand B**

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>PC Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Contents 3 cycles After Instruction Execution</th>
<th>BRANCH_PT Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

**If Operand A ≠ Operand B**

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>PC Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Contents 3 Cycles After Instruction Execution</th>
<th>PC Address + 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>
4.3.5 **BNC**

**Description:**
This instruction executes a conditional branch to *label* if the value of operand A is not equal to the value of operand B. This results when a compare instruction of these operands results in a logic 1.

**Syntax:**
```
BNC
```

**Opcode:** 10100

**Example 1:**
```
BNC | NOP | NOP | NOP | PCADDR(BRANCH_PT)
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP

< other processing(optional) >

BRANCH_PT | NOP | NOP | NOP | NOP
```

**Register PC:**

*If Operand A = Operand B*

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>PC Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Contents 3 Cycles After Instruction Execution</th>
<th>PC Address + 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

*If Operand A ≠ Operand B*

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>PC Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Register Contents 3 Cycles After Instruction Execution</th>
<th>BRANCH_PT Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>
4.3.6 **CLRACC**

**Description:**

This instruction clears the contents of the 76 bit accumulator register. On the next DSP clock cycle, the Accumulator Register will contain all zeros.

**Syntax:**  
CLRACC  

**Opcode:**  
01111

**Example 1:**  
CLRACC | NOP | NOP | NOP | NOP

**Register ACC:**

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>75</th>
<th>Don't Care</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>0x000 0000 0000 0000 0000 0000</td>
<td>75</td>
<td>0</td>
</tr>
</tbody>
</table>
4.3.7 **COMP (rega, regb)**

**Description:**

This instruction compares the sign of Register *rega* with the sign of Register *regb* where *rega* is the accumulator or Register BR, and *regb* may be either, Register LR, Register MR or Register ZERO. The result of the compare function is input to a multiplexer that determines the compare result. See the figure 4-2 for details.

**Note:** The result of the COMP Instruction will be available two DSP clock cycles after the instruction is executed.

There are six cases that correspond to the compare instruction:

1. If Operand A and Operand B are positive, then the result of the compare is 0
2. If Operand A and Operand B are negative, then the result of the compare is 1
3. If Operand A is negative and Operand B is positive and the absolute value of both Operands are equal, then the result of the compare is 0
4. If Operand A is positive and Operand B is negative and the absolute value of both Operands are equal, then the result of the compare is 1
5. If the absolute value of Operand A is greater than the absolute value of Operand B, then the result of the compare is 1
6. If the absolute value of Operand A is less than the absolute value of Operand B, then the result of the compare is 0.

A table of test values and the result is shown below in Table 4-6.

**Syntax:**

<table>
<thead>
<tr>
<th>Syntax</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP(ACC, LR)</td>
<td>010 0000</td>
</tr>
<tr>
<td>COMP(ACC, MR)</td>
<td>001 10000</td>
</tr>
<tr>
<td>COMP(BR, LR)</td>
<td>001 0000</td>
</tr>
<tr>
<td>COMP(BR, MR)</td>
<td>000 1000</td>
</tr>
</tbody>
</table>

**Example 1:**

```
NOP | COMP(ACC, LR) | NOP | NOP | NOP
```

**Register ACC:**

- Register Contents Before Instruction Execution: Don't Care
- Register Contents After Instruction Execution: Don't Care

**Register LR:**

- Register Contents Before Instruction Execution: Don't Care
- Register Contents After Instruction Execution: Don't Care
Figure 4-2: TAS3xxx Comparison Hardware
<table>
<thead>
<tr>
<th>Operand_A</th>
<th>Operand_B</th>
<th>sum</th>
<th>A_CP_B</th>
<th>Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>-1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>-1</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>-1</td>
<td>-1</td>
<td>-2</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>3</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>-2</td>
<td>1</td>
<td>-1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>-1</td>
<td>1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>-2</td>
<td>-1</td>
<td>-3</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>-1</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>-2</td>
<td>-1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>-1</td>
<td>-2</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>-1</td>
<td>-1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>-1</td>
<td>0</td>
<td>-1</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
4.3.8 DLYPTR(ptr)

Description:
This instruction is used to indicate which 10 bit delay memory pointer is used for the current audio delay function.

Syntax: DLYPTR(ptr)  Opcode: 0000

Example 1:  NOP | CLRACC | LD(DelayIn1_D,L, NONE) | NOP | NOP
THRU(L) | NOP | NOP | NOP | NOP
NOP | ADD(ACC,LR,NONE,DLY1) | NOP | NOP | DLYPTR(0)
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | ST(DLYO,DATA,DelayOut1_D)
### 4.3.9 JMP

**Description:**

This instruction executes an unconditional program counter jump to the address specified by `label`.

The PCADDR instruction is always used with the JMP instruction. The label can be anywhere in the code outside the four lines of code specified for the JMP instruction.

**Note 1:** The JMP instruction must be followed by three DSP Clock Cycles of NOPs. The three DSP clock cycles of NOPs allow enough time to fully clear the instruction pipe.

**Note 2:** When the JMP instruction is performed, no other instructions (except NOPs) may be executed on that cycle.

**Note 3:** Due to HW limitations, it is up to the developer to guarantee that all JMP instructions occur within the first 1K for the TAS3108 and TAS3204, and within the first 2K for TAS3208, TAS3308.

**Syntax:**

<table>
<thead>
<tr>
<th>Opcode:</th>
</tr>
</thead>
<tbody>
<tr>
<td>10010</td>
</tr>
</tbody>
</table>

**Example 1:**

```
JMP | NOP | NOP | NOP | PCADDR(PMRK_A) |
    | NOP | NOP | NOP | NOP            |
    | NOP | NOP | NOP | NOP            |
    | NOP | NOP | NOP | NOP            |
< other processing(optional) >
PRMK_A| NOP | NOP | NOP | NOP
```

**Register PC:**

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>PC Address</th>
<th>0</th>
</tr>
</thead>
</table>

| Register Contents 3 Cycles After Instruction Execution | PMRK_A Address | 0 |
4.3.10 LD(mem_addr, reg)

Description:

This instruction executes an unconditional load of the contents of memory address \textit{mem\_addr} into Register \textit{reg}, where \textit{reg} is Register B, L, or MD (for 48 bit Data) or Register MC (for 28 bit Coefficient). \textit{mem\_addr} is 10 bit Data RAM or Coefficient RAM address of the desired register to be loaded.

\textbf{Note:} Data RAM loads belong to Memory Operation Stage 1 Instruction Set, where as Coefficient RAM loads belong to Memory Operation Stage 2 Instruction Set.

\textbf{Important:} Specifying Data RAM loads in Memory Operation Stage 2, or Coefficient loads in Memory Operation Stage 1 is Illegal.

\textbf{Syntax:}

<table>
<thead>
<tr>
<th>Syntax</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD(mem_addr, B)</td>
<td>0 0010</td>
</tr>
<tr>
<td>LD(mem_addr, L)</td>
<td>0 0011</td>
</tr>
<tr>
<td>LD(mem_addr, BL)</td>
<td>1 1100</td>
</tr>
<tr>
<td>LD(mem_addr, MC)</td>
<td>1 1111</td>
</tr>
<tr>
<td>LD(mem_addr, MD)</td>
<td>0 0001</td>
</tr>
</tbody>
</table>

\textbf{Example 1:} NOP | NOP | LD(mem_addr, B) | NOP | NOP

\textbf{Register B:} \textbf{Register mem_addr:}

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Register Contents After Instruction Execution</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFFFF FFFF FFFF 47</td>
<td>0x1234 5678 9ABC 47</td>
</tr>
<tr>
<td>0x1234 5678 9ABC 47</td>
<td>0x1234 5678 9ABC 47</td>
</tr>
</tbody>
</table>
4.3.11 \textit{LDC(mem\_addr, reg)}

\textbf{Description:}

This instruction executes a conditional load of contents of data memory address \textit{mem\_addr} into Register \textit{reg} when the compare instruction results in a logic 1.

Register \textit{reg} can be Register B, L, or MD for 48 bit data or Register MC for 28 bit data.

\textbf{Syntax:}

\begin{align*}
\text{LDC}(\text{mem\_addr}, \text{B}) & \quad \text{Opcode: } 0 \ 0101 \\
\text{LDC}(\text{mem\_addr}, \text{L}) & \quad \text{0 0110} \\
\text{LDC}(\text{mem\_addr}, \text{MD}) & \quad \text{1 0100}
\end{align*}

\textbf{Example 1:}

\begin{align*}
\text{NOP} & \mid \text{NOP} \mid \text{LD}(X\_D, \text{B}) \mid \text{NOP} \mid \text{NOP} \\
\text{NEG}(B) & \mid \text{NOP} \mid \text{LD}(\text{ZERO}\_D, \text{L}) \mid \text{NOP} \mid \text{NOP} \\
\text{THRU}(L) & \mid \text{NOP} \mid \text{NOP} \mid \text{NOP} \mid \text{NOP} \\
\text{NOP} & \mid \text{COMP}(\text{BR},\text{LR}) \mid \text{NOP} \mid \text{NOP} \mid \text{NOP} \\
\text{NOP} & \mid \text{NOP} \mid \text{LNC}(Y\_D, \text{MD}) \mid \text{NOP} \mid \text{NOP} \\
\text{NOP} & \mid \text{NOP} \mid \text{LDC}(Z\_D, \text{MD}) \mid \text{NOP} \mid \text{NOP}
\end{align*}

\textbf{Register MD:}

\textbf{If content of BR = Content of LR}

\begin{center}
\begin{tabular}{|c|c|}
\hline
Register Contents Before Instruction Execution & 31 \ Don't Care \\
\hline
Register Contents After Instruction Execution & 31 \ Contents of Z\_D \\
\hline
\end{tabular}
\end{center}

\textbf{If Operand A \neq \text{Operand B}}

\begin{center}
\begin{tabular}{|c|c|}
\hline
Register Contents Before Instruction Execution & 31 \ Don't Care \\
\hline
Register Contents After Instruction Execution & 31 \ Contents of Y\_D \\
\hline
\end{tabular}
\end{center}
4.3.12 LNC(D_addr, reg)

Description:
This instruction executes a conditional load of contents of data memory address mem_addr into Register reg when the compare instruction results in a logic 0.

Register reg can be Register B, L, or MD for 48 bit data or Register MC for 28 bit data.

Note: Data RAM loads belong to Memory Operation Stage 1 Instruction Set, where as Coefficient RAM loads belong to Memory Operation Stage 2 Instruction Set.

Important: Specifying Data RAM loads in Memory Operation Stage 2, or Coefficient loads in Memory Operation Stage 1 is Illegal.

Syntax: 

- LNC(D_addr, B)  
- LNC(D_addr, L)  
- LNC(D_addr, MD)  
- LNC(D_addr, MD)  

Example 1: 

```
NOP | NOP | LD(X_D, B) | NOP | NOP
NEG(B) | NOP | LD(ZERO_D, L) | NOP | NOP
THRU(L) | NOP | NOP | NOP | NOP
NOP | COMP(BR,LR) | NOP | NOP | NOP
NOP | NOP | LNC(Y_D, MD) | NOP | NOP
NOP | NOP | LDC(Z_D, MD) | NOP | NOP
```

Register MD:

If content of BR = Content of LR

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>31</th>
<th>Don't Care</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>31</td>
<td>Contents of Z_D</td>
<td>0</td>
</tr>
</tbody>
</table>

If content BR ≠ Content of LR

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>31</th>
<th>Don't Care</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>31</td>
<td>Contents of Y_D</td>
<td>0</td>
</tr>
</tbody>
</table>
4.3.13 LOG2

Description:

This instruction computes the approximate Base 2 Logarithm of the data in Register L. The result of this instruction is available in the Register LR on the start of the next DSP clock cycle.

The input is in linear space (25.23 precision unsigned number) with a range of 0.0000 to approximately 16777216. The output is in base 2 log space (5.4 precision unsigned number)

Note: The base 2 logarithm is only available for the contents of Register L

Syntax: LOG2(L)  Opcode: 00100

Example 1: LOG2(L) | NOP | NOP | NOP | NOP

Register L:                         Register LR

| Register Contents Before Instruction Execution | 0x2000 0000 0000       | Register Contents Before Instruction Execution | Don’t Care |
| Register Contents After Instruction Execution | 0x2000 0000 0000       | Register Contents After Instruction Execution | 0x0000 00F8 0000 |

Example 2: LOG2(L) | NOP | NOP | NOP | NOP

Register L:                         Register LR

| Register Contents Before Instruction Execution | 0x0080 0000 0000       | Register Contents Before Instruction Execution | Don’t Care |
| Register Contents After Instruction Execution | 0x0080 0000 0000       | Register Contents After Instruction Execution | 0x0000 03F8 0000 |
### 4.3.14 NEG (reg)

**Description:**
This instruction computes the 2’s Complement on the value of the data in Register B or Register L. The result of this instruction is available in the BR or LR register on the start of the next DSP clock cycle.

**Syntax:**
- NEG(B)
- NEG(L)

**Opcode:**
- NEG(B) 00010
- NEG(L) 00011

**Example 1:**
**NEG(B) | NOP | NOP | NOP | NOP**

- **Register B:**
  - Register Contents Before Instruction Execution: \(0xFF FF 80 00 00\)
  - Register Contents After Instruction Execution: \(0xFF FF 80 00 00\)

- **Register BR:**
  - Register Contents Before Instruction Execution: \(0\)
  - Register Contents After Instruction Execution: \(47\)

**Example 2:**
**NEG(L) | NOP | NOP | NOP | NOP**

- **Register L:**
  - Register Contents Before Instruction Execution: \(0xFF FE 80 00 00\)
  - Register Contents After Instruction Execution: \(0xFF FE 80 00 00\)

- **Register LR:**
  - Register Contents Before Instruction Execution: \(0\)
  - Register Contents After Instruction Execution: \(47\)
4.3.15 NOP

Description:
This instruction does not execute any operation

Syntax: NOP
Opcode: 00000

Example 1: NOP | NOP | NOP | NOP | NOP

All Registers:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Don't Care</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Register Contents After Instruction Execution</th>
<th>Unchanged</th>
</tr>
</thead>
</table>
4.3.16 SHL (bits)

Description:
This instruction shifts the contents of Register B by the number of bits specified. The result is available in Register BR at the start of the next DSP clock cycle.

Note: Shift right operations are only available for the contents of Register B.

Syntax:

SHL (1)  Opcode: 01010
SHL (2)  00111
SHL (3)  01100
SHL (4)  01101
SHL (20)  10110

Example 1:  SHL (1) | NOP | NOP | NOP | NOP

Register B:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>0x0000 0080 0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>0x0000 0080 0000</td>
</tr>
</tbody>
</table>

Register BR:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Don’t Care</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>0x0000 0100 0000</td>
</tr>
</tbody>
</table>

Example 2:  SHL (20) | NOP | NOP | NOP | NOP

Register B:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>0x0000 0000 0008</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>0x0000 0000 0008</td>
</tr>
</tbody>
</table>

Register BR:

<table>
<thead>
<tr>
<th>Register Contents Before Instruction Execution</th>
<th>Don’t Care</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register Contents After Instruction Execution</td>
<td>0x0000 0008 0000</td>
</tr>
</tbody>
</table>
4.3.17 SHR (bits)

Description:
This instruction shifts the contents of Register B by the number of bits specified. The result is available in Register BR at the start of the next DSP clock cycle.

Note: Shift right operations are only available for the contents of Register B.

Syntax: SHR(1) Opcode: 00100
SHR(2) 00111
SHR(3) 01000
SHR(4) 01001

Example 1: SHR (3) | NOP | NOP | NOP | NOP
Register B: | Register BR

Example 2: SHR (4) | NOP | NOP | NOP | NOP
Register B: | Register BR
4.3.18  \textit{ST(reg, COEF, mem_addr)}

\textbf{Description:}

This instruction stores the lower 28 bits contents of Register L, B, or MD into the 10 bit coefficient RAM address \textit{mem_addr}.

\textbf{Syntax:}

\begin{itemize}
  \item ST(L,COEF,C_addr) \quad \textit{Opcode:} 0110
  \item ST(L, COEF, C_addr) \quad 0111
  \item ST(B, COEF, C_addr) \quad 1000
\end{itemize}

\textbf{Example 1:}  \quad \text{NOP | NOP | NOP | NOP | ST(L, COEF, VAR1_C)}

\textbf{Data Ram Register VAR1_C:} \quad \textbf{Register L}

\begin{itemize}
  \item Register Contents Before Instruction Execution \quad \text{Don't Care} \quad 0
  \item Register Contents After Instruction Execution \quad 0x678 9123 \quad 0
\end{itemize}
4.3.19 ST(DI, DATA, mem_addr)

Description:

This instruction stores the contents of Register DI (Digital Audio Data Input) into the 10 bit data RAM address mem_addr.

Register DI is a special register used to access audio data received by the DSP. The ST(DI, DATA,D_addr) instruction copies data from DI into Data RAM for later processing.

Note: The TAS3xxx least three least significant bits of the data RAM address indicate which input channel is copied to memory.

Syntax: \text{ST(DI,DATA,D\_addr)} \quad \text{Opcode: 0110}

Example 1: \text{NOP | NOP | NOP | NOP | ST(DI, DATA, SDIN1L\_D)}

\text{NOP | NOP | NOP | NOP | ST(DI, DATA, SDIN1R\_D)}

Data RAM Register SDIN1L\_D: Data RAM Register SDIN1R\_D
4.3.20 ST(DLYO, DATA, mem_addr)

Description:

This instruction stores the contents of Register DLYO (Delay Memory Out) into the 10 bit data memory address mem_addr.

Register DLYO is a special register used to access delayed audio data samples from the delay memory. There must be 13 cycles between the delay pointer instruction DLYPTR and the ST instruction. These 13 cycles can either contain NOPs or other processing if required.

Syntax: ST(DLYO,DATA,D_addr)         Opcode: 0100

Example 1: NOP | CLRACC | LD(DelayIn1_D,L,NONE) | NOP | NOP
            THRU(L) | NOP | NOP | NOP | NOP
            NOP | NOP | ADD(ACC, LR, NONE, DELYI) | NOP | DLYPTR(0)
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            NOP | NOP | NOP | NOP | NOP
            ST(DLYO,DATA,DelayOut1_D)

Register DLYO:  Data RAM Register DelayOut1_D

| Register Contents Before Instruction Execution | Audio Data | 47 | 0 |
| Register Contents After Instruction Execution | Audio Data | 47 | 0 |

| Register Contents Before Instruction Execution | Don’t Care |
| Register Contents 2 Cycles After Instruction Execution | Audio Data |
| 47 | 0 |
### 4.3.21 \texttt{ST}(\textit{reg}, \textit{DATA}, \textit{mem\_addr})

**Description:**

This instruction stores the contents of Register \textit{reg} into Data memory address \textit{mem\_addr}.

Register \textit{reg} is Register B, L, or MD. \textit{mem\_addr} is a 10 bit Data RAM address

**Note:** Data RAM loads belong to Memory Operation Stage 1 Instruction Set, whereas Coefficient RAM loads belong to Memory Operation Stage 2 Instruction Set.

**Important:** Specifying Data RAM loads in Memory Operation Stage 2, or Coefficient loads in Memory Operation Stage 1 is Illegal.

**Syntax:**

\begin{align*}
\text{ST}(\textit{L}, \textit{DATA}, \textit{mem\_addr}) & \quad \text{Opcode:} \quad 0011 \\
\text{ST}(\textit{MD}, \textit{DATA}, \textit{mem\_addr}) & \quad 0001 \\
\text{ST}(\textit{B}, \textit{DATA}, \textit{mem\_addr}) & \quad 0010
\end{align*}

**Example 1:**

\texttt{NOP | NOP | NOP | NOP | ST(B, DATA, VAR1\_D)}

**Register B:**

\textbf{Register Contents Before Instruction Execution:} 0x1234 5678 9123

\textbf{Register Contents After Instruction Execution:} 0x1234 5678 9123

**Register VAR1\_D**

\textbf{Register Contents Before Instruction Execution:} Don't Care

\textbf{Register Contents After 2 Cycles of Instruction Execution:} 0x1234 5678 9123
4.3.22 STOP

Description:
This instruction halts the Program Counter.

Important: Every DSP assembly program must have at least one STOP instruction (usually at the end of the program).

Note: If a Left/Right Clock error occurs at the same time as execution of the STOP instruction, the PC may miss the STOP instruction and erroneously continue. To guard against this, the following example shows a defensive programming technique to ensure that the Stop instruction is correctly executed.

Syntax: STOP

Opcode: 10101

Example 1: BRANCH_PT | NOP | NOP | NOP | NOP
STOP | NOP | NOP | NOP | PCADDR(BRANCH_PT)
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
NOP | NOP | NOP | NOP | NOP
JMP | NOP | NOP | NOP | PCADDR(BRANCH_PT)
4.3.23 THRU

Description:
This instruction copies the contents of Register B to Register BR or the contents of Register L to Register LR.

Syntax:
- THRU (B)  
- THRU (L)  

Opcode:
- THRU (B): 10000
- THRU (L): 10001

Example 1: THRU (B) | NOP | NOP | NOP | NOP

Register B:    Register BR

Example 2: THRU (L) | NOP | NOP | NOP | NOP

Register L:    Register LR