

TAS5731M Care abouts

by Kes Tam

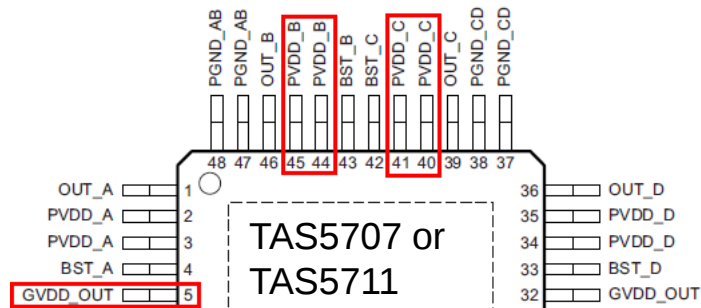
kes-tam@ti.com



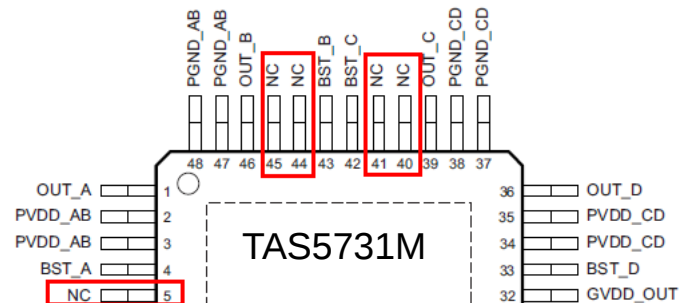
Difference from TAS5707/11

- TAS5731M (and those new IC like TAS5751M) uses a new power stage design.
- The number of PVDD is reduced from four to two.

In TAS5707/11, pin 45/46 are PVDD_B, pin 40/41 are PVDD_C.



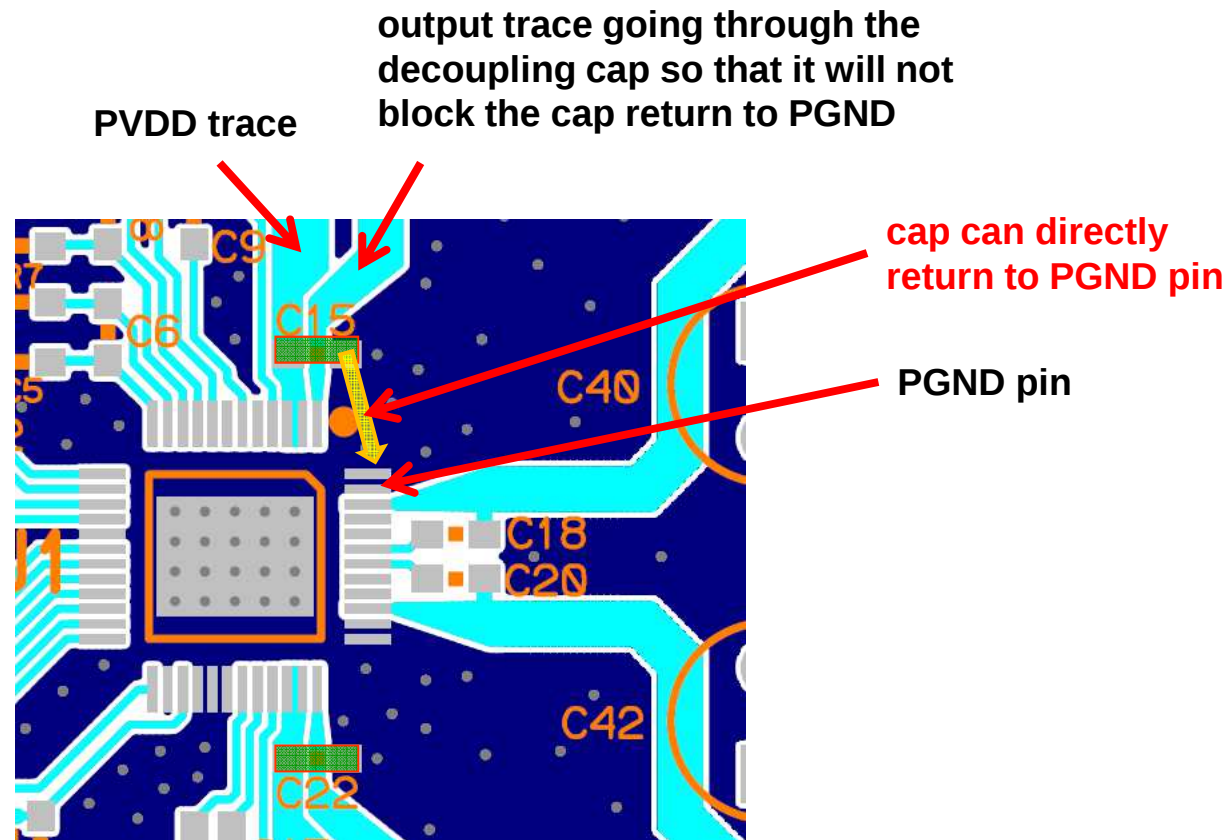
In TAS5731M, pin 40/41 and 45/46 are now NC.



- TAS5731M output power is bigger.
- For these two reasons, we need much better decoupling in the rest two PVDD.

PVDD decoupling cap

- To have the best decoupling on PVDD, the decoupling cap are needed to be closed to the IC PVDD and PGND pin. The connection should be direct without going through any vias.



- The rest of layout care abouts will follow the same as TAS5707/11.

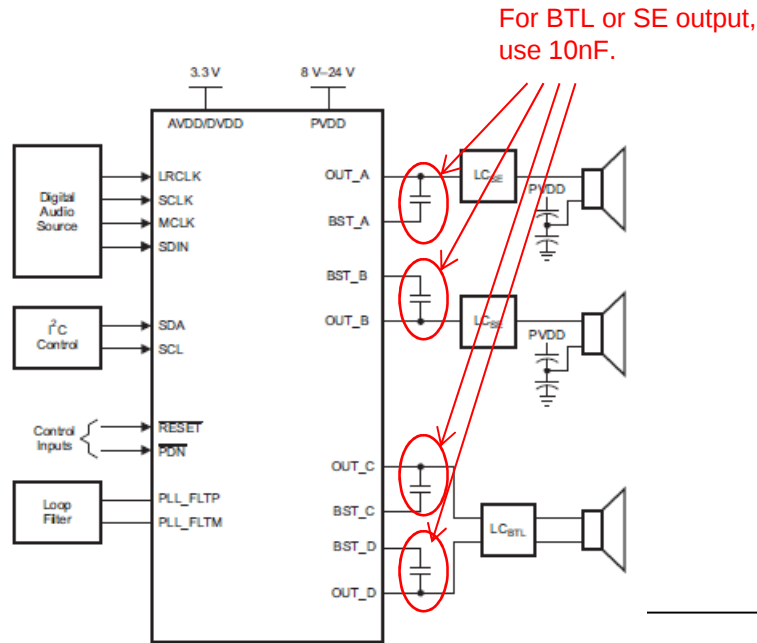


Two stage gate drive

- The new TAS5731M power stage is using a two stage gate drive. A two stage gate drive will first drive the gate to half the gate voltage and then complete driving the gate in the second stage. This makes the voltage ramping slower so that the spike/overshoot in both PVDD and output can be reduced. This allows the device can be used for a higher supply voltage.
- The two stage gate drive takes more time to complete in comparing with the one stage gate drive. So, the max. modulation cannot be too high which will not give sufficient time to complete the driving.
- It requires to set reg 0x10 = 0x07 to reduce the max. modulation to the minimum 93.8%.

Two stages gate drive

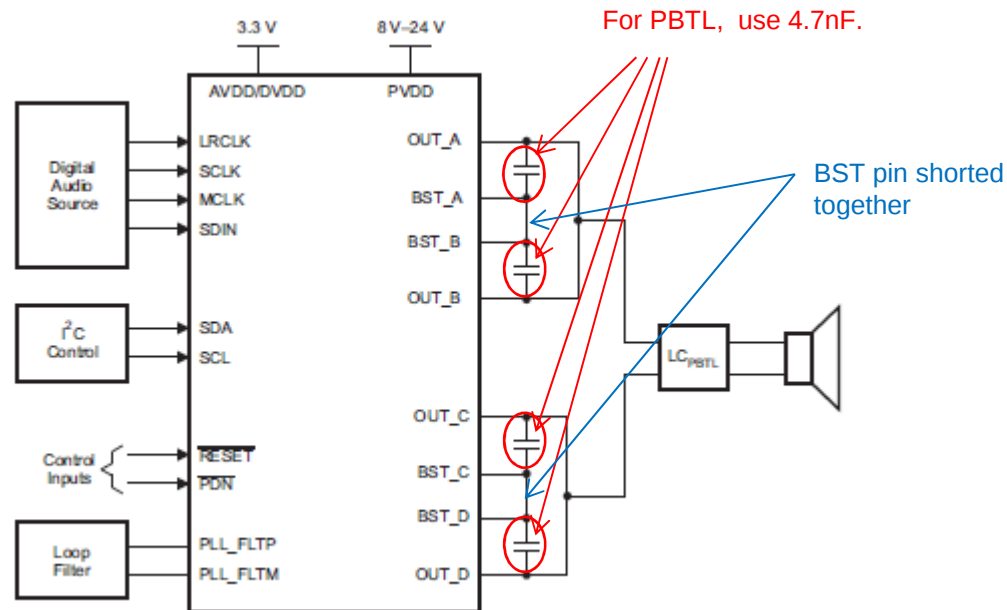
- The first stage gate drive ramping is very slow which leaves a much shorter time for the second stage gate driving.
- If keep using the 33nF BST cap as other TAS57xx device, the charging time will not be enough in the second stage gate drive. So, it requires to reduce the BST cap value to a smaller value in order to complete the charging.
- TAS5731M BST cap are now changed to 10nF in TAS5731M.**



00204-25

PBTL

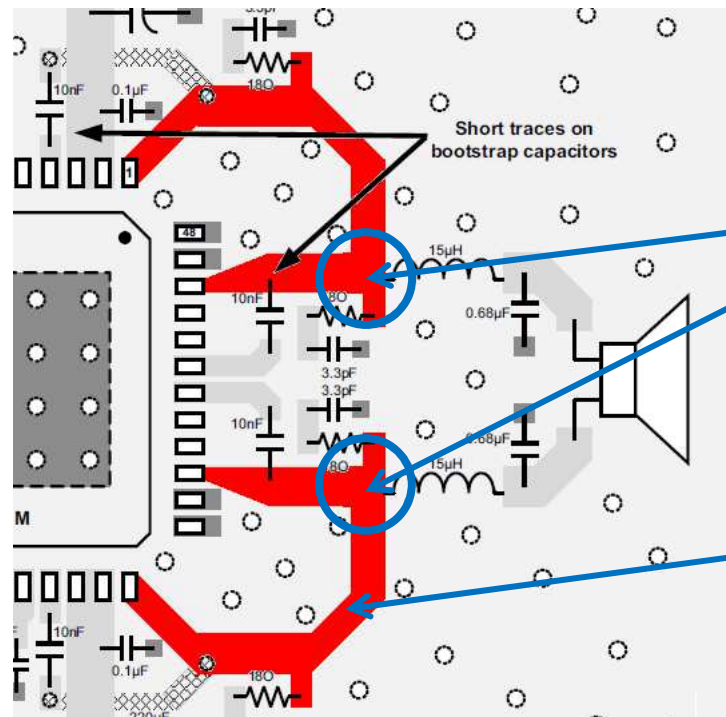
- The new power stage in TAS5731M needs better synchronization in PBTL before inductor to avoid current flowing back within the two parallel channels.
- To do this, it needs to short the BST pins of the two parallel channels.
- The BST cap are changed to 4.7nF so that two cap in parallel will give back the approximate 10nF.



00064-08

PBTL

- To further reduce the risk on the current flow back between two parallel channels. It is suggested to make the output traces shorted in the inductor end. This will make the traces longer. The traces can be acted as a very tiny inductor which suppress current flow in PWM rising and falling.



Output traces shorted in the inductor side

Trace is longer so that it can be acted as a tiny inductor to prevent transient current flow back.



PBTL

- TAS5731 and TAS5731M uses same DSP as TAS5711. But, the power stage input mux is different. The DSP output to power stage input mapping is needed to be adjusted in PBTL.
- To unify TAS5711/TAS5731/TAS5731M DSP to power stage mapping in PBTL, write reg 0x25 = 0x01 00 22 45 and reg 0x19 = 0x3A. This setting can work for all TAS5711, TAS5731 and TAS5731M.