TAS5754/56M Function Block Diagram





TAS5754/56M Processing Options

Feature	HybridFlow 1	HybridFlow 2	HybridFlow 3	HybridFlow 4	HybridFlow 5	HybridFlow 6	HybridFlow 7
Supported Output Configurations			°	0	000		
Typical Target Application	Mid-Level DTVs & General Audio	Mid-Level DTVs & General Audio	Bi-Amped Bluetooth® and Active Speakers	Bluetooth Speakers and Wireless Subs	Hi-End Digital TVs	Docking Stations, All-in-One PC, & General Audio	Mid-Level DTVs, Soundbars, & General Audio
Supported Sample Rate	8–48 kHz	8–48 kHz	8–48 kHz	8–48 kHz	8–192 kHz	8–48 kHz	8–96 kHz
Psychoacoustic Bass Enhancer (PBE)	1	x	1	1	x	x	x
Output Configurations (Stereo/Mono)	Stereo	Stereo	1.1	Mono	Stereo	Stereo	Stereo
DRC Type	3-Band Compander	3-Band Compander	3-Band Compander	3-Band Compander	DRC-Lite	3-Band Compander	3-Band Compander
Biquad Equalizers (In Full- Range Path)	2 × 12	2 × 12	1 × 10 + 1 × 5	1 × 12	2 × 1	2 × 15	2 × 5
PurePath SmoothClip	1	1	1	1	1	1	√
Sound Field Spatializer (SFS)	x	x	x	x	x	1	x
Dynamic Dialog Enhancer (DDE)	x	1	x	x	x	x	x
Dynamic Bass Enhancer (DDE)	1	1	1	1	x	1	x
Serial Audio Data Out (Subwoofer, Full-Range)	FR	SW or FR	SW or FR	FR	SW or FR	FR	FR

Register Page & Header File Structure



Register Page Structure

Register Page Structure

Page:	0	1	2-43	44-52	53-61	62-70	71-151	152-186
Func:	Control	Analog Control	q	Coeffient A	q	Coeffient B	q	Instruction
Desc:	General Control and Configuration	Analog Control	Reserve	256 24-bit coefficients, 30 coefficients per page, 4 registers per coefficient	Reserve	256 24-bit coefficients,30 coefficients perpage,4 registers percoefficient	Reserve	1024 24-bit instructions, 30 instructions per page, 4 registers per instruction



Coefficient Buffer A & B Map

Coeff NO	Page NO	Base Register	Base Register+0	Base Register+1	Base Register+2	Base Register+3
C0	44	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	44	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C29	44	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	45	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C59	45	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	46	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C89	46	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C90	47	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C119	47	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C120	48	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C149	48	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C150	49	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C179	49	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C180	50	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C209	50	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C210	51	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C239	51	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C240	52	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C255	52	68	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.



Header / CFG File Structure

Content Comment				
	Put TAS5754 into standby mode and mute the device.			
Page 0 -1	General control and analog control			
Page 44 - 52	Coefficient A (C-RAM)			
Page 62 - 70	Coefficient B (C-RAM)			
Page 152 - 169	Instruction (I-RAM)			
	Post-Initialization: Enable adaptive mode. Wake up and unmute the device.			



How to Dump CFG / Header File



Step 1

- 1. Make sure PPCMB is connected to PC.
- 2. Load your xml file into PPC2.
- 3. Click download button to start running the hybrid flow.

Configure Audio Processing System Build PPCMB Audio I/O: USB Sample Rate: 48kHz Mono HybridFlow: No HybridFlow Mono HybridFlow: No HybridFlow Mode: Basic	
PPCMB Audio I/O: USB Sample Rate: 48kHz Stereo HybridFlow: HybridFlow 1 Mode: Basic	
Mono HybridFlow: No HybridFlow	
	_
Storeo Dovico	
Input Source: Carial Audio free DDCMR	
SDOUT Origin: Doct-DSD	
Serial Audio Data Format	
Serial Audio Word Length 24 bits	
Swap A/B Data	8
Auto-detect Clocks	
Error Handling Status 32-48	
Monitor for AVDD UVE	
Monitor for f _s Errors Z Detected MCLK [MHz]	
Monitor for SCLK Errors 20 3.072	
Monitor for Mick Errors V Detected scck [min2] Monitor for Missing MCLK V	
Monitor for Missing LRCK/FSs or SCLKs 🛛 Audio Data Status	
Monitor for PLL Lock Errors Z Amp Status	
Missing Clock Detection Period	
	4
Connected to device FWIDPUREPATH-CMBEVM-REVF	



Step 2

- 1. Stop the hybrid flow from running.
- 2. Switch to Advanced mode.

Prochoose "Direct I2C Read / Wrte" Page	
Configure Audio Processing Direct I ² C Read/Write Registers System Build Direct I ² C Read/Write Data	Device Settings
Page Register -	FWID Firmware Volume Controls [dB]
Read Write	Destination File Burst 1 Format .h Dump
Output Command Buffer Interface	14 14 10 18 Out B Out A Fine Image: Status 32-48 Detected f _a [KHz] 12.288
Clear	3.072 3.072 Detected SCLK [MHz] OK Audio Data Status OK Amp Status OK Clock Status
Connected to device FWIDPUREPATH-CMBEVM-REVF	Load Settings Save Settings View Log Logging



Step 3

- 1. Select the right destination, burst length and format in the Register Dump.
- 2. Click the dump button to start dumping.

A PurePath Console		
Configure Audio Processing Direct I ² C Read/Write Registers System Build Direct I ² C Read/Write Data Page Register	Device Settings Stereo • 0x98 (152 dec) FWID Firmware	Mode: Advanced Stereo OUT
Read Write	Register Dump Destination File Burst 1 Format .h Dump	
Output Dumping Memory typedef unsigned char cfg_u8; typedef union { cfg_u8 offset; cfg_u8 value; ;; ;cfg_u8 param; ; cfg_u8 param;	Load Save	14 14 10 E Out B Out A Fine ● ● Gang A&B Status 32-48 Detected fs [kHz] 12.288 Detected MCLK [MHz] 3.072 Detected SCLK [MHz] OK Audio Data Status OK Amp Status OK Clock Status
Connected to device FWIDPUREPATH-CMBEVM-REVF	Load Settings Save Settings	View Log Logging





1. Fix the P0-R42 value if it is set to 0x00.

🔚 HF1_burst1_fix.cfg 🗵 64 w 98 19 00 65 w 98 1a 80 66 w 98 1b 00 w 98 1c 00 w 98 1d 00 w 98 1e 00 w 98 1f 04 w 98 20 00 w 98 21 00 w 98 22 00 w 98 23 01 74w 98 24 00 w 98 25 00 w 98 26 f3 w 98 27 04 w 98 28 02 80 w 98 29 00 #w 98 2a 00 #Anglog Mute 81 w 98 2a 11 83 w 98 2b 1f w 98 2c 00 84 w 98 2d 00 w 98 2e 00 87 w 98 2f 00

🔚 hf 1-burst 1_fix.h 🛽	3
100	$\{ 0x22, 0x00 \},$
101	{ 0x23, 0x01 },
102	$\{ 0x24, 0x00 \},$
103	$\{ 0x25, 0x00 \},$
104	{ 0x26, 0xf3 },
105	$\{ 0x27, 0x04 \},$
106	$\{ 0x28, 0x02 \},$
107	{ 0x29, 0x00 },
108	<pre>/*{ 0x2a, 0x00 }, Ananlog Mute */</pre>
109	{ 0x2a, 0x11 },
110	{ 0x2b, 0x1f },
111	$\{ 0x2c, 0x00 \},\$
112	$\{ 0x2d, 0x00 \},$
113	$\{ 0x2e, 0x00 \},$
114	{ 0x2f, 0x00 },
115	$\{ 0x30, 0x00 \},$
116	$\{ 0x31, 0x00 \},$
117	$\{ 0x32, 0x00 \},$
118	$\{ 0x33, 0x00 \},$
119	$\{ 0x34, 0x00 \},$
120	$\{ 0x35, 0x00 \},$
121	$\{ 0x36, 0x00 \},$
122	$\{ 0x37, 0x00 \},$
123	$\{ 0x38, 0x00 \},$



P0-R3 and P0-R42(0x2a)

8.4.2.3 PO-R3

Mute Channel B [4] (R/W)	00000000			
This bit issues soft mute request for the Channel B. The volume will be smoothly ramped down/up to avoid pop/click nois				
Normal volume	0			
Mute	1			
Mute Channel A [0] (R/W)	0000000			
his bit issues soft mute request for the Channel A. The volume will be smoothly ramped down/up to avoid pop/click noise.				
Normal volume	0			
Mute	1			

8.4.2.29 P0-R42

Channel B DAC Data Path [5:4] (R/W)	0000001
These bits control the Channel B audio data path connection.	
Zero data (mute)	0 0
Channel B data	01
Channel A data	10
Reserved (do not set)	11
Channel A DAC Data Path [1:0] (R/W)	000000001
These bits control the Channel A audio data path connection.	-
Zero data (mute)	00
Channel A data	01
Channel B data	10
Reserved (do not set)	11



C-RAM Access





C-RAM Access Table – Adaptive

Status	miniDSP C-RAM Access	Control Interface C-RAM Access
Powered Down	No	Yes (Buffer A and Buffer B)
Powered Up (p44_r1_b1 = 0)	Buffer A only	Buffer B only
Powered Up (p44_r1_b1 = 1)	Buffer B only	Buffer A only

p44_r1_b1 is short for Page 44 / Register 1, Bit 1



C-RAM Access at Power-Down Mode

TAS5754 Powered Down in Adaptive Mode

miniDSP





C-RAM Access at Power-Up Mode

TAS5754 Powered Up in Adaptive Mode (p44 r1 b1 = 0) TAS5754 Powered Up in Adaptive Mode (p44 r1 b1 = 1) miniDSP miniDSP C-RAM C-RAM DAC Buffer DAC Buffer DAC Buffer DAC Buffer В В Α A DAC 'Buffer A' DAC 'Buffer B' DAC 'Buffer A' DAC 'Buffer B' Pages 44 - 52 Pages 62 - 70 Pages 44 - 52 Pages 62 - 70 Control Interface (I²C) Control Interface (I²C)

Page 44 / Register 1 (Hex 0x01)

Dec	Hex	b7	b6	b5	b4	b3	b2	b1	ь0
1	0x01	RSV	RSV	RSV	RSV	ACRM	AMDC	ACRS	ACSW
Reset	Value						0		0

ACRS	Active CRAM Selection (Read Only)
	This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can accessed by serial interface (SPI/I2C)
	0: CRAM A is active and being used by the DSP
	1: CRAM B is active and being used by the DSP
ACSW	Switch Active CRAM
	This bit is used to request switching roles of the two buffers, i.e. switching the active buffer role between CRAM A and CRAM B. This bit is cleared automatically when the switching process completed.
	Default value: 0
	0: No switching requested or switching completed
	1: Switching is being requested

🜵 Texas Instruments

C-RAM Access (Adaptive Mode) Example



