

TAS5782M TDM Configurations (8-ch, 32-bit)

Device Configurations

Device 0:

w 90 00 00
w 90 28 13 #DSP, 32-bit
w 90 29 00 #Channel 0&1

Device 1:

w 92 00 00
w 92 28 13 #DSP, 32-bit
w 92 29 40 #Channel 2&3

Device 2:

w 94 00 00
w 94 28 13 #DSP, 32-bit
w 94 29 80 #Channel 4&5

Device 3:

w 96 00 00
w 96 28 13 #DSP, 32-bit
w 96 29 c0 #Channel 6&7

Note: All the TAS5782M devices share the same TDM bus.

AP Settings

Output Settings (Digital Serial Transmitter)

Configuration:

• Audio

☒ Single Data Line (TDM)
☐ Multiple Data Lines

Channels: ☒ MSB First

Format:

Justification:

Frame Pulse:

Frame Clk: ☐ Invert ☐ Shift Left

Word Width:

Bit Depth: ☐ Dither

• Clocks

Master Clk Source:

Master Clk Rate:

MClk Output: ☒ On ☐ Invert

Bit & Frame Dir:

Frame Clk Rate:

MClk/FClk Ratio:

• Bit Clock Edge Sync

Outs:

Ins:

• Logic

Level:

Outputs: ☒ ON

• Frequency

Scale Freq By:

Bitclk ▶

Frame ▶

Data1 ▶

LSB MSB Ch1 LSB MSB

Close Help