TAS57xx PCB Layout Guideline

TAS57xx PCB Layout Guidelines

Class-D switching edges are fast and switched currents are high so it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet audio, thermal and EMC requirements.

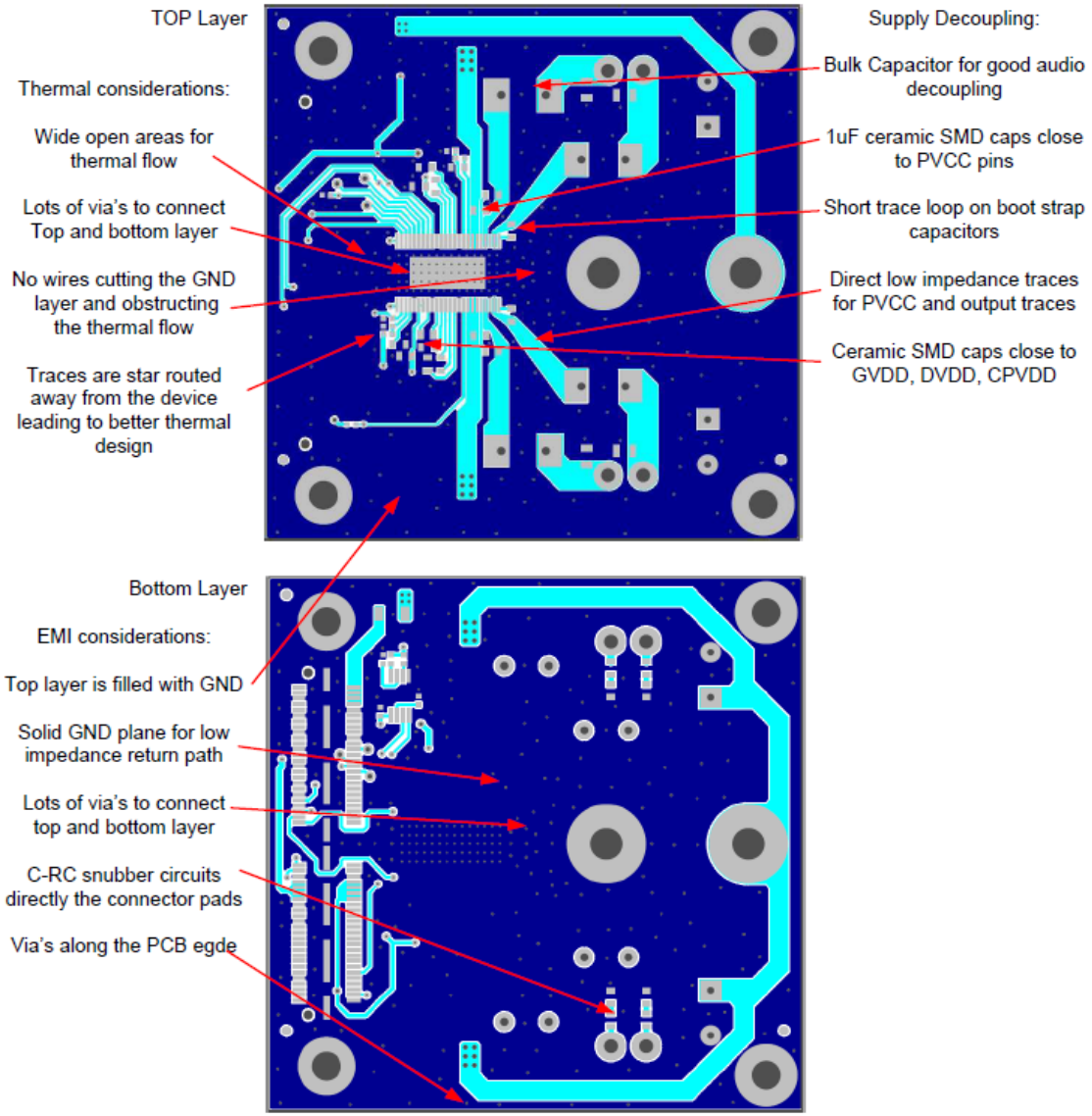
- TAS57xxM uses the PCB for heat sinking therefore the PowerPAD needs to be soldered to the PCB and adequate copper area and copper vias connecting the top, bottom and internal layers must be used.
- Decoupling capacitors: the high-frequency decoupling capacitors must be placed as close to the supply pins as possible; on the TAS57xx, a high-quality ceramic capacitor is used. Large bulk power supply decoupling capacitors must be placed near the TAS57xx on the PVDD supplies.
- Keep the current loop from each of the outputs through the output inductor and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding: A big common GND plane is recommended. The PVDD decoupling capacitors must connect to GND. The TAS57xx PowerPAD must be connected to GND.
- Output filter: remember to select inductors that can handle the high short circuit current of the device. The LC filter must be placed close to the outputs.

TAS57xx PCB Layout Guidelines -Thermal

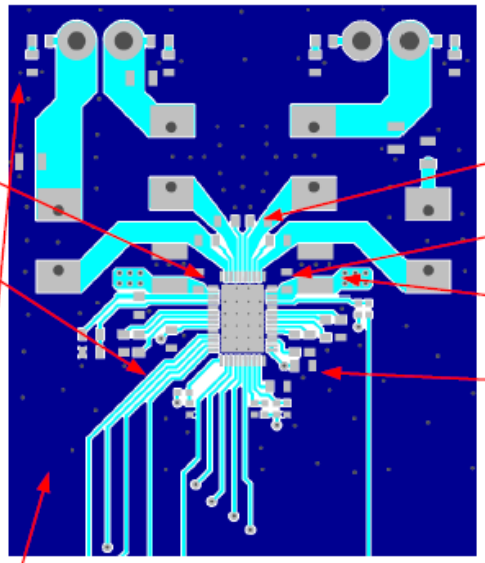
Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed.

- Avoid placing other heat-producing components or structures near the amplifier (including above or below in the end equipment).
- Use a higher layer count PCB if possible to provide more heat sinking capability for the TAS57xx device and to prevent traces of copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS57xx device away from the edge of the PCB when possible to ensure that heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS57xx device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS57xx device. Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

TAS57xx – HTTSOP PCB Layout Example



TAS57xx – VQFN PCB Layout Example



TOP Layer

Thermal considerations:

Connect thermal pad to top GND plane at the corners

Traces are star routed away from the device leading to better thermal design

Supply Decoupling:

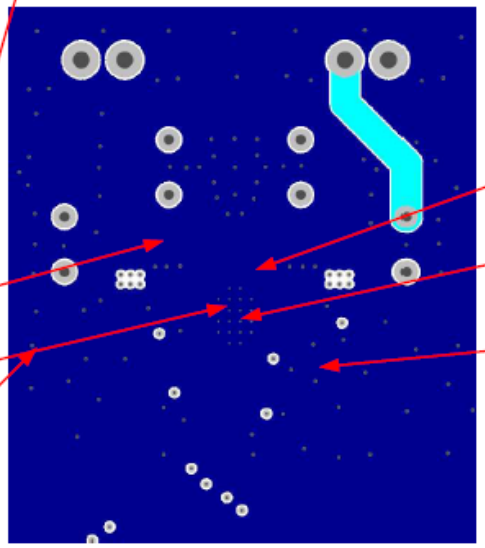
Bulk Capacitor for good audio decoupling

Short trace loop on boot strap capacitors

1uF ceramic SMD caps close to PVCC pins

Direct low impedance traces for PVCC and output traces

Ceramic SMD caps close to GVDD, DVDD, CPVDD



Bottom Layer

EMI considerations:

C-RC snubber circuits directly the connector pads

Top layer is filled with GND

Solid GND plane for low impedance return path

Lots of via's to connect top and bottom layer

Via's along the PCB egde

Thermal considerations:

Wide open areas for thermal flow

Lots of via's to connect Top and bottom layer

No wires cutting the GND layer and obstructing the thermal flow