TAS5805M Trouble Shooting (Draft)

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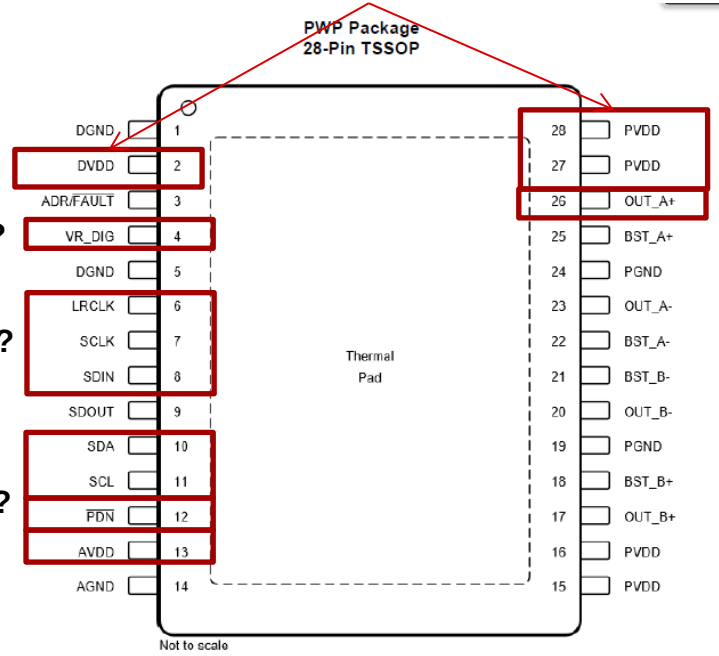
Hardware checking

6. DVDD? PVDD?



1. 1.5V?

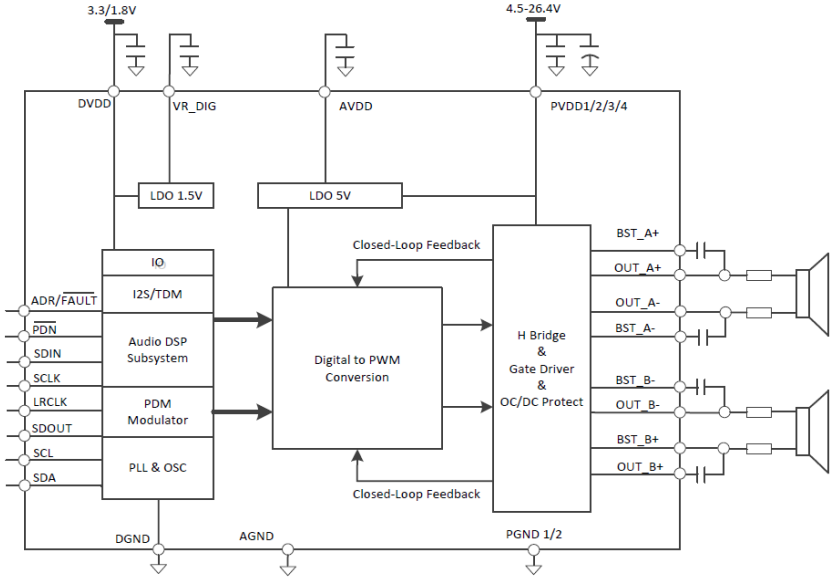
2. Valid?

3. i2C?

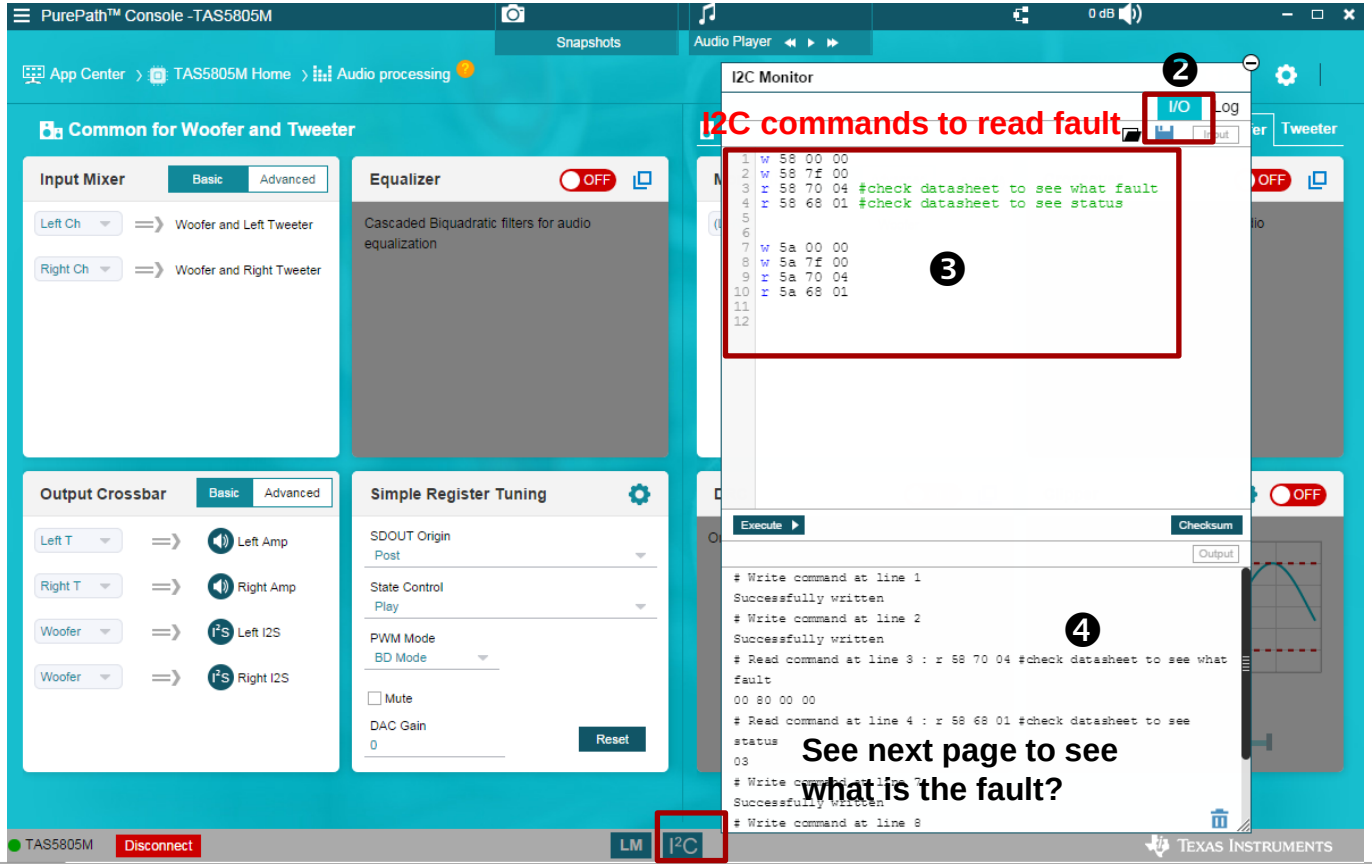
4. High?

5. 5V?

7. PWM?



Software debug



Global fault and status of TAS5805

9.6.1.36 CHAN_FAULT Register (Offset = 70h) [reset = 0x00]

CHAN_FAULT is shown in Figure 134 and described in Table 42.

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Figure 134. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1_DC_1	CH2_DC_1	CH1_OC_I	CH2_OC_I
R				R	R	R	R

Table 42. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	This bit is reserved
3	CH1_DC_1	R	0	Left channel DC fault
2	CH2_DC_1	R	0	Right channel DC fault
1	CH1_OC_I	R	0	Left channel over current fault
0	CH2_OC_I	R	0	Right channel over current fault

9.6.1.37 GLOBAL_FAULT1 Register (Offset = 71h) [reset = 0h]

GLOBAL_FAULT1 is shown in Figure 135 and described in Table 43.

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Figure 135. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
OTP_CRC_ERROR	BQ_WR_ERROR				CLK_FAULT_I	PVDD_OV_I	PVDD_UV_I
R	R				R	R	R

Table 43. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTP_CRC_ERROR	R	0h	Indicate OTP CRC check error.
6	BQ_WR_ERROR	R	0h	The recent BQ is written failed
5-3	RESERVED	R	0h	This bit is reserved
2	CLK_FAULT_I	R	0h	Clock fault
1	PVDD_OV_I	R	0h	PVDD OV fault
0	PVDD_UV_I	R	0h	PVDD UV fault

9.6.1.38 GLOBAL_FAULT2 Register (Offset = 72h) [reset = 0h]

GLOBAL_FAULT2 is shown in Figure 136 and described in Table 44.

Return to Summary Table.

Figure 136. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		OTSD_I
R					R		R

Table 44. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000	This bit is reserved
0	OTSD_I	R	0	Over temperature shut down fault

9.6.1.39 OT WARNING Register (Offset = 73h) [reset = 0x00]

OT_WARNING is shown in Figure 137 and described in Table 45.

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Figure 137. OT_WARNING Register

7	6	5	4	3	2	1	0
RESERVED			RESERVED		OTW	RESERVED	
R			R		R	R	R

Table 45. OT_WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	This bit is reserved
5-3	RESERVED	R	000	This bit is reserved
2	OTW	R	0	Over temperature warning ,135C
1-0	RESERVED	R	00	This bit is reserved

9.6.1.28 POWER_STATE Register (Offset = 68h) [reset = 0x00]

POWER_STATE is shown in Figure 126 and described in Table 34.

Return to Summary Table.

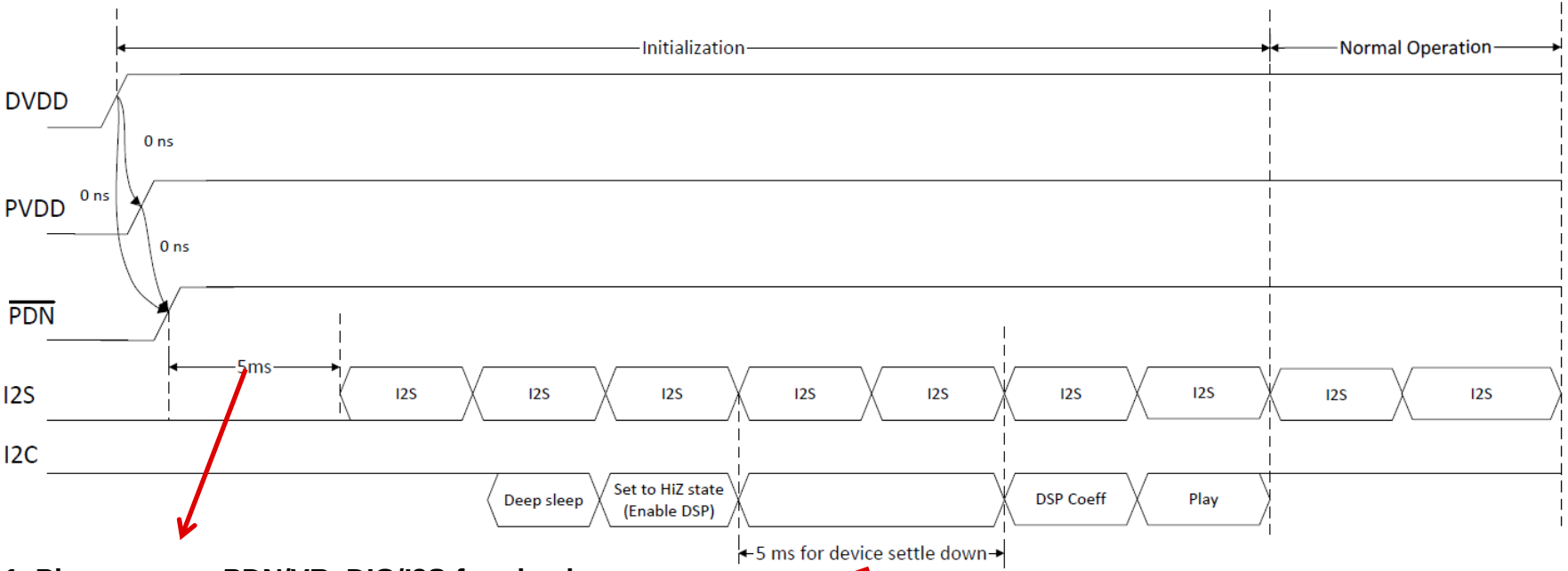
Figure 126. POWER_STATE Register

7	6	5	4	3	2	1	0
STATE_RPT							
R							

Table 34. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STATE_RPT	R	00000000	0: Deep sleep 1: Sleep 2: HIZ 3: Play Others: reserved

Power on sequence check



1. Please scope PDN/VR_DIG/I2S for check;

2. Please scope I2C/I2S/PDN for trouble shooting

Further trouble shooting

- After you finish steps above, if anything is wrong, please debug;
- If everything above is ok, please email to me.