TAS58xxM TDM Configurations (16-ch, 32-bit)

Register Setting

Register 0x33

Table 15. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2S_SHIFT_MSB	R/W	0	I2S Shift MSB
6	RESERVED	R/W	0	This bit is reserved
5-4	DATA_FORMAT	R/W	00	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_LRCLK_PULSE	R/W	00	01: lrclk pulse < 8 SCLK
1-0	WORD_LENGTH	R/W	10	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

Register 0x34

Table 16. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2S_SHIFT	R/W	00000000	I2S Shift LSB These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample. 000000000: offset = 0 SCLK (no offset) 000000001: ofsset = 1 SCLK 000000010: offset = 2 SCLKs and 111111111: offset = 512 SCLKs

Device Configurations (1 / 2)

Device 0:

```
w 98 00 00
w 98 7f  00
w 98 33 17    #TDM/DSP, 32-bit
w 98 34 00    #Channel 0&1
```

Device 1:

```
w 98 00 00
w 98 7f  00
w 98 33 17    #TDM/DSP, 32-bit
w 98 34 40    #Channel 2&3
```

Device 2:

```
w 98 00 00
w 98 7f  00
w 98 33 17    #TDM/DSP, 32-bit
w 98 34 80    #Channel 4&5
```

Device 3:

```
w 98 00 00
w 98 7f  00
w 98 33 17    #TDM/DSP, 32-bit
w 98 34 c0    #Channel 6&7
```

Note: All the TAS58xxM devices share the same TDM bus.

Device Configurations (2 / 2)

Device 4:

```
w 98 00 00
w 98 7f  00
w 98 33 97    #TDM/DSP, 32-bit
w 98 34 00    #Channel 8&9
```

Device 5:

```
w 98 00 00
w 98 7f  00
w 98 33 97    #TDM/DSP, 32-bit
w 98 34 40    #Channel 10&11
```

Device 6:

```
w 98 00 00
w 98 7f  00
w 98 33 97    #TDM/DSP, 32-bit
w 98 34 80    #Channel 12&13
```

Device 7:

```
w 98 00 00
w 98 7f  00
w 98 33 97    #TDM/DSP, 32-bit
w 98 34 c0    #Channel 14&15
```

Note: All the TAS58xxM devices share the same TDM bus.