Functional Safety Information

TAS6424E-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TAS6424E-Q1 (56-pin DKQ package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

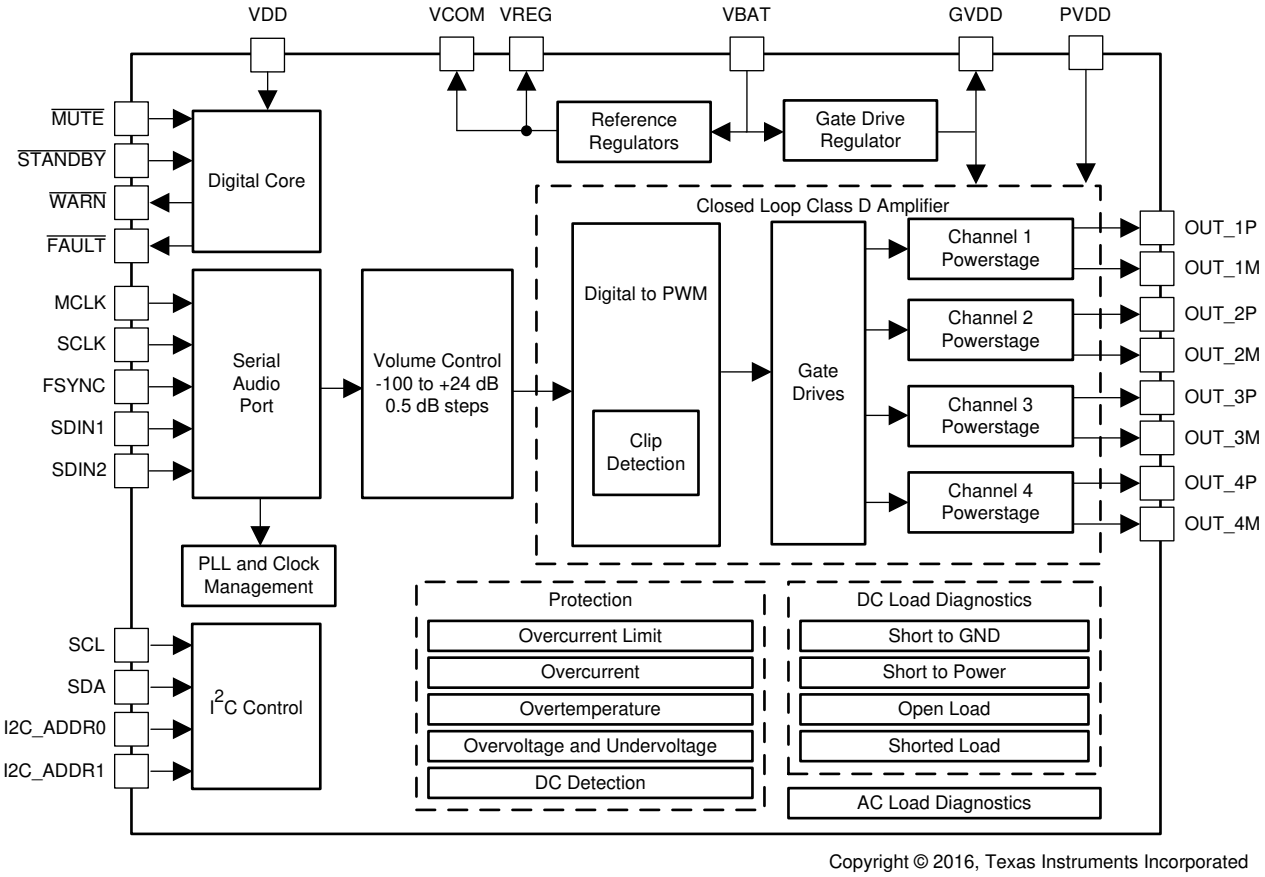

Figure 1-1. Functional Block Diagram

TAS6424E-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TAS6424E-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	55
Die FIT Rate	3
Package FIT Rate	52

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 5000 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =<50V supply	70 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TAS6424E-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Safe failure modes	50%
Unsafe failure modes	50%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TAS6424E-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (PVDD, VBAT or VDD) (see Table 4-5, Table 4-6, Table 4-7)

These scenario tables also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TAS6424E-Q1 pin diagram. For a detailed description of the device pins, refer to the *Pin Configuration and Functions* section in the TAS6424E-Q1 data sheet.

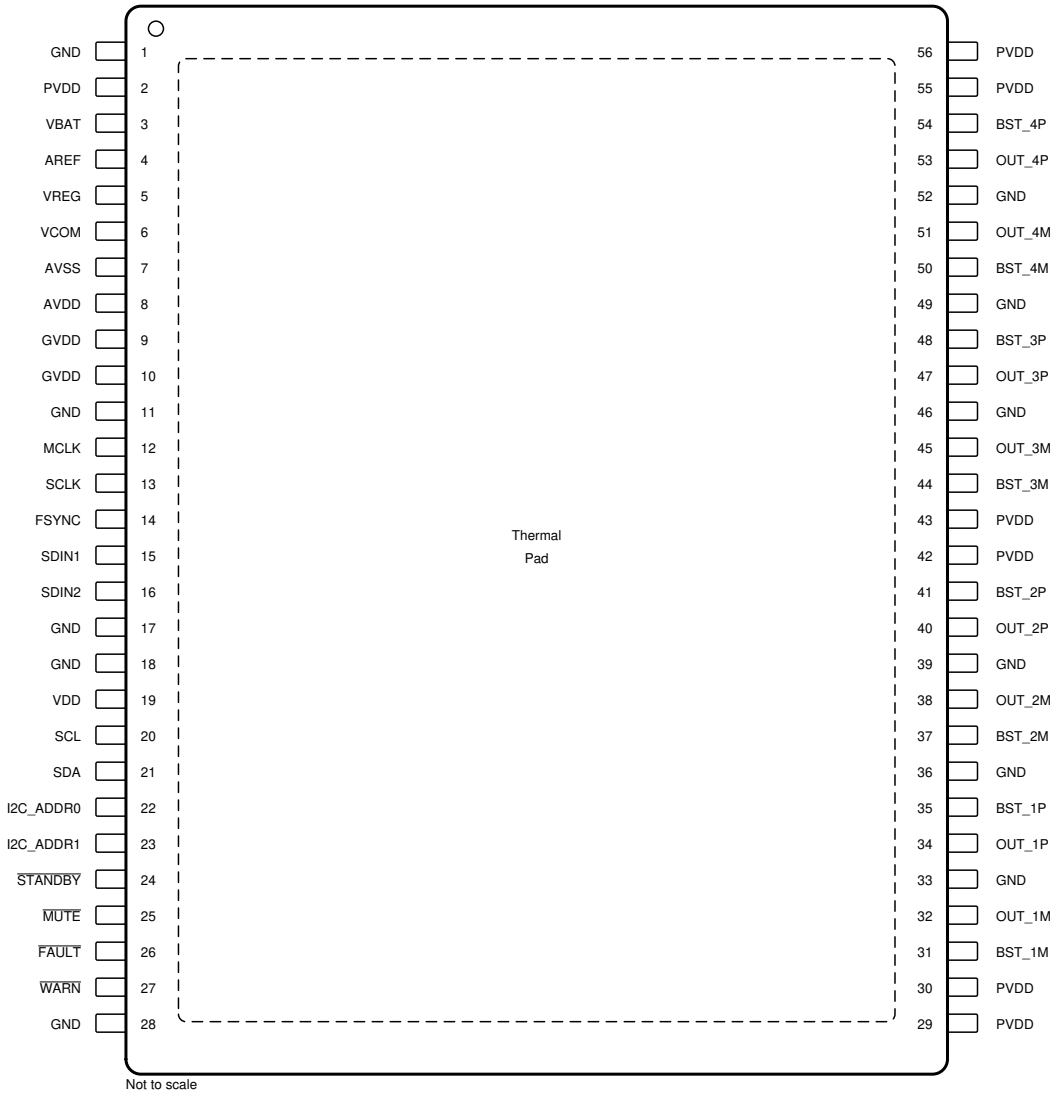

Figure 4-1. TAS6424E-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_C = 25 °C
- PVDD = 4.5 V - 26.4 V
- VBAT = 14.4 V
- VDD = 3.3 V
- R_L = 4 Ω
- P_{OUT} = 1 W, f = 1 kHz
- f_{SW} = 2.11 MHz
- AES17 Filter, Default I^2C settings
- Output channels in "PLAY" mode

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	No effects	D
PVDD	2	No damage to device considering power and ground are at same potential.	B
VBAT	3	No damage to device considering power and ground are at same potential.	B
AREF	4	Functionality okay, while Performance may degrade	C

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VREG	5	Device will not play	B
VCOM	6	Gain is not correct. Under certain configurations, device may heat up	B
AVSS	7	No effects	D
AVDD	8	LDO trigger current limit protection, if continuous stress, may heat up	B
GVDD	9	LDO trigger current limit protection, if continuous stress, may heat up	B
GVDD	10	LDO trigger current limit protection, if continuous stress, may heat up	B
GND	11	No effects	D
MCLK	12	Clock error	B
SCLK	13	Clock error	B
FSYNC	14	Clock error	B
SDIN1	15	Input Audio is wrong. Under certain configurations, device may heat up	B
SDIN2	16	Input Audio is wrong. Under certain configurations, device may heat up	B
GND	17	No effects	D
GND	18	No effects	D
VDD	19	No damage to device considering power and ground are at same potential.	B
SCL	20	I2C interface not work	B
SDA	21	I2C interface not work	B
I2C_ADDR0	22	I2C Address might be affected. Device might lose I2C connection.	B
I2C_ADDR1	23	I2C Address might be affected. Device might lose I2C connection.	B
/STANDBY	24	Device is in standby mode	B
/MUTE	25	Device is in mute state	B
/FAULT	26	FAULT cannot assert correctly, might affect system MCU	B
/WARN	27	WARN cannot assert correctly, might affect system MCU	B
GND	28	No effects	D
PVDD	29	No damage to device considering power and ground are at same potential.	B
PVDD	30	No damage to device considering power and ground are at same potential.	B
BST_1M	31	Output cannot be driven to PVDD. LDO may heat up.	B
OUT_1M	32	Output over-current protection. Device shut-down. Fault will latch.	B
GND	33	No effects	D
OUT_1P	34	Output over-current protection. Device shut-down. Fault will latch.	B
BST_1P	35	Output cannot be driven to PVDD. LDO may heat up.	B
GND	36	No effects	D
BST_2M	37	Output cannot be driven to PVDD. LDO may heat up.	B
OUT_2M	38	Output over-current protection. Device shut-down. Fault will latch.	B
GND	39	No effects	D
OUT_2P	40	Output over-current protection. Device shut-down. Fault will latch.	B
BST_2P	41	Output cannot be driven to PVDD. LDO may heat up.	B
PVDD	42	No damage to device considering power and ground are at same potential.	B
PVDD	43	No damage to device considering power and ground are at same potential.	B
BST_3M	44	Output cannot be driven to PVDD. LDO may heat up.	B
OUT_3M	45	Output over-current protection. Device shut-down. Fault will latch.	B
GND	46	No effects	D
OUT_3P	47	Output over-current protection. Device shut-down. Fault will latch.	B
BST_3P	48	Output cannot be driven to PVDD. LDO may heat up.	B
GND	49	No effects	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BST_4M	50	Output cannot be driven to PVDD. LDO may heat up.	B
OUT_4M	51	Output over-current protection. Device shut-down. Fault will latch.	B
GND	52	No effects	D
OUT_4P	53	Output over-current protection. Device shut-down. Fault will latch.	B
BST_4P	54	Output cannot be driven to PVDD. LDO may heat up.	B
PVDD	55	No damage to device considering power and ground are at same potential.	B
PVDD	56	No damage to device considering power and ground are at same potential.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
PVDD	2	Device will not play	B
VBAT	3	Device will not play	B
AREF	4	Performance may degrade due to lack to external decouple cap	C
VREG	5	Performance may degrade due to lack to external decouple cap	C
VCOM	6	Performance may degrade due to lack to external decouple cap	C
AVSS	7	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
AVDD	8	Performance may degrade due to lack to external decouple cap	C
GVDD	9	Driver may not work correctly. May trigger Over-Current protection.	B
GVDD	10	Driver may not work correctly. May trigger Over-Current protection.	B
GND	11	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
MCLK	12	Report clock error	B
SCLK	13	Report clock error	B
FSYNC	14	Report clock error	B
SDIN1	15	No input audio signal	B
SDIN2	16	No input audio signal	B
GND	17	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
GND	18	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
VDD	19	Device will not startup	B
SCL	20	Device will not respond to I2C command	B
SDA	21	Device will not respond to I2C command	B
I2C_ADDR0	22	Device I2C address might be wrong	B
I2C_ADDR1	23	Device I2C address might be wrong	B
/STANDBY	24	Internal pull-down resistor will standby the device	B
/MUTE	25	Internal pull-down resistor will mute the device	B
/FAULT	26	FAULT cannot reported to system	B
/WARN	27	WARN cannot reported to system	B
GND	28	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
PVDD	29	Device will not play	B
PVDD	30	Device will not play	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BST_1M	31	Output cannot be driven to PVDD.	B
OUT_1M	32	Open-Load condition	C
GND	33	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
OUT_1P	34	Open-Load condition	C
BST_1P	35	Output cannot be driven to PVDD. LDO may heat up.	B
GND	36	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
BST_2M	37	Output cannot be driven to PVDD. LDO may heat up.	B
OUT_2M	38	Open-Load condition	C
GND	39	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
OUT_2P	40	Open-Load condition	C
BST_2P	41	Output cannot be driven to PVDD. LDO may heat up.	B
PVDD	42	Device will not play	B
PVDD	43	Device will not play	B
BST_3M	44	Output cannot be driven to PVDD. LDO may heat up.	B
OUT_3M	45	Open-Load condition	C
GND	46	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
OUT_3P	47	Open-Load condition	C
BST_3P	48	Output cannot be driven to PVDD. LDO may heat up.	B
GND	49	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
BST_4M	50	Output cannot be driven to PVDD. LDO may heat up.	B
OUT_4M	51	Open-Load condition	C
GND	52	If all GND are not connected, device may damage. If only one is not connected, device functional, performance may degrade.	A
OUT_4P	53	Open-Load condition	C
BST_4P	54	Output cannot be driven to PVDD. LDO may heat up.	B
PVDD	55	Device will not play	B
PVDD	56	Device will not play	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	2	No damage to device considering power and ground are at same potential.	B
PVDD	2	3	Report VBAT OV if PVDD is above 20V	B
VBAT	3	4	Device may damage (AREF cannot handle VBAT)	A
AREF	4	5	Device will not play	B
VREG	5	6	Amplifier gain not correct	B
VCOM	6	7	Amplifier gain not correct	B
AVSS	7	8	Device won't startup, AVDD LDO may heat up.	B
AVDD	8	9	Device won't startup, AVDD LDO may heat up.	B
GVDD	9	10	Audio performance degradation	C
GVDD	10	11	LDO trigger current limit protection, if continuous stress, may heat up	B
GND	11	12	Report clock error	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
MCLK	12	13	Report clock error	B
SCLK	13	14	Report clock error	B
FSYNC	14	15	Report clock error	B
SDIN1	15	16	Incorrect audio output	B
SDIN2	16	17	Incorrect audio output	B
GND	17	18	No effects	D
GND	18	19	System-level fault. Power short to Ground	B
VDD	19	20	Device won't respond to I2C command	B
SCL	20	21	Device won't respond to I2C command	B
SDA	21	22	Device won't respond to I2C command	B
I2C_ADDR0	22	23	I2C address may change	B
I2C_ADDR1	23	24	I2C address may change	B
/STANDBY	24	25	Device control signal might conflict	B
/MUTE	25	26	Device control signal might conflict	B
/FAULT	26	27	Device FAULT WARN assertion might conflict	B
/WARN	27	28	/WARN pin cannot be cleared	B
GND	28	29	No damage to device considering power and ground are at same potential.	B
PVDD	29	30	No effects	D
PVDD	30	31	BST-OUT ESD diode may damage when OUT is low.	A
BST_1M	31	32	Device cannot work properly	B
OUT_1M	32	33	Output S2G event	B
GND	33	34	DC diagnostic or OC	B
OUT_1P	34	35	Device cannot work properly	B
BST_1P	35	36	Device won't startup	B
GND	36	37	Device won't startup	B
BST_2M	37	38	Device cannot work properly	B
OUT_2M	38	39	Output S2G event	B
GND	39	40	Output S2G event	B
OUT_2P	40	41	Device cannot work properly	B
BST_2P	41	42	BST-OUT ESD diode may damage when OUT is low.	A
PVDD	42	43	No effects	D
PVDD	43	44	BST-OUT ESD diode may damage when OUT is low.	A
BST_3M	44	45	Device cannot work properly	B
OUT_3M	45	46	Output S2G event	B
GND	46	47	DC diagnostic or OC	B
OUT_3P	47	48	Device cannot work properly	B
BST_3P	48	49	Device won't startup	B
GND	49	50	Device won't startup	B
BST_4M	50	51	Device cannot work properly	B
OUT_4M	51	52	Output S2G event	B
GND	52	53	DC diagnostic or OC	B
OUT_4P	53	54	Device cannot work properly	B
BST_4P	54	55	BST-OUT ESD diode may damage when OUT is low.	A
PVDD	55	56	No effects	D
PVDD	56	55	No effects	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to PVDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	System-level fault. Power short to Ground	B
PVDD	2	No effects	D
VBAT	3	Report VBAT OV fault if PVDD>20V	B
AREF	4	System-level fault. Power short to Ground	B
VREG	5	Device may damage	A
VCOM	6	Device may damage	A
AVSS	7	System-level fault. Power short to Ground	B
AVDD	8	Device may damage	A
GVDD	9	Device may damage	A
GVDD	10	Device may damage	A
GND	11	System-level fault. Power short to Ground	B
MCLK	12	Device may damage	A
SCLK	13	Device may damage	A
FSYNC	14	Device may damage	A
SDIN1	15	Device may damage	A
SDIN2	16	Device may damage	A
GND	17	System-level fault. Power short to Ground	B
GND	18	System-level fault. Power short to Ground	B
VDD	19	Device may damage	A
SCL	20	Device may damage	A
SDA	21	Device may damage	A
I2C_ADDR0	22	Device may damage	A
I2C_ADDR1	23	Device may damage	A
/STANDBY	24	Device may damage	A
/MUTE	25	Device may damage	A
/FAULT	26	Device may damage	A
/WARN	27	Device may damage	A
GND	28	System-level fault. Power short to Ground	B
PVDD	29	No effects	D
PVDD	30	No effects	D
BST_1M	31	Device may damage	A
OUT_1M	32	Output S2P event, protected if short after filter.	B
GND	33	System-level fault. Power short to Ground	B
OUT_1P	34	Output S2P event, protected if short after filter.	B
BST_1P	35	Device may damage	A
GND	36	System-level fault. Power short to Ground	B
BST_2M	37	Device may damage	A
OUT_2M	38	Output S2P event, protected if short after filter.	B
GND	39	System-level fault. Power short to Ground	B
OUT_2P	40	Output S2P event, protected if short after filter.	B
BST_2P	41	Device may damage	A
PVDD	42	No effects	D
PVDD	43	No effects	D
BST_3M	44	Device may damage	A
OUT_3M	45	Output S2P event, protected if short after filter.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to PVDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	46	System-level fault. Power short to Ground	B
OUT_3P	47	Output S2P event, protected if short after filter.	B
BST_3P	48	Device may damage	A
GND	49	System-level fault. Power short to Ground	B
BST_4M	50	Device may damage	A
OUT_4M	51	Output S2P event, protected if short after filter.	B
GND	52	System-level fault. Power short to Ground	B
OUT_4P	53	Output S2P event, protected if short after filter.	B
BST_4P	54	Device may damage	A
PVDD	55	No effects	D
PVDD	56	No effects	D

Table 4-6. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	System-level fault. Power short to Ground	B
PVDD	2	Report VBAT OV fault	B
VBAT	3	No effects	D
AREF	4	System-level fault. Power short to Ground	B
VREG	5	Device may damage	A
VCOM	6	Device may damage	A
AVSS	7	System-level fault. Power short to Ground	B
AVDD	8	Device may damage	A
GVDD	9	Device may damage	A
GVDD	10	Device may damage	A
GND	11	System-level fault. Power short to Ground	B
MCLK	12	Device may damage	A
SCLK	13	Device may damage	A
FSYNC	14	Device may damage	A
SDIN1	15	Device may damage	A
SDIN2	16	Device may damage	A
GND	17	System-level fault. Power short to Ground	B
GND	18	System-level fault. Power short to Ground	B
VDD	19	Device may damage	A
SCL	20	Device may damage	A
SDA	21	Device may damage	A
I2C_ADDR0	22	Device may damage	A
I2C_ADDR1	23	Device may damage	A
/STANDBY	24	Device may damage	A
/MUTE	25	Device may damage	A
/FAULT	26	Device may damage	A
/WARN	27	Device may damage	A
GND	28	System-level fault. Power short to Ground	B
PVDD	29	Report VBAT OV fault	B
PVDD	30	Report VBAT OV fault	B
BST_1M	31	Device may damage	A

Table 4-6. Pin FMA for Device Pins Short-Circuited to VBAT (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT_1M	32	Output S2P event, protected if short after filter.	B
GND	33	System-level fault. Power short to Ground	B
OUT_1P	34	Output S2P event, protected if short after filter.	B
BST_1P	35	Device may damage	A
GND	36	System-level fault. Power short to Ground	B
BST_2M	37	Device may damage	A
OUT_2M	38	Output S2P event, protected if short after filter.	B
GND	39	System-level fault. Power short to Ground	B
OUT_2P	40	Output S2P event, protected if short after filter.	B
BST_2P	41	Device may damage	A
PVDD	42	Report VBAT OV fault	B
PVDD	43	Report VBAT OV fault	B
BST_3M	44	Device may damage	A
OUT_3M	45	Output S2P event, protected if short after filter.	B
GND	46	System-level fault. Power short to Ground	B
OUT_3P	47	Output S2P event, protected if short after filter.	B
BST_3P	48	Device may damage	A
GND	49	System-level fault. Power short to Ground	B
BST_4M	50	Device may damage	A
OUT_4M	51	Output S2P event, protected if short after filter.	B
GND	52	System-level fault. Power short to Ground	B
OUT_4P	53	Output S2P event, protected if short after filter.	B
BST_4P	54	Device may damage	A
PVDD	55	Report VBAT OV fault	B
PVDD	56	Report VBAT OV fault	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	System-level fault. Power short to Ground	B
PVDD	2	Report UV fault	B
VBAT	3	Report UV fault	B
AREF	4	System-level fault. Power short to Ground	B
VREG	5	VREG is too low.	B
VCOM	6	VCOM is local CM modulator. Gain not correct.	B
AVSS	7	System-level fault. Power short to Ground	B
AVDD	8	Trigger AVDD LDO current limit	B
GVDD	9	Trigger GVDD LDO current limit	B
GVDD	10	Trigger GVDD LDO current limit	B
GND	11	System-level fault. Power short to Ground	B
MCLK	12	Device I2S not responsive	B
SCLK	13	Device I2S not responsive	B
FSYNC	14	Device I2S not responsive	B
SDIN1	15	May heat up for incorrect input audio	B
SDIN2	16	May heat up for incorrect input audio	B
GND	17	System-level fault. Power short to Ground	B

Table 4-7. Pin FMA for Device Pins Short-Circuited to VDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	18	System-level fault. Power short to Ground	B
VDD	19	No effects.	D
SCL	20	Device I2C not responsive	B
SDA	21	Device I2C not responsive	B
I2C_ADDR0	22	This will change device I2C address	B
I2C_ADDR1	23	This will change device I2C address	B
/STANDBY	24	Device may automatically unmute once released from standby	B
/MUTE	25	If UNMUTE under wrong condition, damage possible	B
/FAULT	26	Error not handling correctly	B
/WARN	27	Warning not handling correctly	B
GND	28	System-level fault. Power short to Ground	B
PVDD	29	Report UV fault	B
PVDD	30	Report UV fault	B
BST_1M	31	Device may damage	A
OUT_1M	32	Device may damage	A
GND	33	System-level fault. Power short to Ground	B
OUT_1P	34	Device may damage	A
BST_1P	35	Device may damage	A
GND	36	System-level fault. Power short to Ground	B
BST_2M	37	Device may damage	A
OUT_2M	38	Device may damage	A
GND	39	System-level fault. Power short to Ground	B
OUT_2P	40	Device may damage	A
BST_2P	41	Device may damage	A
PVDD	42	Report UV fault	B
PVDD	43	Report UV fault	B
BST_3M	44	Device may damage	A
OUT_3M	45	Device may damage	A
GND	46	System-level fault. Power short to Ground	B
OUT_3P	47	Device may damage	A
BST_3P	48	Device may damage	A
GND	49	System-level fault. Power short to Ground	B
BST_4M	50	Device may damage	A
OUT_4M	51	Device may damage	A
GND	52	System-level fault. Power short to Ground	B
OUT_4P	53	Device may damage	A
BST_4P	54	Device may damage	A
PVDD	55	Report UV fault	B
PVDD	56	Report UV fault	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2022	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265