TAS6684 SDOUT Format Question

Sending current sense & temp data to SDOUT in a 20-bit slot

Problem

- Need to combine 3 TAS6684's Isense & temp data streams onto 1 TDM8 @ 32-bit lane
- 12 channels, 256 bits per frame means each channel can occupy a maximum of 21 bits

Proposal

• Set bits [3:0] of ASI_CTRL17 to 0b0010 to enable only Isense data output

3-0	reg_tx_sel	R/W	Enable or disable the output data channel 0000: Disable all the output data channels xxx1: Enable Vpredict Ch1/2/3/4 output xx1x: Enable Isense Ch1/2/3/4 output x1xx: Enable Aux Ch1/2/3/4 output In non-TDM mode, if user needs to output 4 channels, 4'b0011
			should be set

Set bits [1:0] of ASI_CTRL5 to 0b01 to set Isense data width to 20 bits

1-0	I2S_WL_6	R/W	0x2	I2S Word Length
				These bits control output audio interface sample word lengths for
				channel 3/4 output in non-TDM mode and isense output channels in
				TDM mode.
				00: 16 bits
				01: 20 bits
				10: 24 bits
				11: 32 bits
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Proposal (contd.)

- Set bits [7:0] of ASI_CTRL14 to offset the Isense data from each of the 3 devices in the TDM frame:
 - Device 1: Offset = 0
 - Device 2: Offset = 80
 - Device 3: Offset = 160

Table 8-20. ASI_CTRL14 Register Field Descriptions

Table of Ed. Adi_Office File Beschiptions					
Bit	Field	Туре	Reset	Description	
7-0	reg_i2s_shift6_lsb	R/W	0x0	I2S/TDM Shift6 LSB These bits control the offset of audio data in the audio frame for output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio. reg_i2s_shift6 = {reg_i2s_shift6_msb, reg_i2s_shift6_lsb} reg_i2s_shift6 controls the offset in isense ch1/2/3/4 path. 0000000000: offset = 0 BCK (no offset) 000000001: offset = 1 BCK 0000000010: offset = 2 BCKs 1111111111: offset = 1023 BCKs	

Adding Temp Data - Question

- Data sheet discusses possibility to use 3 bits of the Isense data slot for a temp reading:
 - **sd_lts_pvdd** enables the monitoring data of PVDD and local temperature sensing transitted on TDM slots. When bit 5 of ASI_CTRL1 Register (Address = 0x21) [Reset = 0x00] is set to '0', the data slots of Isense and Vpredict consist of 32 bits data of current sense and predict voltage. Otherwise, the 32 bits slot of isense data packet consists of 29 bits of isense data and 3 bits of local temperature sensor data. In this case, the 32 bits slot of Vpredict data packet consists of 24 bits of predict voltage and 8 bits PVDD monitoring data.

Table 7-3. TDM Data Format of Isense and Vpredict

sd_lts_pvdd(ASI_CTRL1 Register (Address = 0x21) [Reset = 0x00], b[5])	Data Format of Isense	Data Format of Vpred
0	32 bits data of current sense	32 bits data of predict voltage
1	29 bits data of current sense + 3 bits data of Channel temperature	24 bits data of predict voltage + 8 bits monitoring data of PVDD

- However, this section is always referring to "32-bit" Isense data. Does this generalize to "the Isense data width selected in bits [1:0] of ASI_CTRL5"?
- If so, and we enable bit 5 of ASI_CTRL1, will the device send 3 bits of temp data in our 20-bit Isense slot? I.e. we get a 17-bit Isense value and 3 bit temp value?
- If so, are the temp data bits placed at the high or low end of the slot?