Table 7-45. Summary of Register Map

PAGE NUMBER	DESCRIPTION
0	Page 0 is the default page on power up. Configuration for serial interface, digital I/O, clocking, ADC, DAC settings, and other circuitry.
1	Configuration for analog PGAs, ADC, DAC, output drivers, volume controls, and other circuitry.
3	Register 16 controls the MCLK divider that controls the interrupt pulse duration, debounce timing, and detection block clock.
4–5	ADC AGC and filter coefficients
8–9	DAC Buffer A filter and DRC coefficients
12–13	DAC Buffer B filter and DRC coefficients

7.4.2 Registers

7.4.2.1 Control Registers, Page 0 (Default Page): Clock Multipliers, Dividers, Serial Interfaces, Flags, Interrupts, and GPIOs

Table 7-46. Page 0 / Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

Table 7-47. Page 0 / Register 1: Software Reset

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	0000 000	Reserved. Write only zeros to these bits.
D0	R/W	0	0: Don't care 1: Self-clearing software reset for control register

Table 7-48. Page 0 / Register 2: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	Reserved. Do not write to this register.

Table 7-49. Page 0 / Register 3: OT FLAG

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	XXXX XX	Reserved. Do not write to these bits.
D1	R	1	0: Overtemperature protection flag (active-low). Valid only if speaker amplifier is powered up 1: Normal operation
D0	R/W	X	Reserved. Do not write to these bits.

Table 7-50. Page 0 / Register 4: Clock-Gen Muxing(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only zeros to these bits.
D3–D2	R/W	00	00: PLL_CLKIN = **MCLK** (device pin) 01: PLL_CLKIN = BCLK (device pin) 10: PLL_CLKIN = GPIO1 (device pin) 11: PLL_CLKIN = DIN (can be used for the system where DAC is not used)
D1–D0	R/W	00	00: CODEC_CLKIN = **MCLK** (device pin) 01: CODEC_CLKIN = BCLK (device pin) 10: CODEC_CLKIN = GPIO1 (device pin) 11: CODEC_CLKIN = PLL_CLK (generated on-chip)

(1) See Section 7.3.11 for more details on clock generation mutiplexing and dividers.

Table 7-51. Page 0 / Register 5: PLL P and R Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: PLL is powered down. 1: PLL is powered up.
D6–D4	R/W	001	000: PLL divider P = 8 001: PLL divider P = 1 010: PLL divider P = 2 ... 110: PLL divider P = 6 111: PLL divider P = 7
D3–D0	R/W	0001	0000: PLL multiplier R = 16 0001: PLL multiplier R = 1 0010: PLL multiplier R = 2 ... 1110: PLL multiplier R = 14 1111: PLL multiplier R = 15

Table 7-52. Page 0 / Register 6: PLL J-Value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only zeros to these bits.
D5–D0	R/W	00 0100	00 0000: Do not use (reserved) 00 0001: PLL multiplier J = 1 00 0010: PLL multiplier J = 2 ... 11 1110: PLL multiplier J = 62 11 1111: PLL multiplier J = 63

Table 7-53. Page 0 / Register 7: PLL D-Value MSB(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only zeros to these bits.
D5–D0	R/W	00 0000	PLL fractional multiplier D-value MSB bits D[13:8]

(1) Note that this register is updated only when Page 0 / Register 8 is written immediately after Page 0 / Register 7.

Table 7-54. Page 0 / Register 8: PLL D-Value LSB(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	PLL fractional multiplier D-value LSB bits D[7:0]

(1) Note that Page 0 / Register 8 must be written immediately after Page 0 / Register 7.

Table 7-55. Page 0 / Register 9 and Page 0 / Register 10: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only zeros to these bits.

Table 7-56. Page 0 / Register 11: DAC NDAC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DAC NDAC divider is powered down. 1: DAC NDAC divider is powered up.
D6–D0	R/W	000 0001	000 0000: DAC NDAC divider = 128 000 0001: DAC NDAC divider = 1 000 0010: DAC NDAC divider = 2 ... 111 1110: DAC NDAC divider = 126 111 1111: DAC NDAC divider = 127

Table 7-57. Page 0 / Register 12: DAC MDAC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DAC MDAC divider is powered down. 1: DAC MDAC divider is powered up.
D6–D0	R/W	000 0001	000 0000: DAC MDAC divider = 128 000 0001: DAC MDAC divider = 1 000 0010: DAC MDAC divider = 2 ... 111 1110: DAC MDAC divider = 126 111 1111: DAC MDAC divider = 127

Table 7-58. Page 0 / Register 13: DAC DOSR_VAL MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 00	Reserved
D1–D0	R/W	00	DAC OSR value DOSR(9:8)

Table 7-59. Page 0 / Register 14: DAC DOSR_VAL LSB(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	DAC OSR Value DOSR (7:0) 0000 0000: DAC OSR (7:0) = 1024 (MSB page 0 / register 13, bits D1–D0 = 00) 0000 0001: DAC OSR (7:0) = 1 (MSB page 0 / register 13, bits D1–D0 = 00) 0000 0010: DAC OSR (7:0) = 2 (MSB page 0 / register 13, bits D1–D0 = 00) ... 1111 1110: DAC OSR (7:0) = 1022 (MSB page 0 / register 13, bits D1–D0 = 11) 1111 1111: DAC OSR (7:0) = 1023 (MSB page 0 / register 13, bits D1–D0 = 11)

(1) DAC OSR must be an integral multiple of the interpolation in the DAC miniDSP engine (specified in register 16). When using PRB modes, interpolation ratio is 8 while using Filter-A, 4 while using Filter-B and 2 while using Filter-C.

Table 7-60. Page 0 / Register 15: DAC IDAC_VAL(1)(2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	0000 0000: Number of instruction for DAC PRB engine, IDAC = 1024 0000 0001: Number of instruction for DAC PRB engine, IDAC = 4 0000 0010: Number of instruction for DAC PRB engine, IDAC = 8 ... 1111 1101: Number of instruction for DAC PRB engine, IDAC = 1012 1111 1110: Number of instruction for DAC PRB engine, IDAC = 1016 1111 1111: Number of instruction for DAC PRB engine, IDAC = 1020

(1) IDAC must be an integral multiple of the interpolation in the DAC PRB engine (specified in register 16). When using PRB modes, interpolation ratio is 8 while using Filter-A, 4 while using Filter-B and 2 while using Filter-C.
(2) The Page 0 / Register 15 programmed value is valid when Page 0 / Register 60, D(4:0) is programmed as *0 0000*.

Table 7-61. Page 0 / Register 16: DAC PRB Engine Interpolation

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Do not write to these registers.
D3–D0(1)	R/W	1000	0000: Interpolation ratio in DAC PRB engine = 16 0001: Interpolation ratio in DAC PRB engine = 1 0010: Interpolation ratio in DAC PRB engine = 2 ... 1101: Interpolation ratio in DAC PRB engine = 13 1110: Interpolation ratio in DAC PRB engine = 14 1111: Interpolation ratio in DAC PRB engine = 15

(1) The Page 0 / Register 16, D(3:0) programmed value is valid when Page 0 / Register 60, D(4:0) is programmed as *0 0000*.

Table 7-62. Page 0 / Register 17: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-63. Page 0 / Register 18: ADC NADC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: ADC NADC divider is powered down and ADC_MOD_CLK = DAC_MOD_CLK 1: ADC NADC divider is powered up.
D6–D0	R/W	000 0001	000 0000: ADC NADC divider = 128 000 0001: ADC NADC divider = 1 000 0010: ADC NADC divider = 2 ... 111 1110: ADC NADC divider = 126 111 1111: ADC NADC divider = 127

Table 7-64. Page 0 / Register 19: ADC MADC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: ADC MADC divider is powered down and ADC_MOD_CLK = DAC_MOD_CLK. 1: ADC MADC divider is powered up.
D6–D0	R/W	000 0001	000 0000: ADC MADC divider = 128 000 0001: ADC MADC divider = 1 000 0010: ADC MADC divider = 2 ... 111 1110: ADC MADC divider = 126 111 1111: ADC MADC divider = 127

Table 7-65. Page 0 / Register 20: ADC AOSR_VAL(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	ADC Oversampling Value 0000 0000: ADC AOSR = 256 0000 0001-0001 1111: Reserved. Do not use 0010 0000: ADC AOSR = 32 (Use with PRB_R13 to PRB_R18, ADC Filter Type C) 0010 0001-0011 1111: Reserved. Do not use 0100 0000: AOSR = 64 (Use with PRB_R1 to PRB_R12, ADC Filter Type A or B) 0100 0001-0111 1111: Reserved. Do not use 1000 0000: AOSR = 128(Use with PRB_R1 to PRB_R6, ADC Filter Type A) 1000 0001-1111 1111: Reserved. Do not use

(1) ADC OSR must be an integral multiple of the decimation in the ADC PRB engine (specified in register 22). When PRB modes are used, decimation ratio is 4 while using Filter-A, 2 while using Filter-B and 1 while using Filter-C

Table 7-66. Page 0 / Register 21: ADC IADC_VAL(1)(2)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	Reserved. Write only default values.

(1) IADC must be an integral multiple of the decimation in the ADC PRB engine (specified in Register 22). When PRB modes are used, decimation ratio is 4 while using Filter-A, 2 while using Filter-B and 1 while using Filter-C
(2) Page 0 / Register 21 programmed value is valid when Page 0/ Register 61, D(4:0) is programmed as *0 0000*.

Table 7-67. Page 0 / Register 22: ADC PRB Engine Decimation

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	Reserved. Write only default values.

Table 7-68. Page 0 / Register 23 and Page 0 / Register 24: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-69. Page 0 / Register 25: CLKOUT MUX

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Reserved
D2–D0	R/W	000	000: CDIV_CLKIN = MCLK (device pin) 001: CDIV_CLKIN = BCLK (device pin) 010: CDIV_CLKIN = DIN (can be used for the systems where DAC is not required) 011: CDIV_CLKIN = PLL_CLK (generated on-chip) 100: CDIV_CLKIN = DAC_CLK (DAC DSP clock - generated on-chip) 101: CDIV_CLKIN = DAC_MOD_CLK (generated on-chip) 110: CDIV_CLKIN = ADC_CLK (ADC DSP clock - generated on-chip) 111: CDIV_CLKIN = ADC_MOD_CLK (generated on-chip)

Table 7-70. Page 0 / Register 26: CLKOUT M_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: CLKOUT M divider is powered down. 1: CLKOUT M divider is powered up.
D6–D0	R/W	000 0001	000 0000: CLKOUT divider M = 128 000 0001: CLKOUT divider M = 1 000 0010: CLKOUT divider M = 2 ... 111 1110: CLKOUT divider M = 126 111 1111: CLKOUT divider M = 127

Table 7-71. Page 0 / Register 27: Codec Interface Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: Codec interface = I^2S 01: Codec Interface = DSP 10: Codec interface = RJF 11: Codec interface = LJF
D5–D4	R/W	00	00: Codec interface word length = 16 bits 01: Codec interface word length = 20 bits 10: Codec interface word length = 24 bits 11: Codec interface word length = 32 bits
D3	R/W	0	0: BCLK is input 1: BCLK is output
D2	R/W	0	0: WCLK is input 1: WCLK is output
D1	R/W	0	Reserved
D0	R/W	0	Driving **DOUT** to High-Impedance for the Extra BCLK Cycle When Data Is Not Being Transferred 0: Disabled 1: Enabled

Table 7-72. Page 0 / Register 28: Data-Slot Offset Programmability

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Offset (Measured With Respect to WCLK Rising Edge in DSP Mode) 0000 0000: Offset = 0 BCLKs 0000 0001: Offset = 1 BCLK 0000 0010: Offset = 2 BCLKs ... 1111 1110: Offset = 254 BCLKs 1111 1111: Offset = 255 BCLKs

Table 7-73. Page 0 / Register 29: Codec Interface Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved
D5	R/W	0	0: DIN-to-DOUT loopback is disabled 1: DIN-to-DOUT loopback is enabled
D4	R/W	0	0: ADC-to-DAC loopback is disabled 1: ADC-to-DAC loopback is enabled
D3	R/W	0	0: BCLK is not inverted (valid for both primary and secondary BCLK) 1: BCLK is inverted (valid for both primary and secondary BCLK)
D2	R/W	0	BCLK and WCLK Active Even With Codec Powered Down (Valid for Both Primary and Secondary BCLK) 0: Disabled 1: Enabled
D1–D0	R/W	00	00: BDIV_CLKIN = DAC_CLK (DAC DSP clock - generated on-chip) 01: BDIV_CLKIN = DAC_MOD_CLK (generated on-chip) 10: BDIV_CLKIN = ADC_CLK (ADC DSP clock - generated on-chip) 11: BDIV_CLKIN = ADC_MOD_CLK (generated on-chip)

Table 7-74. Page 0 / Register 30: BCLK N_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: BCLK N-divider is powered down. 1: BCLK N-divider is powered up.
D6–D0	R/W	000 0001	000 0000: BCLK divider N = 128 000 0001: BCLK divider N = 1 000 0010: BCLK divider N = 2 ... 111 1110: BCLK divider N = 126 111 1111: BCLK divider N = 127

Table 7-75. Page 0 / Register 31: Codec Secondary Interface Control 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	000: Secondary BCLK is obtained from GPIO1 pin. 001: Reserved. 010: Reserved. 011: Secondary BCLK is obtained from DOUT pin. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
D4–D2	R/W	000	000: Secondary WCLK is obtained from GPIO1 pin. 001: Reserved. 010: Reserved. 011: Secondary WCLK is obtained from DOUT pin. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
D1–D0	R/W	00	00: Secondary DIN is obtained from the GPIO1 pin. 01: Reserved. 10: Reserved. 11: Reserved.

Table 7-76. Page 0 / Register 32: Codec Secondary Interface Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	000: ADC_WCLK is obtained from GPIO1 pin. 001: Reserved. 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
D4	R/W	0	Reserved
D3	R/W	0	0: Primary BCLK is fed to codec serial-interface and ClockGen blocks. 1: Secondary BCLK is fed to codec serial-interface and ClockGen blocks.
D2	R/W	0	0: Primary WCLK is fed to codec serial-interface block. 1: Secondary WCLK is fed to codec serial-interface block.
D1	R/W	0	0: ADC_WCLK used in the codec serial-interface block is the same as DAC_WCLK. 1: ADC_WCLK used in the codec serial-interface block = ADC_WCLK.
D0	R/W	0	0: Primary DIN is fed to codec serial-interface block. 1: Secondary DIN is fed to codec serial-interface block.

Table 7-77. Page 0 / Register 33: Codec Secondary Interface Control 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Primary BCLK output = internally generated BCLK clock 1: Primary BCLK output = secondary BCLK
D6	R/W	0	0: Secondary BCLK output = primary BCLK 1: Secondary BCLK output = internally generated BCLK clock
D5–D4	R/W	00	00: Primary WCLK output = internally generated DAC_f_S 01: Primary WCLK output = internally generated ADC_f_S clock 10: Primary WCLK output = secondary WCLK 11: Reserved
D3–D2	R/W	00	00: Secondary WCLK output = primary WCLK 01: Secondary WCLK output = internally generated DAC_f_S clock 10: Secondary WCLK output = internally generated ADC_f_S clock 11: Reserved
D1	R/W	0	0: Primary DOUT = DOUT from codec serial-interface block 1: Primary DOUT = secondary DIN

Table 7-77. Page 0 / Register 33: Codec Secondary Interface Control 3 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	0: Secondary DOUT = primary DIN 1: Secondary DOUT = DOUT from codec serial interface block

Table 7-78. Page 0 / Register 34: I^2C Bus Condition

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only the reset value to these bits.
D5	R/W	0	0: I^2C general-call address is ignored. 1: Device accepts I^2C general-call address.
D4–D0	R/W	0 0000	Reserved. Write only zeros to these bits.

Table 7-79. Page 0 / Register 35: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only zeros to these bits.

Table 7-80. Page 0 / Register 36: ADC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: ADC PGA applied gain ≠ programmed gain 1: ADC PGA applied gain = programmed gain
D6	R	0	0: ADC powered down 1: ADC powered up
D5(1)	R	0	0: AGC not saturated 1: AGC applied gain = maximum applicable gain by AGC
D4–D0	R/W	X XXXX	Reserved. Write only zeros to these bits.

(1) Sticky flag bIt. These is a read-only bit. This bit is automatically cleared once it is read and is set only if the source trigger occurs again.

Table 7-81. Page 0 / Register 37: DAC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: Left-channel DAC powered down 1: Left-channel DAC powered up
D6	R	X	Reserved. Write only zero to this bit.
D5	R	0	0: HPL driver powered down 1: HPL driver powered up
D4	R	0	0: Mono class-D driver powered down 1: Mono class-D driver powered up
D3	R	0	0: Right-channel DAC powered down 1: Right-channel DAC powered up
D2	R/W	X	Reserved. Write only zero to this bit.
D1	R	0	0: HPR driver powered down 1: HPR driver powered up
D0	R	0	0: Reserved 1: Reserved

Table 7-82. Page 0 / Register 38: DAC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	XXX	Reserved. Do not write to these bits.
D4	R	0	0: Left-channel DAC PGA applied gain ≠ programmed gain 1: Left-channel DAC PGA applied gain = programmed gain

Table 7-82. Page 0 / Register 38: DAC Flag Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D1	R/W	XXX	Reserved. Write only zeros to these bits.
D0	**R**	0	0: Right-channel DAC PGA applied gain ≠ programmed gain 1: Right-channel DAC PGA applied gain = programmed gain

Table 7-83. Page 0 / Register 39: Overflow Flags

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left-Channel DAC Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D6	R	0	Right-Channel DAC Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D5	R	0	DAC Barrel Shifter Output Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D4	R/W	0	Reserved. Write only zeros to these bits.
D3	R	0	Delta-Sigma Mono ADC Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D2	R/W	0	Reserved. Write only zero to this bit.
D1	R	0	ADC Barrel Shifter Output Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D0	R/W	0	Reserved. Write only zero to this bit.

Table 7-84. Page 0 / Register 40 Through Page 0 / Register 43: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only the reset value to these bits.

Table 7-85. Page 0 / Register 44: Interrupt Flags—DAC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No short circuit is detected at HPL / mono class-D driver. 1: Short circuit is detected at HPL / mono class-D driver.
D6	R	0	0: Reserved 1: Reserved
D5	**R**	X	0: No headset button pressed. 1: Headset button pressed.
D4	**R**	X	0: No headset insertion or removal is detected. 1: Headset insertion or removal is detected.
D3	**R**	0	0: Left DAC signal power is less than or equal to the signal threshold of DRC. 1: Left DAC signal power is above the signal threshold of DRC.
D2	**R**	0	0: Right DAC signal power is less than or equal to the signal threshold of DRC. 1: Right DAC signal power is above the signal threshold of DRC.
D1-D0	**R**	0	Reserved.

Table 7-86. Page 0 / Register 45: Interrupt Flags—ADC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.

Table 7-86. Page 0 / Register 45: Interrupt Flags—ADC (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6	R	0	0: ADC signal power greater than noise threshold for AGC. 1: ADC signal power less than noise threshold for AGC.
D5	R/W	0	Reserved. Write only zeros to these bits.
D4	R	X	ADC PRB Engine Standard Interrupt Port Output. 0: Read a 0 from standard interrupt-port. 1: Read a 1 from standard interrupt-port.
D3	R	X	ADC PRB Engine Auxiliary Interrupt Port Output. 0: Read a 0 from auxiliary interrupt-port. 1: Read a 1 from auxiliary interrupt-port.
D2	R	0	0: DC measurement using delta-sigma audio ADC is not available. 1: DC measurement using delta-sigma audio ADC is not available.
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

Table 7-87. Page 0 / Register 46: Interrupt Flags—DAC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No short circuit detected at HPL / mono class-D driver. 1: Short circuit detected at HPL / mono class-D driver.
D6	R	0	0: Reserved 1: Reserved
D5	R	X	0: No headset button pressed. 1: Headset button pressed.
D4	R	X	0: Headset removal detected. 1: Headset insertion detected.
D3	R	0	0: Left DAC signal power is below signal threshold of DRC. 1: Left DAC signal power is above signal threshold of DRC.
D2	R	0	0: Right DAC signal power is below signal threshold of DRC. 1: Right DAC signal power is above signal threshold of DRC.
D1	R	0	DAC PRB Engine Standard Interrupt Port Output. 0: Read a 0 from standard interrupt-port. 1: Read a 1 from standard interrupt-port.
D0	R	0	DAC PRB Engine Auxiliary Interrupt Port Output. 0: Read a 0 from auxiliary interrupt-port. 1: Read a 1 from auxiliary interrupt-port.

Table 7-88. Page 0 / Register 47: Interrupt Flags—ADC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved
D6	R	0	0: Delta-sigma mono ADC signal power greater than noise threshold for left AGC 1: Delta-sigma mono ADC signal power less than noise threshold for left AGC
D5	R/W	0	Reserved
D4	R	X	ADC PRB Engine Standard Interrupt Port Output 0: Read a 0 from standard interrupt-port 1: Read a 1 from standard interrupt-port
D3	R	X	ADC PRB Engine Auxiliary Interrupt Port Output 0: Read a 0 from auxiliary interrupt-port 1: Read a 1 from auxiliary interrupt-port
D2	R	0	0: DC measurement using delta-sigma audio ADC is not available 1: DC measurement using delta-sigma audio ADC is not available
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

Table 7-89. Page 0 / Register 48: INT1 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset-insertion detect interrupt is not used in the generation of INT1 interrupt. 1: Headset-insertion detect interrupt is used in the generation of INT1 interrupt.
D6	R/W	0	0: Button-press detect interrupt is not used in the generation of INT1 interrupt. 1: Button-press detect interrupt is used in the generation of INT1 interrupt.
D5	R/W	0	0: DAC DRC signal-power interrupt is not used in the generation of INT1 interrupt. 1: DAC DRC signal-power interrupt is used in the generation of INT1 interrupt.
D4	R/W	0	0: ADC AGC noise interrupt is not used in the generation of INT1 interrupt. 1: ADC AGC noise interrupt is used in the generation of INT1 interrupt.
D3	R/W	0	0: Short-circuit interrupt is not used in the generation of INT1 interrupt. 1: Short-circuit interrupt is used in the generation of INT1 interrupt.
D2	R/W	0	0: Engine-generated interrupt is not used in the generation of INT1 interrupt. 1: Engine-generated interrupt is used in the generation of INT1 interrupt.
D1	R/W	0	0: DC measurement using delta-sigma audio ADC data-available interrupt is not used in the generation of INT1 interrupt 1: DC measurement using delta-sigma audio ADC data-available interrupt is used in the generation of INT1 interrupt
D0	R/W	0	0: INT1 is only one pulse (active-high) of typical 2-ms duration. 1: INT1 is multiple pulses (active-high) of typical 2-ms duration and 4-ms period, until flag registers 44 and 45 are read by the user.

Table 7-90. Page 0 / Register 49: INT2 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset-insertion detect interrupt is not used in the generation of INT2 interrupt. 1: Headset-insertion detect interrupt is used in the generation of INT2 interrupt.
D6	R/W	0	0: Button-press detect interrupt is not used in the generation of INT2 interrupt. 1: Button-press detect interrupt is used in the generation of INT2 interrupt.
D5	R/W	0	0: DAC DRC signal-power interrupt is not used in the generation of INT2 interrupt. 1: DAC DRC signal-power interrupt is used in the generation of INT2 interrupt.
D4	R/W	0	0: ADC AGC noise interrupt is not used in the generation of INT2 interrupt. 1: ADC AGC noise interrupt is used in the generation of INT2 interrupt.
D3	R/W	0	0: Short-circuit interrupt is not used in the generation of INT2 interrupt. 1: Short-circuit interrupt is used in the generation of INT2 interrupt.
D2	R/W	0	0: Engine-generated interrupt is not used in the generation of INT2 interrupt. 1: Engine-generated interrupt is used in the generation of INT2 interrupt.
D1	R/W	0	0: DC measurement using delta-sigma audio ADC data-available interrupt is not used in the generation of INT2 interrupt 1: DC measurement using delta-sigma audio ADC data-available interrupt is used in the generation of INT2 interrupt
D0	R/W	0	0: INT2 is only one pulse (active-high) of typical 2-ms duration. 1: INT2 is multiple pulses (active-high) of typical 2-ms duration and 4-ms period, until flag registers 44 and 45 are read by the user.

Table 7-91. Page 0 / Register 50: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Write only reset values.

Table 7-92. Page 0 / Register 51: GPIO1 In/Out Pin Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	XX	Reserved. Do not write any value other than reset value.
D5–D2	R/W	0000	0000: GPIO1 disabled (input and output buffers powered down) 0001: GPIO1 is in input mode (can be used as secondary BCLK input, secondary WCLK input, secondary DIN input, ADC_WCLK input, Dig_Mic_In or in ClockGen block). 0010: GPIO1 is used as general-purpose input (GPI). 0011: GPIO1 output = general-purpose output 0100: GPIO1 output = CLKOUT output 0101: GPIO1 output = INT1 output 0110: GPIO1 output = INT2 output 0111: GPIO1 output = ADC_WCLK output for codec interface 1000: GPIO1 output = secondary BCLK output for codec interface 1001: GPIO1 output = secondary WCLK output for codec interface 1010: GPIO1 output = ADC_MOD_CLK output for the digital microphone 1011: GPIO1 output = secondary DOUT for codec interface 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
D1	R	X	GPIO1 input buffer value
D0	R/W	0	0: GPIO1 general-purpose output value = 0 1: GPIO1 general-purpose output value = 1

Table 7-93. Page 0 / Register 52: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write any value other than reset value.

Table 7-94. Page 0 / Register 53: DOUT (OUT Pin) Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved
D4	R/W	1	0: DOUT bus keeper enabled 1: DOUT bus keeper disabled
D3–D1	R/W	001	000: DOUT disabled (output buffer powered down) 001: DOUT = primary DOUT output for codec interface 010: DOUT = general-purpose output 011: DOUT = CLKOUT output 100: DOUT = INT1 output 101: DOUT = INT2 output 110: DOUT = secondary BCLK output for codec interface 111: DOUT = secondary WCLK output for codec interface
D0	R/W	0	0: DOUT general-purpose output value = 0 1: DOUT general-purpose output value = 1

Table 7-95. Page 0 / Register 54: DIN (IN Pin) Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Reserved
D2–D1	R/W	01	00: DIN disabled (input buffer powered down) 01: DIN enabled (can be used as DIN for codec interface, Dig_Mic_In or into ClockGen block) 10: DIN is used as general-purpose input (GPI) 11: Reserved
D0	R	X	DIN input-buffer value

Table 7-96. Page 0 / Register 55: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0010	Reserved

Table 7-97. Page 0 / Register 56: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 001X	Reserved

Table 7-98. Page 0 / Register 57: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W		Reserved. Write only reset value.

Table 7-99. Page 0 / Register 58: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	000X 0000	Reserved. Write only reset value.

Table 7-100. Page 0 / Register 59: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Reserved. Write only zeros to these bits.

Table 7-101. Page 0 / Register 60: DAC Instruction Set

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only default value.
D4–D0	R/W	00 0001	0 0000: Reserved. Write only reset value. 0 0001: DAC signal-processing block PRB_P1 0 0010: DAC signal-processing block PRB_P2 0 0011: DAC signal-processing block PRB_P3 0 0100: DAC signal-processing block PRB_P4 ... 1 1000: DAC signal-processing block PRB_P24 1 1001: DAC signal-processing block PRB_P25 1 1010–1 1111: Reserved. Do not use.

Table 7-102. Page 0 / Register 61: ADC Instruction Set

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only default values.
D4–D0	R/W	0 0100	0 0000: Reserved. Write only reset value. 0 0001–0 0011: Reserved 0 0100: ADC signal-processing block PRB_R4 0 0101: ADC signal-processing block PRB_R5 0 0110: ADC signal-processing block PRB_R6 0 0111–01001: Reserved 0 1010: ADC signal-processing block PRB_R10 0 1011: ADC signal-processing block PRB_R11 0 1100: ADC signal-processing block PRB_R12 0 1101–0 1111: Reserved 1 0000: ADC signal-processing block PRB_R16 1 0001: ADC signal-processing block PRB_R17 1 0010: ADC signal-processing block PRB_R18 1 0011–1 1111: Reserved. Do not write these sequences to these bits.

Table 7-103. Page 0 / Register 62: Programmable Instruction Mode-Control Bits

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved
D6	R/W	0	ADC PRB engine auxiliary control bit A, which can be used for conditional instructions like JMP
D5	R/W	0	ADC PRB engine auxiliary control bit B, which can be used for conditional instructions like JMP
D4	R/W	0	0: Reset ADC PRB instruction counter at the start of the new frame. 1: Do not reset ADC PRB instruction counter at the start of the new frame.
D3	R/W	0	Reserved
D2	R/W	0	DAC PRB engine auxiliary control bit A, which can be used for conditional instructions like JMP
D1	R/W	0	DAC PRB engine auxiliary control bit B, which can be used for conditional instructions like JMP
D0	R/W	0	0: Reset DAC PRB instruction counter at the start of the new frame. 1: Do not reset DAC PRB instruction counter at the start of the new frame.

Table 7-104. Page 0 / Register 63: DAC Data-Path Setup

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left-channel DAC is powered down. 1: Left-channel DAC is powered up.
D6	R/W	0	0: Right-channel DAC is powered down. 1: Right-channel DAC is powered up.
D5–D4	R/W	01	00: Left-channel DAC data path = off 01: Left-channel DAC data path = left data 10: Left-channel DAC data path = right data 11: Left-channel DAC data path = left-channel and right-channel data [(L + R) / 2]
D3–D2	R/W	01	00: Right-channel DAC data path = off 01: Right-channel DAC data path = right data 10: Right-channel DAC data path = left data 11: Right-channel DAC data path = left-channel and right-channel data [(L + R) / 2]
D1–D0	R/W	00	00: DAC-channel volume-control soft-stepping is enabled for one step per sample period. 01: DAC-channel volume-control soft-stepping is enabled for one step per two sample periods. 10: DAC-channel volume-control soft-stepping is disabled. 11: Reserved. Do not write this sequence to these bits.

Table 7-105. Page 0 / Register 64: DAC Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only zeros to these bits.
D3	R/W	1	0: Left-channel DAC not muted 1: Left-channel DAC muted

Table 7-105. Page 0 / Register 64: DAC Volume Control (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R/W	1	0: Right-channel DAC not muted 1: Right-channel DAC muted
D1–D0	R/W	00	00: Left and right channels have independent volume control.(1) 01: Left-channel volume control Is the programmed value of right-channel volume control. 10: Right-channel volume control is the programmed value of left-channel volume control. 11: Same as 00

(1) When DRC is enabled, left and right channel volume controls are always independent. Program bits D1–D0 to 00.

Table 7-106. Page 0 / Register 65: DAC Left Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0111 1111–0011 0001: Do not write these sequences to these bits. 0011 0000: Left-channel DAC digital volume = 24 dB 0010 1111: Left-channel DAC digital volume = 23.5 dB 0010 1110: Left-channel DAC digital volume = 23 dB ... 0000 0001: Left-channel DAC digital volume = 0.5 dB 0000 0000: Left-channel DAC digital volume = 0 dB 1111 1111: Left-channel DAC digital volume = –0.5 dB ... 1000 0010: Left-channel DAC digital volume = –63 dB 1000 0001: Left-channel DAC digital volume = –63.5 dB 1000 0000: Reserved. Do not use.

Table 7-107. Page 0 / Register 66: DAC Right Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0111 1111–0011 0001: Reserved. Do not write these sequences to these bits. 0011 0000: Right-channel DAC digital volume = 24 dB 0010 1111: Right-channel DAC digital volume = 23.5 dB 0010 1110: Right-channel DAC digital volume = 23 dB ... 0000 0001: Right-channel DAC digital volume = 0.5 dB 0000 0000: Right-channel DAC digital volume = 0 dB 1111 1111: Right-channel DAC digital volume = –0.5 dB ... 1000 0010: Right-channel DAC digital volume = –63 dB 1000 0001: Right-channel DAC digital volume = –63.5 dB 1000 0000: Reserved. Do not use.

Table 7-108. Page 0 / Register 67: Headset Detection

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset detection disabled 1: Headset detection enabled
D6–D5	R	XX	00: No headset detected 01: Headset without microphone is detected 10: Reserved 11: Headset with microphone is detected
D4–D2	R/W	000	Debounce Programming for Glitch Rejection During Headset Detection(1) 000: 16 ms (sampled with 2-ms clock) 001: 32 ms (sampled with 4-ms clock) 010: 64 ms (sampled with 8-ms clock) 011: 128 ms (sampled with 16-ms clock) 100: 256 ms (sampled with 32-ms clock) 101: 512 ms (sampled with 64-ms clock) 110: Reserved 111: Reserved

(1) Note that these times are generated using the 1 MHz reference clock which is defined in Page 3 / Register 16.

Table 7-108. Page 0 / Register 67: Headset Detection (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1–D0	R/W	00	Debounce programming for glitch rejection during headset button-press detection 00: 0 ms 01: 8 ms (sampled with 1-ms clock) 10: 16 ms (sampled with 2-ms clock) 11: 32 ms (sampled with 4-ms clock)

Table 7-109. Page 0 / Register 68: DRC Control 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only the reset value to these bits.
D6	R/W	0	0: DRC disabled for left channel 1: DRC enabled for left channel
D5	R/W	0	0: DRC disabled for right channel 1: DRC enabled for right channel
D4–D2	R/W	011	000: DRC threshold = –3 dB 001: DRC threshold = –6 dB 010: DRC threshold = –9 dB 011: DRC threshold = –12 dB 100: DRC threshold = –15 dB 101: DRC threshold = –18 dB 110: DRC threshold = –21 dB 111: DRC threshold = –24 dB
D1–D0	R/W	11	00: DRC hysteresis = 0 dB 01: DRC hysteresis = 1 dB 10: DRC hysteresis = 2 dB 11: DRC hysteresis = 3 dB

Table 7-110. Page 0 / Register 69: DRC Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D	R	0	Reserved. Write only the reset value to these bits.
D6–D3	R/W	0111	DRC Hold Time 0000: DRC Hold Disabled 0001: DRC Hold Time = 32 DAC Word Clocks 0010: DRC Hold Time = 64 DAC Word Clocks 0011: DRC Hold Time = 128 DAC Word Clocks 0100: DRC Hold Time = 256 DAC Word Clocks 0101: DRC Hold Time = 512 DAC Word Clocks 0110: DRC Hold Time = 1024 DAC Word Clocks 0111: DRC Hold Time = 2048 DAC Word Clocks 1000: DRC Hold Time = 4096 DAC Word Clocks 1001: DRC Hold Time = 8192 DAC Word Clocks 1010: DRC Hold Time = 16 384 DAC Word Clocks 1011: DRC Hold Time = 32 768 DAC Word Clocks 1100: DRC Hold Time = 65 536 DAC Word Clocks 1101: DRC Hold Time = 98 304 DAC Word Clocks 1110: DRC Hold Time = 131 072 DAC Word Clocks 1111: DRC Hold Time = 163 840 DAC Word Clocks
D2-D0	R	000	Reserved. Write only the reset value to these bits.

Table 7-111. Page 0 / Register 70: DRC Control 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	0000: DRC attack rate = 4 dB per DAC Word Clock 0001: DRC attack rate = 2 dB per DAC word clock 0010: DRC attack rate = 1 dB per DAC word clock ... 1110: DRC attack rate = 2.4414e–5 dB per DAC word clock 1111: DRC attack rate = 1.2207e–5 dB per DAC word clock

Table 7-111. Page 0 / Register 70: DRC Control 3 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D0	R/W	0000	Decay Rate is defined as DR / $2^{[\text{bits D3-D0 value}]}$ dB per DAC Word Clock, where DR = 0.015625 dB 0000: DRC decay rate (DR) = 0.015625 dB per DAC Word Clock 0001: DRC decay rate = DR / 2 dB per DAC Word Clock 0010: DRC decay rate = DR / 2^2 dB per DAC Word Clock 0011: DRC decay rate = DR / 2^3 dB per DAC Word Clock 0100: DRC decay rate = DR / 2^4 dB per DAC Word Clock 0101: DRC decay rate = DR / 2^5 dB per DAC Word Clock 0110: DRC decay rate = DR / 2^6 dB per DAC Word Clock 0111: DRC decay rate = DR / 2^7 dB per DAC Word Clock 1000: DRC decay rate = DR / 2^8 dB per DAC Word Clock 1001: DRC decay rate = DR / 2^9 dB per DAC Word Clock 1010: DRC decay rate = DR / 2^{10} dB per DAC Word Clock 1011: DRC decay rate = DR / 2^{11} dB per DAC Word Clock 1100: DRC decay rate = DR / 2^{12} dB per DAC Word Clock 1101: DRC decay rate = DR / 2^{13} dB per DAC Word Clock 1110: DRC decay rate = DR / 2^{14} dB per DAC Word Clock 1111: DRC decay rate = DR / 2^{15} dB per DAC Word Clock

Table 7-112. Page 0 / Register 71: Left Beep Generator (1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Beep generator is disabled. 1: Beep generator is enabled (self-clearing based on beep duration).
D6	R/W	0	Reserved. Write only reset value.
D5–D0	R/W	00 0000	00 0000: Left-channel beep volume control = 2 dB 00 0001: Left-channel beep volume control = 1 dB 00 0010: Left-channel beep volume control = 0 dB 00 0011: Left-channel beep volume control = –1 dB ... 11 1110: Left-channel beep volume control = –60 dB 11 1111: Left-channel beep volume control = –61 dB

(1) The beep generator is only available in PRB_P25 DAC processing mode.

Table 7-113. Page 0 / Register 72: Right Beep Generator(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: Left and right channels have independent beep volume control. 01: Left-channel beep volume control is the programmed value of right-channel beep volume control. 10: Right-channel beep volume control is the programmed value of left-channel beep volume control. 11: Same as 00
D5–D0	R/W	00 0000	00 0000: Right-channel beep volume control = 2 dB 00 0001: Right-channel beep volume control = 1 dB 00 0010: Right-channel beep volume control = 0 dB 00 0011: Right-channel beep volume control = –1 dB ... 11 1110: Right-channel beep volume control = –60 dB 11 1111: Right-channel beep volume control = –61 dB

(1) The beep generator is only available in PRB_P25 DAC processing mode.

Table 7-114. Page 0 / Register 73: Beep Length MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	8 MSBs out of 24 bits for the number of samples for which the beep must be generated.

Table 7-115. Page 0 / Register 74: Beep-Length Middle Bits

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	8 middle bits out of 24 bits for the number of samples for which the beep must be generated.

Table 7-116. Page 0 / Register 75: Beep Length LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	8 LSBs out of 24 bits for the number of samples for which beep must be generated.

Table 7-117. Page 0 / Register 76: Beep Sin(x) MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0001 0000	8 MSBs out of 16 bits for $\sin(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-118. Page 0 / Register 77: Beep Sin(x) LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1101 1000	8 LSBs out of 16 bits for $\sin(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-119. Page 0 / Register 78: Beep Cos(x) MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	8 MSBs out of 16 bits for $\cos(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-120. Page 0 / Register 79: Beep Cos(x) LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	8 LSBs out of 16 bits for $\cos(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-121. Page 0 / Register 80: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only the reset value to these bits.

Table 7-122. Page 0 / Register 81: ADC Digital Mic

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: ADC channel is powered down. 1: ADC channel is powered up.
D6	R/W	0	Reserved
D5–D4	R/W	00	00: Digital microphone input is obtained from GPIO1 pin. 01: Reserved. 10: Digital microphone input is obtained from DIN pin. 11: Reserved.
D3	R/W	0	0: Digital microphone is not enabled for delta-sigma mono ADC channel. 1: Digital microphone is enabled for delta-sigma mono ADC channel
D2	R/W	0	Reserved
D1–D0	R/W	00	00: ADC channel volume control soft-stepping is enabled for one step per sample period. 01: ADC channel volume control soft-stepping is enabled for one step per two sample periods. 10: ADC channel volume control soft-stepping is disabled. 11: Reserved. Do not write this sequence to these bits.

Table 7-123. Page 0 / Register 82: ADC Digital Volume Control Fine Adjust

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: ADC channel not muted 1: ADC channel muted
D6–D4	R/W	000	Delta-Sigma Mono ADC Channel Volume Control Fine Gain 000: 0 dB 001: –0.1 dB 010: –0.2 dB 011: –0.3 dB 100: –0.4 dB 101–111: Reserved
D3–D0	R/W	0000	Reserved. Write only zeros to these bits.

Table 7-124. Page 0 / Register 83: ADC Digital Volume Control Coarse Adjust

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved
D6–D0		000 0000	Delta-Sigma Mono ADC Channel Volume-Control Coarse Gain 100 0000–110 0111: Reserved 110 1000: –12 dB 110 1001: –11.5 dB ... 111 1111: –0.5 dB 000 0000: 0 dB 000 0001: 0.5 dB ... 010 0111: 19.5 dB 010 1000: 20 dB 010 1001–011 1111: Reserved

Table 7-125. Page 0 / Register 84 and Page 0 / Register 85: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	XXXX XXXX	Reserved. Write only the reset value to these bits.

Table 7-126. Page 0 / Register 86: AGC Control 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: AGC disabled 1: AGC enabled
D6–D4	R/W	000	000: AGC target level = –5.5 dB 001: AGC target level = –8 dB 010: AGC target level = –10 dB 011: AGC target level = –12 dB 100: AGC target level = –14 dB 101: AGC target level = –17 dB 110: AGC target level = –20 dB 111: AGC target level = –24 dB
D3–D0	R/W	0000	Reserved. Write only zeros to these bits.

Table 7-127. Page 0 / Register 87: AGC Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: AGC hysterysis setting of 1 dB 01: AGC hysterysis setting of 2 dB 10: AGC hysterysis setting of 4 dB 11: AGC hysterysis disabled

Table 7-127. Page 0 / Register 87: AGC Control 2 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5–D1	R/W	00 000	00 000: AGC noise and silence detection is disabled. 00 001: AGC noise threshold = –30 dB 00 010: AGC noise threshold = –32 dB 00 011: AGC noise threshold = –34 dB ... 11 101: AGC noise threshold = –86 dB 11 110: AGC noise threshold = –88 dB 11 111: AGC noise threshold = –90 dB
D0	R/W	0	Reserved. Write only zero to this bit.

Table 7-128. Page 0 / Register 88: AGC Maximum Gain

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6–D0	R/W	111 1111	000 0000: AGC maximum gain = 0 dB 000 0001: AGC maximum gain = 0.5 dB 000 0010: AGC maximum gain = 1 dB ... 111 0011: AGC maximum gain = 57.5 dB 111 0100: AGC maximum gain = 58 dB 111 0101: AGC maximum gain = 58.5 dB 111 0110: AGC maximum gain = 59 dB 111 0111: AGC maximum gain = 59.5 dB 111 1000–111 1111: Reserved. Do not write these sequences to these bits.

Table 7-129. Page 0 / Register 89: AGC Attack Time

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	0000 0: AGC attack time = 1 × (32 / f_S) where f_S is the ADC sample rate 0000 1: AGC attack time = 3 × (32 / f_S) where f_S is the ADC sample rate 0001 0: AGC attack time = 5 × (32 / f_S) where f_S is the ADC sample rate 0001 1: AGC attack time = 7 × (32 / f_S) where f_S is the ADC sample rate 0010 0: AGC attack time = 9 × (32 / f_S) where f_S is the ADC sample rate ... 1111 0: AGC attack time = 61 × (32 / f_S) where f_S is the ADC sample rate 1111 1: AGC attack time = 63 × (32 / f_S) where f_S is the ADC sample rate
D2–D0	R/W	000	000: Multiply factor for the programmed AGC attack time = 1 001: Multiply factor for the programmed AGC attack time = 2 010: Multiply factor for the programmed AGC attack time = 4 ... 111: Multiply factor for the programmed AGC attack time = 128

Table 7-130. Page 0 / Register 90: AGC Decay Time

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	0000 0: AGC decay time = 1 × (512 / f_S) 0000 1: AGC decay time = 3 × (512 / f_S) 0001 0: AGC decay time = 5 × (512 / f_S) 0001 1: AGC decay time = 7 × (512 / f_S) 0010 0: AGC decay time = 9 × (512 / f_S) ... 1111 0: AGC decay time = 61 × (512 / f_S) 1111 1: AGC decay time = 63 × (512 / f_S)
D2–D0	R/W	000	000: Multiply factor for the programmed AGC decay time = 1 001: Multiply factor for the programmed AGC decay time = 2 010: Multiply factor for the programmed AGC decay time = 4 ... 111: Multiply factor for the programmed AGC decay time = 128

Table 7-131. Page 0 / Register 91: AGC Noise Debounce

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only zeros to these bits.
D4–D0	R/W	0 0000	0 0000: AGC noise debounce = 0 / f_S 0 0001: AGC noise debounce = 4 / f_S 0 0010: AGC noise debounce = 8 / f_S 0 0011: AGC noise debounce = 16 / f_S 0 0100: AGC noise debounce = 32 / f_S 0 0101: AGC noise debounce = 64 / f_S 0 0110: AGC noise debounce = 128 / f_S 0 0111: AGC noise debounce = 256 / f_S 0 1000: AGC noise debounce = 512 / f_S 0 1001: AGC noise debounce = 1024 / f_S 0 1010: AGC noise debounce = 2048 / f_S 0 1011: AGC noise debounce = 4096 / f_S 0 1100: AGC noise debounce = 2 × 4096 / f_S 0 1101: AGC noise debounce = 3 × 4096 / f_S 0 1110: AGC noise debounce = 4 × 4096 / f_S ... 1 1110: AGC noise debounce = 20 × 4096 / f_S 1 1111: AGC noise debounce = 21 × 4096 / f_S

Table 7-132. Page 0 / Register 92: AGC Signal Debounce

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only zeros to these bits.
D3–D0	R/W	0000	0000: AGC signal debounce = 0 / f_S 0001: AGC signal debounce = 4 / f_S 0010: AGC signal debounce = 8 / f_S 0011: AGC signal debounce = 16 / f_S 0100: AGC signal debounce = 32 / f_S 0101: AGC signal debounce = 64 / f_S 0110: AGC signal debounce = 128 / f_S 0111: AGC signal debounce = 256 / f_S 1000: AGC signal debounce = 512 / f_S 1001: AGC signal debounce = 1024 / f_S 1010: AGC signal debounce = 2048 / f_S 1011: AGC signal debounce = 2 × 2048 / f_S 1100: AGC signal debounce = 3 × 2048 / f_S 1101: AGC signal debounce = 4 × 2048 / f_S 1110: AGC signal debounce = 5 × 2048 / f_S 1111: AGC signal debounce = 6 × 2048 / f_S

Table 7-133. Page 0 / Register 93: AGC Gain-Applied Reading

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	1110 1000: Gain applied by AGC = –12 dB 1110 1001: Gain applied by AGC = –11.5 dB 1110 1010: Gain applied by AGC = –11 dB ... 1111 1111: Gain applied by AGC = –0.5 dB 0000 0000: Gain applied by AGC = 0 dB 0000 0001 Gain applied by AGC = 0.5 dB ... 0111 0101: Gain applied by AGC = 58.5 dB 0111 0110: Gain applied by AGC = 59 dB 0111 0111: Gain applied by AGC = 59.5 dB

Table 7-134. Page 0 / Register 94 Through Page 0 / Register 101: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-135. Page 0 / Register 102: ADC DC Measurement 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DC measurement is disabled for mono ADC channel 1: DC measurement is enabled for mono ADC channel
D6	R/W	0	Reserved. Write only reset value.
D5	R/W	0	0: DC measurement occurs based on first-order sync filter with averaging of 2^D 1: DC measurement occurs based on first-order low-pass IIR filter whose coefficients are calculated based on D value
D4–D0	R/W	00000	DC Measurement D setting: 00000: Reserved. Don't use. 00001: D = 1 00010: D = 2 ... 10011: D = 19 10100: D = 20 10101 to 11111: Reserved. Don't use.

Table 7-136. Page 0 / Register 103: ADC DC Measurement 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only reset value.
D6	R/W	0	0: DC measurement data update is enabled. 1: DC measurement data update is disabled. User can read the last updated data without any data corruption.
D5	R/W	0	0: For IIR based DC measurement, the measurement value is the instantaneous output of the IIR filter 1: For IIR based DC measurement, the measurement value is update before periodic clearing of the IIR filter
D4–D0	R/W	00000	IIR based DC measurement, average time setting: 00000: Infinite average is used 00001: Averaging time is 2^1 ADC modulator clock periods 00010: Averaging time is 2^2 ADC modulator clock periods ... 10011: Averaging time is 2^{19} ADC modulator clock periods 10100: Averaging time is 2^{20} ADC modulator clock periods 10101 to 11111: Reserved. Don't use.

Table 7-137. Page 0 / Register 104: ADC DC Measurement Output 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	ADC DC Measurement Output (23:16)

Table 7-138. Page 0 / Register 105: ADC DC Measurement Output 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	ADC DC Measurement Output (15:8)

Table 7-139. Page 0 / Register 106: ADC DC Measurement Output 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	ADC DC Measurement Output (7:0)

Table 7-140. Page 0 / Register 107 Through Page 0 / Register 115: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-141. Page 0 / Register 116: VOL/MICDET-Pin SAR ADC — Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION		
D7	R/W	0	0: DAC volume control is controlled by control register. (7-bit Vol ADC is powered down) 1: DAC volume control is controlled by pin.		
D6	R/W	0	0: Internal on-chip RC oscillator is used for the 7-bit Vol ADC for pin volume control. 1: MCLK is used for the 7-bit Vol ADC for pin volume control.		
D5–D4	R/W	00	00: No hysteresis for volume control ADC output 01: Hysteresis of ±1 bit 10: Hysteresis of ±2 bits 11: Reserved. Do not write this sequence to these bits.		
D3	R/W	0	Reserved. Write only reset value.		
D2–D0	R/W	000	Throughput of the 7-bit Vol ADC for pin volume control, frequency based on MCLK or internal oscillator.		
				MCLK = 12 MHz	**Internal Oscillator Source**
			000: Throughput = 001: Throughput = 010: Throughput = 011: Throughput = 100: Throughput = 101: Throughput = 110: Throughput = 111: Throughput =	15.625 Hz 31.25 Hz 62.5 Hz 125 Hz 250 Hz 500 Hz 1 kHz 2 kHz	10.68 Hz 21.35 Hz 42.71 Hz 8.2 Hz 170 Hz 340 Hz 680 Hz 1.37 kHz **Note**: These values are based on a nominal oscillator frequency of 8.2 MHz. The values scale to the actual oscillator frequency.

Table 7-142. Page 0 / Register 117: VOL/MICDET-Pin Gain

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6–D0	R	XXX XXXX	000 0000: Gain applied by pin volume control = 18 dB 000 0001: Gain applied by pin volume control = 17.5 dB 000 0010: Gain applied by pin volume control = 17 dB ... 010 0011: Gain applied by pin volume control = 0.5 dB 010 0100: Gain applied by pin volume control = 0 dB 010 0101: Gain applied by pin volume control = –0.5 dB ... 101 1001: Gain applied by pin volume control = –26.5 dB 101 1010: Gain applied by pin volume control = –27 dB 101 1011: Gain applied by pin volume control = –28 dB ... 111 1101: Gain applied by pin volume control = –62 dB 111 1110: Gain applied by pin volume control = –63 dB 111 1111: Reserved.

Table 7-143. Page 0 / Register 118 Through Page 0 / Register 127: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

7.4.2.2 Control Registers, Page 1: DAC and ADC Routing, PGA, Power-Controls, and MISC Logic-Related Programmability

Table 7-144. Page 1 / Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

Table 7-145. Page 1 / Register 1 Through Page 1 / Register 29: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-146. Page 1 / Register 30: Headphone and Speaker Amplifier Error Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 00	Reserved
D1	R/W	0	0: Reset speaker driver power-up control bits on short-circuit detection. 1: Speaker driver power-up control bits remain unchanged on short-circuit detection.
D0	R/W	0	0: Reset HPL and HPR power-up control bits on short-circuit detection if page 1 / register 31, D1 = 1. 1: HPL and HPR power-up control bits remain unchanged on short-circuit detection.

Table 7-147. Page 1 / Register 31: Headphone Drivers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: HPL output driver is powered down. 1: HPL output driver is powered up.
D6	R/W	0	0: HPR output driver is powered down. 1: HPR output driver is powered up.
D5	R/W	0	Reserved. Write only zero to this bit.
D4–D3	R/W	0	00: Output common-mode voltage = 1.35 V 01: Output common-mode voltage = 1.5 V 10: Output common-mode voltage = 1.65 V 11: Output common-mode voltage = 1.8 V
D2	R/W	1	Reserved. Write only 1 to this bit.
D1	R/W	0	0: If short-circuit protection is enabled for headphone driver and short circuit detected, device limits the maximum current to the load. 1: If short-circuit protection is enabled for headphone driver and short circuit detected, device powers down the output driver.
D0	R	0	0: Short circuit is not detected on the headphone driver. 1: Short circuit is detected on the headphone driver.

Table 7-148. Page 1 / Register 32: Class-D Speaker Amplifier

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Mono class-D output driver is powered down. 1: Mono class-D output driver is powered up.
D6	R/W	0	0: Reserved 1: Reserved
D5–D1	R/W	00 011	Reserved. Write only the reset value to this bit.

Table 7-148. Page 1 / Register 32: Class-D Speaker Amplifier (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R	0	0: Short circuit is not detected on the class-D driver. Valid only if class-D amplifier is powered up. For short-circuit flag sticky bit, see page 0 / register 44. 1: Short circuit is detected on the class-D driver. Valid only if class-D amp is powered-up. For short-circuit flag sticky bit, see page 0 / register 44.

Table 7-149. Page 1 / Register 33: HP Output Drivers POP Removal Settings

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: If the power down sequence is activated by device software, power down using page 1 / register 46, bit D7, then power down the DAC simultaneously with the HP and SP amplifiers. 1: If the power down sequence is activated by device software, power down using page 1 / register 46, bit D7, then power down DAC only after HP and SP amplifiers are completely powered down. This is to optimize power-down POP.
D6–D3	R/W	0111	0000: Driver power-on time = 0 μs 0001: Driver power-on time = 15.3 μs 0010: Driver power-on time = 153 μs 0011: Driver power-on time = 1.53 ms 0100: Driver power-on time = 15.3 ms 0101: Driver power-on time = 76.2 ms 0110: Driver power-on time = 153 ms 0111: Driver power-on time = 304 ms 1000: Driver power-on time = 610 ms 1001: Driver power-on time = 1.22 s 1010: Driver power-on time = 3.04 s 1011: Driver power-on time = 6.1 s 1100–1111: Reserved. Do not write these sequences to these bits. **Note**: These values are based on typical oscillator frequency of 8.2 MHz. Scale according to the actual oscillator frequency.
D2–D1	R/W	11	00: Driver ramp-up step time = 0 ms 01: Driver ramp-up step time = 0.98 ms 10: Driver ramp-up step time = 1.95 ms 11: Driver ramp-up step time = 3.9 ms **Note**: These values are based on typical oscillator frequency of 8.2 MHz. Scale according to the actual oscillator frequency.
D0	R/W	0	0: Weakly driven output common-mode voltage is generated from resistor divider of the AVDD supply. 1: Reserved

Table 7-150. Page 1 / Register 34: Output Driver PGA Ramp-Down Period Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only the reset value to this bit.
D6–D4	R/W	000	Speaker power-up wait time (duration based on using internal oscillator) 000: Wait time = 0 ms 001: Wait time = 3.04 ms 010: Wait time = 7.62 ms 011: Wait time = 12.2 ms 100: Wait time = 15.3 ms 101: Wait time = 19.8 ms 110: Wait time = 24.4 ms 111: Wait time = 30.5 ms **Note**: These values are based on typical oscillator frequency of 8.2 MHz. Scale according to the actual oscillator frequency.
D3–D0	R/W	0000	Reserved. Write only the reset value to these bits.

Table 7-151. Page 1 / Register 35: DAC_L and DAC_R Output Mixer Routing

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: DAC_L is not routed anywhere. 01: DAC_L is routed to the left-channel mixer amplifier. 10: DAC_L is routed directly to the HPL driver. 11: Reserved
D5	R/W	0	0: MIC1LP input is not routed to the left-channel mixer amplifier. 1: MIC1LP input is routed to the left-channel mixer amplifier.
D4		0	0: MIC1RP input is not routed to the left-channel mixer amplifier. 1: MIC1RP input is routed to the left-channel mixer amplifier.
D3–D2	R/W	00	00: DAC_R is not routed anywhere. 01: DAC_R is routed to the right-channel mixer amplifier. 10: DAC_R is routed directly to the HPR driver. 11: Reserved
D1	R/W	0	0: MIC1RP input is not routed to the right-channel mixer amplifier. 1: MIC1RP input is routed to the right-channel mixer amplifier.
D0	R/W	0	0: HPL driver output is not routed to the HPR driver. 1: HPL driver output is routed to the HPR driver input (used for differential output mode).

Table 7-152. Page 1 / Register 36: Left Analog Volume to HPL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left-channel analog volume 1: Left-channel analog volume control is routed to HPL output driver.
D6–D0	R/W	111 1111	Left-channel analog volume control gain (non-linear) for the HPL output driver, 0 dB to –78 dB. See Table 7-38.

Table 7-153. Page 1 / Register 37: Right Analog Volume to HPR

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right-channel analog volume control is not routed to HPR output driver. 1: Right-channel analog volume control is routed to HPR output driver.
D6–D0	R/W	111 1111	Right-channel analog volume control gain (non-linear) for the HPR output driver, 0 dB to –78 dB. See Table 7-38.

Table 7-154. Page 1 / Register 38: Left Analog Volume to SPK

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left-channel analog volume control output is not routed to mono class-D output driver 1: Left-channel analog volume control output is routed to mono class-D output driver.
D6–D0	R/W	111 1111	Left-channel analog volume control output gain (non-linear) for the mono class-D output driver, 0 dB to –78 dB. See Table 7-38.

Table 7-155. Page 1 / Register 39: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1111	Reserved

Table 7-156. Page 1 / Register 40: HPL Driver

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.

Table 7-156. Page 1 / Register 40: HPL Driver (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D3	R/W	0000	0000: HPL driver PGA = 0 dB 0001: HPL driver PGA = 1 dB 0010: HPL driver PGA = 2 dB ... 1000: HPL driver PGA = 8 dB 1001: HPL driver PGA = 9 dB 1010–1111: Reserved. Do not write these sequences to these bits.
D2	R/W	0	0: HPL driver is muted. 1: HPL driver is not muted.
D1	R/W	1	Reserved
D0	R	0	0: Not all programmed gains to HPL have been applied yet. 1: All programmed gains to HPL have been applied.

Table 7-157. Page 1 / Register 41: HPR Driver

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6–D3	R/W	0000	0000: HPR driver PGA = 0 dB 0001: HPR driver PGA = 1 dB 0010: HPR driver PGA = 2 dB ... 1000: HPR driver PGA = 8 dB 1001: HPR driver PGA = 9 dB 1010–1111: Reserved. Do not write these sequences to these bits.
D2	R/W	0	0: HPR driver is muted. 1: HPR driver is not muted.
D1	R/W	1	Reserved. Write only '1' to this bit.
D0	R	0	0: Not all programmed gains to HPR have been applied yet. 1: All programmed gains to HPR have been applied.

Table 7-158. Page 1 / Register 42: SPK Driver

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only zeros to these bits.
D4–D3	R/W	00	00: Mono class-D driver output stage gain = 6 dB 01: Mono class-D driver output stage gain = 12 dB 10: Mono class-D driver output stage gain = 18 dB 11: Mono class-D driver output stage gain = 24 dB
D2	R/W	0	0: Mono class-D driver is muted. 1: Mono class-D driver is not muted.
D1	R/W	0	Reserved. Write only zero to this bit.
D0	R	0	0: Not all programmed gains to the Mono class-D driver have been applied yet. 1: All programmed gains to the Mono class-D driver have been applied.

Table 7-159. Page 1 / Register 43: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only zeros to these bits.
D4–D3	R/W	00	00: Reserved 01: Reserved 10: Reserved 11: Reserved
D2	R/W	0	0: Reserved 1: Reserved
D1	R/W	0	Reserved. Write only zero to this bit.

Table 7-159. Page 1 / Register 43: Reserved (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R	0	0: Reserved 1: Reserved

Table 7-160. Page 1 / Register 44: HP Driver Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION		
D7–D5	R/W	000	Debounce time for the headset short-circuit detection		
			(1)	**MCLK/DIV (Page 3 / register 16) = 1-MHz Source**	**Internal Oscillator Source**
			000: Debounce time = 001: Debounce time = 010: Debounce time = 011: Debounce time = 100: Debounce time = 101: Debounce time = 110: Debounce time = 111: Debounce time =	0 µs 8 µs 16 µs 32 µs 64 µs 128 µs 256 µs 512 µs	0 µs 7.8 µs 15.6 µs 31.2 µs 62.4 µs 124.9 µs 250 µs 500 µs **Note**: These values are based on a nominal oscillator frequency of 8.2 MHz. The values scale to the actual oscillator frequency.
D4–D3	R/W	00	00: Default mode for the DAC 01: DAC performance increased by increasing the current 10: Reserved 11: DAC performance increased further by increasing the current again		
D2	R/W	0	0: HPL output driver is programmed as headphone driver. 1: HPL output driver is programmed as lineout driver.		
D1	R/W	0	0: HPR output driver is programmed as headphone driver. 1: HPR output driver is programmed as lineout driver.		
D0	R/W	0	Reserved. Write only zero to this bit.		

(1) The clock used for the debounce has a clock period = debounce duration / 8.

Table 7-161. Page 1 / Register 45: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-162. Page 1 / Register 46: MICBIAS

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Device software power down is not enabled. 1: Device software power down is enabled.
D6–D4	R/W	000	Reserved. Write only zeros to these bits.
D3	R/W	0	0: Programmed MICBIAS is not powered up if headset detection is enabled but headset is not inserted. 1: Programmed MICBIAS is powered up even if headset is not inserted.
D2	R/W	0	Reserved. Write only zero to this bit.
D1–D0	R/W	00	00: MICBIAS output is powered down. 01: MICBIAS output is powered to 2 V. 10: MICBIAS output is powered to 2.5 V. 11: MICBIAS output is powered to AVDD.

Table 7-163. Page 1 / Register 47: MIC PGA

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: MIC PGA is controlled by bits D6–D0. 1: MIC PGA is at 0 dB.
D6–D0	R/W	000 0000	000 0000: PGA = 0 dB 000 0001: PGA = 0.5 dB 000 0010: PGA = 1 dB ... 111 0110: PGA = 59 dB 111 0111: PGA = 59.5 dB 111 1000–111 1111: Reserved. Do not write these sequences to these bits.

Table 7-164. Page 1 / Register 48: Delta-Sigma Mono ADC Channel Fine-Gain Input Selection for P-Terminal

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6 (1)	R/W	00	00: MIC1LP is not selected for the MIC PGA. 01: MIC1LP is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ. 10: MIC1LP is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ. 11: MIC1LP is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ.
D5–D4	R/W	00	00: MIC1RP is not selected for the MIC PGA. 01: MIC1RP is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ 10: MIC1RP is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ 11: MIC1RP is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ
D3–D2	R/W	00	00: MIC1LM is not selected for the MIC PGA. 01: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ 10: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ 11: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

(1) Input impedance selection affects the microphone PGA gain. See Section 7.3.9.1 for details.

Table 7-165. Page 1 / Register 49: ADC Input Selection for M-Terminal

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6 (1)	R/W	00	00: CM is not selected for the MIC PGA. 01: CM is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ. 10: CM is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ. 11: CM is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ.
D5–D4		00	00: MIC1LM is not selected for the MIC PGA. 01: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ. 10: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ. 11: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ.
D3–D0	R/W	0000	Reserved. Write only zeros to these bits.

(1) Input impedance selection affects the microphone PGA gain. See Section 7.3.9.1 for details.

Table 7-166. Page 1 / Register 50: Input CM Settings

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: MIC1LP input is floating, if it is not used for the MIC PGA and analog bypass. 1: MIC1LP input is connected to CM internally, if it is not used for the MIC PGA and analog bypass.
D6	R/W	0	0: MIC1RP input is floating, if it is not used for the MIC PGA and analog bypass. 1: MIC1RP input is connected to CM internally, if it is not used for the MIC PGA and analog bypass.
D5	R/W	0	0: MIC1LM input is floating, if it is not used for the MIC PGA. 1: MIC1LM input is connected to CM internally, if it is not used for the MIC PGA.
D4–D1	R/W	00 00	Reserved. Write only zeros to these bits.
D0	R	0	0: Not all programmed analog gains to the ADC have been applied yet. 1: All programmed analog gains to the ADC have been applied.

Table 7-167. Page 1 / Register 51 Through Page 1 / Register 127: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only the reset value to these bits.

7.4.2.3 Control Registers, Page 3: MCLK Divider for Programmable Delay Timer

Default values shown for this page only become valid 100 μs following a hardware or software reset.

Table 7-168. Page 3 / Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The only register used in page 3 is register 16. The remaining page-3 registers are reserved and must not be written to.

Table 7-169. Page 3 / Register 16: Timer Clock MCLK Divider

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Internal oscillator is used for programmable delay timer. 1: External MCLK(1) is used for programmable delay timer.
D6–D0	R/W	000 0001	MCLK Divider to Generate 1-MHz Clock for the Programmable Delay Timer 000 0000: MCLK divider = 128 000 0001: MCLK divider = 1 000 0010: MCLK divider = 2 ... 111 1110: MCLK divider = 126 111 1111: MCLK divider = 127

(1) External clock is used only to control the delay programmed between the conversions and not used for doing the actual conversion. This feature is provided in case a more accurate delay is desired because the internal oscillator frequency varies from device to device.

7.4.2.4 Control Registers, Page 4: ADC Digital Filter Coefficients

Default values shown for this page only become valid 100 μs following a hardware or software reset.

Table 7-170. Page 4 / Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The remaining page-4 registers are either reserved registers or are used for setting coefficients for the various filters in the TLV320AIC3100. Reserved registers must not be written to.

The filter coefficient registers are arranged in pairs, with two adjacent 8-bit registers containing the 16-bit coefficient for a single filter. The 16-bit integer contained in the MSB and LSB registers for a coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32 768 to 32 767. When programming any coefficient value for a filter, the MSB register must always be written first, immediately followed by the LSB register. Even if only the MSB or LSB portion of the coefficient changes, both registers must be written in this sequence. is a list of the page-4 registers, excepting the previously described register 0.

Table 7-171. Page-4 Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	XXXX XXXX	Reserved. Do not write to this register.
2	0000 0001	8 MSBs of N0 coefficient for AGC LPF (first-order IIR) used as averager to detect level
3	0001 0111	8 LSBs of N0 coefficient for AGC LPF (first-order IIR) used as averager to detect level
4	0000 0001	8 MSBs of N1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
5	0001 0111	8 LSBs of N1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
6	0111 1101	8 MSBs of D1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
7	1101 0011	8 LSBs of D1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
8	0111 1111	8 MSBs of N0 coefficient for ADC-programmable first-order IIR
9	1111 1111	8 LSBs of N0 coefficient for ADC-programmable first-order IIR
10	0000 0000	8 MSBs of N1 coefficient for ADC-programmable first-order IIR
11	0000 0000	8 LSBs of N1 coefficient for ADC-programmable first-order IIR
12	0000 0000	8 MSBs of D1 coefficient for ADC-programmable first-order IIR
13	0000 0000	8 LSBs of D1 coefficient for ADC-programmable first-order IIR
14	0111 1111	Coefficient N0(15:8) for ADC biquad A or coefficient FIR0(15:8) for ADC FIR filter
15	1111 1111	Coefficient N0(7:0) for ADC biquad A or coefficient FIR0(7:0) for ADC FIR filter
16	0000 0000	Coefficient N1(15:8) for ADC biquad A or coefficient FIR1(15:8) for ADC FIR filter
17	0000 0000	Coefficient N1(7:0) for ADC biquad A or coefficient FIR1(7:0) for ADC FIR filter
18	0000 0000	Coefficient N2(15:8) for ADC biquad A or coefficient FIR2(15:8) for ADC FIR filter
19	0000 0000	Coefficient N2(7:0) for ADC biquad A or coefficient FIR2(7:0) for ADC FIR filter
20	0000 0000	Coefficient D1(15:8) for ADC biquad A or coefficient FIR3(15:8) for ADC FIR filter
21	0000 0000	Coefficient D1(7:0) for ADC biquad A or coefficient FIR3(7:0) for ADC FIR filter
22	0000 0000	Coefficient D2(15:8) for ADC biquad A or coefficient FIR4(15:8) for ADC FIR filter
23	0000 0000	Coefficient D2(7:0) for ADC biquad A or coefficient FIR4(7:0) for ADC FIR filter
24	0111 1111	Coefficient N0(15:8) for ADC biquad B or coefficient FIR5(15:8) for ADC FIR filter
25	1111 1111	Coefficient N0(7:0) for ADC biquad B or coefficient FIR5(7:0) for ADC FIR filter
26	0000 0000	Coefficient N1(15:8) for ADC biquad B or coefficient FIR6(15:8) for ADC FIR filter
27	0000 0000	Coefficient N1(7:0) for ADC biquad B or coefficient FIR6(7:0) for ADC FIR filter
28	0000 0000	Coefficient N2(15:8) for ADC biquad B or coefficient FIR7(15:8) for ADC FIR filter
29	0000 0000	Coefficient N2(7:0) for ADC biquad B or coefficient FIR7(7:0) for ADC FIR filter
30	0000 0000	Coefficient D1(15:8) for ADC biquad B or coefficient FIR8(15:8) for ADC FIR filter
31	0000 0000	Coefficient D1(7:0) for ADC biquad B or coefficient FIR8(7:0) for ADC FIR filter
32	0000 0000	Coefficient D2(15:8) for ADC biquad B or coefficient FIR9(15:8) for ADC FIR filter
33	0000 0000	Coefficient D2(7:0) for ADC biquad B or coefficient FIR9(7:0) for ADC FIR filter
34	0111 1111	Coefficient N0(15:8) for ADC biquad C or coefficient FIR10(15:8) for ADC FIR filter
35	1111 1111	Coefficient N0(7:0) for ADC biquad C or coefficient FIR10(7:0) for ADC FIR filter
36	0000 0000	Coefficient N1(15:8) for ADC biquad C or coefficient FIR11(15:8) for ADC FIR filter
37	0000 0000	Coefficient N1(7:0) for ADC biquad C or coefficient FIR11(7:0) for ADC FIR filter
38	0000 0000	Coefficient N2(15:8) for ADC biquad C or coefficient FIR12(15:8) for ADC FIR filter
39	0000 0000	Coefficient N2(7:0) for ADC biquad C or coefficient FIR12(7:0) for ADC FIR filter
40	0000 0000	Coefficient D1(15:8) for ADC biquad C or coefficient FIR13(15:8) for ADC FIR filter
41	0000 0000	Coefficient D1(7:0) for ADC biquad C or coefficient FIR13(7:0) for ADC FIR filter
42	0000 0000	Coefficient D2(15:8) for ADC biquad C or coefficient FIR14(15:8) for ADC FIR filter
43	0000 0000	Coefficient D2(7:0) for ADC biquad C or coefficient FIR14(7:0) for ADC FIR filter
44	0111 1111	Coefficient N0(15:8) for ADC biquad D or coefficient FIR15(15:8) for ADC FIR filter
45	1111 1111	Coefficient N0(7:0) for ADC biquad D or coefficient FIR15(7:0) for ADC FIR filter
46	0000 0000	Coefficient N1(15:8) for ADC biquad D or coefficient FIR16(15:8) for ADC FIR filter
47	0000 0000	Coefficient N1(7:0) for ADC biquad D or coefficient FIR16(7:0) for ADC FIR filter

Table 7-171. Page-4 Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
48	0000 0000	Coefficient N2(15:8) for ADC biquad D or coefficient FIR17(15:8) for ADC FIR filter
49	0000 0000	Coefficient N2(7:0) for ADC biquad D or coefficient FIR17(7:0) for ADC FIR filter
50	0000 0000	Coefficient D1(15:8) for ADC biquad D or coefficient FIR18(15:8) for ADC FIR filter
51	0000 0000	Coefficient D1(7:0) for ADC biquad D or coefficient FIR18(7:0) for ADC FIR filter
52	0000 0000	Coefficient D2(15:8) for ADC biquad D or coefficient FIR19(15:8) for ADC FIR filter
53	0000 0000	Coefficient D2(7:0) for ADC biquad D or coefficient FIR19(7:0) for ADC FIR filter
54	0111 1111	Coefficient N0(15:8) for ADC biquad E or coefficient FIR20(15:8) for ADC FIR filter
55	1111 1111	Coefficient N0(7:0) for ADC biquad E or coefficient FIR20(7:0) for ADC FIR filter
56	0000 0000	Coefficient N1(15:8) for ADC biquad E or coefficient FIR21(15:8) for ADC FIR filter
57	0000 0000	Coefficient N1(7:0) for ADC biquad E or coefficient FIR21(7:0) for ADC FIR filter
58	0000 0000	Coefficient N2(15:8) for ADC biquad E or coefficient FIR22(15:8) for ADC FIR filter
59	0000 0000	Coefficient N2(7:0) for ADC biquad E or coefficient FIR22(7:0) for ADC FIR filter
60	0000 0000	Coefficient D1(15:8) for ADC biquad E or coefficient FIR23(15:8) for ADC FIR filter
61	0000 0000	Coefficient D1(7:0) for ADC biquad E or coefficient FIR23(7:0) for ADC FIR filter
62	0000 0000	Coefficient D2(15:8) for ADC biquad E or coefficient FIR24(15:8) for ADC FIR filter
63	0000 0000	Coefficient D2(7:0) for ADC biquad E or coefficient FIR24(7:0) for ADC FIR filter
64-127	0000 0000	Reserved. Write only reset values.

7.4.2.5 Control Registers, Page 8: DAC Digital Filter Coefficients

Default values shown for this page only become valid 100 μs following a hardware or software reset.

Table 7-172. Page 8 / Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The remaining page-8 registers are either reserved registers or are used for setting coefficients for the various filters in the TLV320AIC3100. Reserved registers must not be written to.

The filter coefficient registers are arranged in pairs, with two adjacent 8-bit registers containing the 16-bit coefficient for a single filter. The 16-bit integer contained in the MSB and LSB registers for a coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32 768 to 32 767. When programming any coefficient value for a filter, the MSB register must always be written first, immediately followed by the LSB register. Even if only the MSB or LSB portion of the coefficient changes, both registers must be written in this sequence. is a list of the page-8 registers, excepting the previously described register 0.

Table 7-173. Page 8 / Register 1: DAC Coefficient Buffer Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only the reset value.
D3	R	0	DAC PRB generated flag for toggling MSB of coefficient RAM address (only used in non-adaptive mode)
D2	R/W	0	DAC Adaptive Filtering Control 0: Adaptive filtering disabled in DAC processing blocks 1: Adaptive filtering enabled in DAC processing blocks

Table 7-173. Page 8 / Register 1: DAC Coefficient Buffer Control (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1	R	0	DAC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, DAC processing blocks accesses DAC coefficient Buffer A and the external control interface accesses DAC coefficient Buffer B 1: In adaptive filter mode, DAC processing blocks accesses DAC coefficient Buffer B and the external control interface accesses DAC coefficient Buffer A
D0	R/W	0	DAC Adaptive Filter Buffer Switch Control 0: DAC coefficient buffers are not switched at the next frame boundary. 1: DAC coefficient buffers are switched at the next frame boundary, if adaptive filtering mode is enabled. This bit self-clears on switching.

Table 7-174. Page-8 DAC Buffer A Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
2 (0x02)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad A
3	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad A
4	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad A
5	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad A
6	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad A
7	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad A
8	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad A
9	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad A
10	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad A
11	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad A
12	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad B
13	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad B
14	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad B
15	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad B
16	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad B
17	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad B
18	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad B
19	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad B
20	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad B
21	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad B
22	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad C
23	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad C
24	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad C
25	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad C
26	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad C
27	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad C
28	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad C

Table 7-174. Page-8 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
29	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad C
30	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad C
31	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad C
32	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad D
33	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad D
34	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad D
35	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad D
36	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad D
37	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad D
38	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad D
39	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad D
40	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad D
41	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad D
42	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad E
43	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad E
44	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad E
45	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad E
46	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad E
47	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad E
48	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad E
49	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad E
50	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad E
51	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad E
52	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad F
53	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad F
54	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad F
55	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad F
56	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad F
57	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad F
58	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad F
59	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad F
60	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad F
61	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad F
62	0000 0000	Reserved
63	0000 0000	Reserved
64	0000 0000	8 MSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
65	0000 0000	8 LSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
66	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad A
67	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad A
68	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad A
69	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad A
70	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad A
71	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad A
72	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad A
73	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad A
74	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad A
75	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad A

Table 7-174. Page-8 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
76	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad B
77	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad B
78	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad B
79	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad B
80	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad B
81	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad B
82	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad B
83	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad B
84	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad B
85	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad B
86	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad C
87	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad C
88	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad C
89	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad C
90	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad C
91	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad C
92	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad C
93	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad C
94	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad C
95	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad C
96	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad D
97	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad D
98	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad D
99	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad D
100	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad D
101	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad D
102	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad D
103	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad D
104	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad D
105	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad D
106	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad E
107	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad E
108	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad E
109	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad E
110	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad E
111	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad E
112	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad E
113	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad E
114	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad E
115	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad E
116	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad F
117	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad F
118	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad F
119	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad F
120	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad F
121	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad F
122	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad F

Table 7-174. Page-8 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
123	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad F
124	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad F
125	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad F
126	0000 0000	Reserved
127	0000 0000	Reserved

7.4.2.6 Control Registers, Page 9: DAC Digital Filter Coefficients

Default values shown for this page only become valid 100 μs following a hardware or software reset.

Table 7-175. Page 9 / Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The remaining page-9 registers are either reserved registers or are used for setting coefficients for the various filters in the TLV320AIC3100. Reserved registers must not be written to.

The filter-coefficient registers are arranged in pairs, with two adjacent 8-bit registers containing the 16-bit coefficient for a single filter. The 16-bit integer contained in the MSB and LSB registers for a coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32 768 to 32 767. When programming any coefficient value for a filter, the MSB register must always be written first, immediately followed by the LSB register. Even if only the MSB or LSB portion of the coefficient changes, both registers must be written in this sequence. is a list of the page-9 registers, excepting the previously described register 0.

Table 7-176. Page-9 DAC Buffer A Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	XXXX XXXX	Reserved. Do not write to this register.
2	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable first-order IIR
3	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable first-order IIR
4	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable first-order IIR
5	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable first-order IIR
6	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable first-order IIR
7	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable first-order IIR
8	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable first-order IIR
9	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable first-order IIR
10	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable first-order IIR
11	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable first-order IIR
12	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable first-order IIR
13	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable first-order IIR
14	0111 1111	8 MSBs of n0 coefficient for DRC first-order high-pass filter
15	1111 0111	8 LSBs of n0 coefficient for DRC first-order high-pass filter
16	1000 0000	8 MSBs of n1 coefficient for DRC first-order high-pass filter
17	0000 1001	8 LSBs of n1 coefficient for DRC first-order high-pass filter
18	0111 1111	8 MSBs of d1 coefficient for DRC first-order high-pass filter

Table 7-176. Page-9 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
19	1110 1111	8 LSBs of d1 coefficient for DRC first-order high-pass filter
20	0000 0000	8 MSBs of n0 coefficient for DRC first-order low-pass filter
21	0001 0001	8 LSBs of n0 coefficient for DRC first-order low-pass filter
22	0000 0000	8 MSBs of n1 coefficient for DRC first-order low-pass filter
23	0001 0001	8 LSBs of n1 coefficient for DRC first-order low-pass filter
24	0111 1111	8 MSBs of d1 coefficient for DRC first-order low-pass filter
25	1101 1110	8 LSBs of d1 coefficient for DRC first-order low-pass filter
26-127	0000 0000	Reserved

7.4.2.7 Control Registers, Page 12: DAC Programmable Coefficients Buffer B (1:63)

Table 7-177. Page-12 DAC Buffer B Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	0000 0000	Reserved. Do not write to this register.
2	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad A
3	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad A
4	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad A
5	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad A
6	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad A
7	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad A
8	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad A
9	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad A
10	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad A
11	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad A
12	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad B
13	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad B
14	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad B
15	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad B
16	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad B
17	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad B
18	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad B
19	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad B
20	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad B
21	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad B
22	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad C
23	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad C
24	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad C
25	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad C
26	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad C
27	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad C
28	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad C
29	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad C
30	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad C
31	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad C
32	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad D
33	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad D

Table 7-177. Page-12 DAC Buffer B Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
34	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad D
35	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad D
36	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad D
37	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad D
38	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad D
39	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad D
40	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad D
41	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad D
42	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad E
43	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad E
44	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad E
45	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad E
46	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad E
47	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad E
48	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad E
49	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad E
50	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad E
51	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad E
52	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad F
53	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad F
54	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad F
55	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad F
56	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad F
57	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad F
58	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad F
59	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad F
60	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad F
61	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad F
62	0000 0000	Reserved
63	0000 0000	Reserved
64	0000 0000	8 MSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
65	0000 0000	8 LSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
66	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad A
67	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad A
68	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad A
69	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad A
70	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad A
71	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad A
72	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad A
73	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad A
74	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad A
75	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad A
76	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad B
77	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad B
78	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad B
79	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad B
80	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad B

Table 7-177. Page-12 DAC Buffer B Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
81	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad B
82	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad B
83	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad B
84	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad B
85	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad B
86	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad C
87	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad C
88	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad C
89	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad C
90	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad C
91	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad C
92	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad C
93	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad C
94	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad C
95	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad C
96	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad D
97	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad D
98	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad D
99	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad D
100	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad D
101	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad D
102	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad D
103	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad D
104	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad D
105	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad D
106	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad E
107	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad E
108	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad E
109	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad E
110	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad E
111	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad E
112	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad E
113	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad E
114	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad E
115	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad E
116	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad F
117	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad F
118	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad F
119	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad F
120	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad F
121	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad F
122	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad F
123	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad F
124	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad F
125	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad F
126	0000 0000	Reserved
127	0000 0000	Reserved

7.4.2.8 Control Registers, Page 13: DAC Programmable Coefficients RAM Buffer B (65:127)

Table 7-178. Page-13 DAC Buffer B Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	0000 0000	Reserved. Do not write to this register.
2	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable first-order IIR
3	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable first-order IIR
4	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable first-order IIR
5	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable first-order IIR
6	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable first-order IIR
7	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable first-order IIR
8	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable first-order IIR
9	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable first-order IIR
10	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable first-order IIR
11	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable first-order IIR
12	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable first-order IIR
13	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable first-order IIR
14	0111 1111	8 MSBs of n0 coefficient for DRC first-order high-pass filter
15	1111 0111	8 LSBs of n0 coefficient for DRC first-order high-pass filter
16	1000 0000	8 MSBs of n1 coefficient for DRC first-order high-pass filter
17	0000 1001	8 LSBs of n1 coefficient for DRC first-order high-pass filter
18	0111 1111	8 MSBs of d1 coefficient for DRC first-order high-pass filter
19	1110 1111	8 LSBs of d1 coefficient for DRC first-order high-pass filter
20	0000 0000	8 MSBs of n0 coefficient for DRC first-order low-pass filter
21	0001 0001	8 LSBs of n0 coefficient for DRC first-order low-pass filter
22	0000 0000	8 MSBs of n1 coefficient for DRC first-order low-pass filter
23	0001 0001	8 LSBs of n1 coefficient for DRC first-order low-pass filter
24	0111 1111	8 MSBs of d1 coefficient for DRC first-order low-pass filter
25	1101 1110	8 LSBs of d1 coefficient for DRC first-order low-pass filter
26–127	0000 0000	Reserved