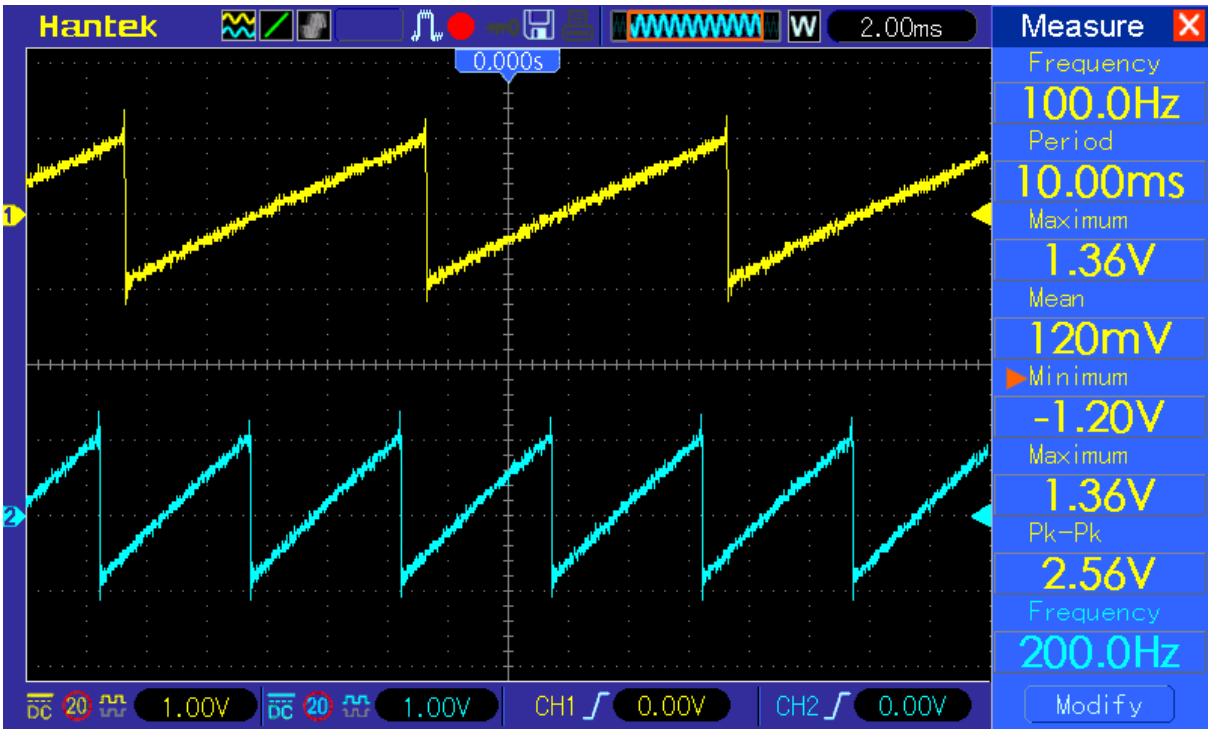
I2S Source Signals

For all tests the following signals were sent via I2S.



Yellow signal : DACL : 100Hz ascending saw signal
Blue signal : DACR : faster 200Hz ascending saw signal

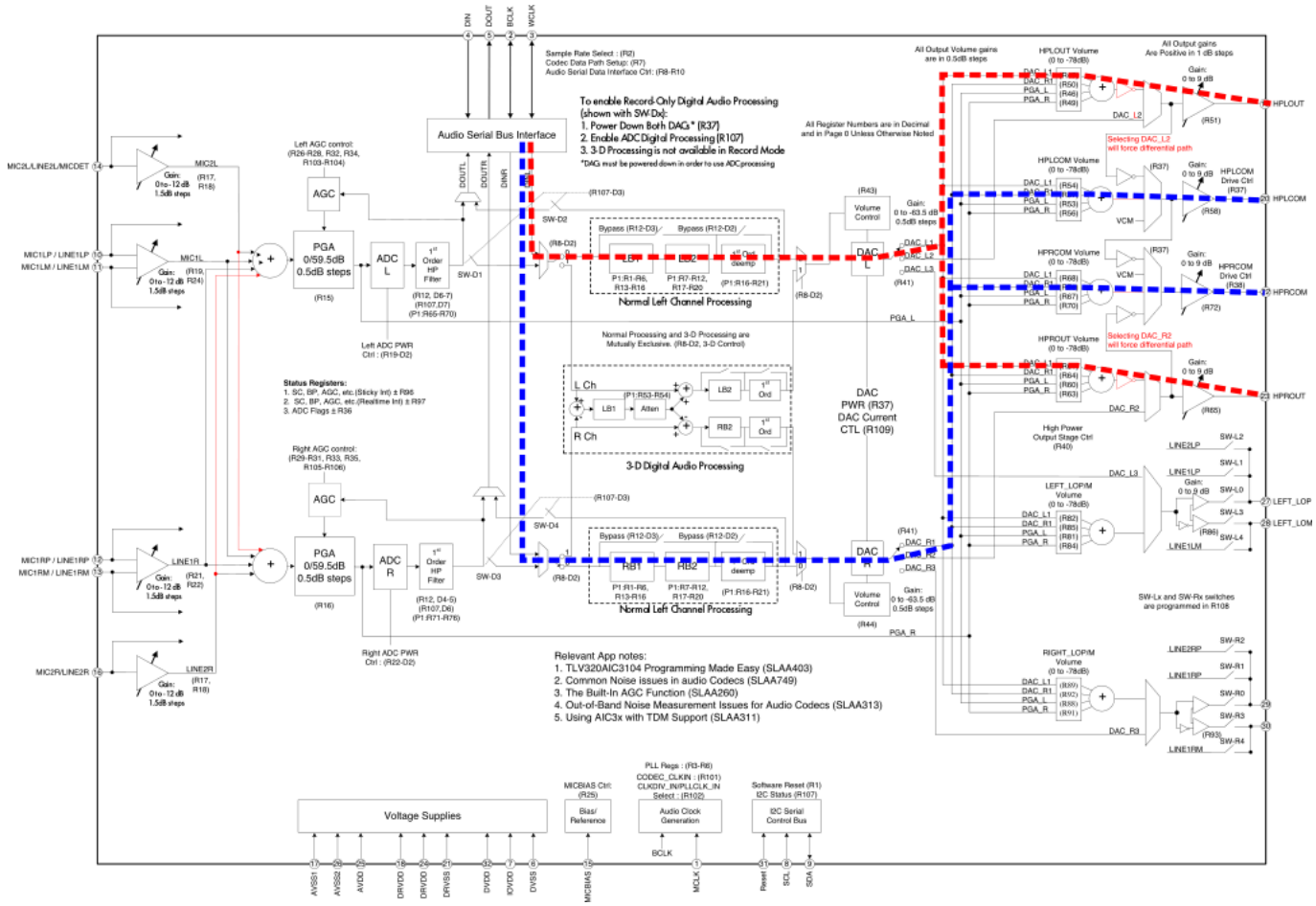
Signals are generated by the following code, where BLOC size is 20ms.

```
for (int i = 0; i < SAMPLES_PER_BLOCK; i = i + 2) {
    tx_mem_block[i] = INT16_MIN + ((INT16_MAX - INT16_MIN) / SAMPLES_PER_BLOCK) * ((i * 2) % SAMPLES_PER_BLOCK);
    tx_mem_block[i + 1] = INT16_MIN + ((INT16_MAX - INT16_MIN) / SAMPLES_PER_BLOCK) * ((i * 4) % SAMPLES_PER_BLOCK);
}
```

All tests are performed after a hardware chip reset, so unless noted, registers are left as their default post-reset state.

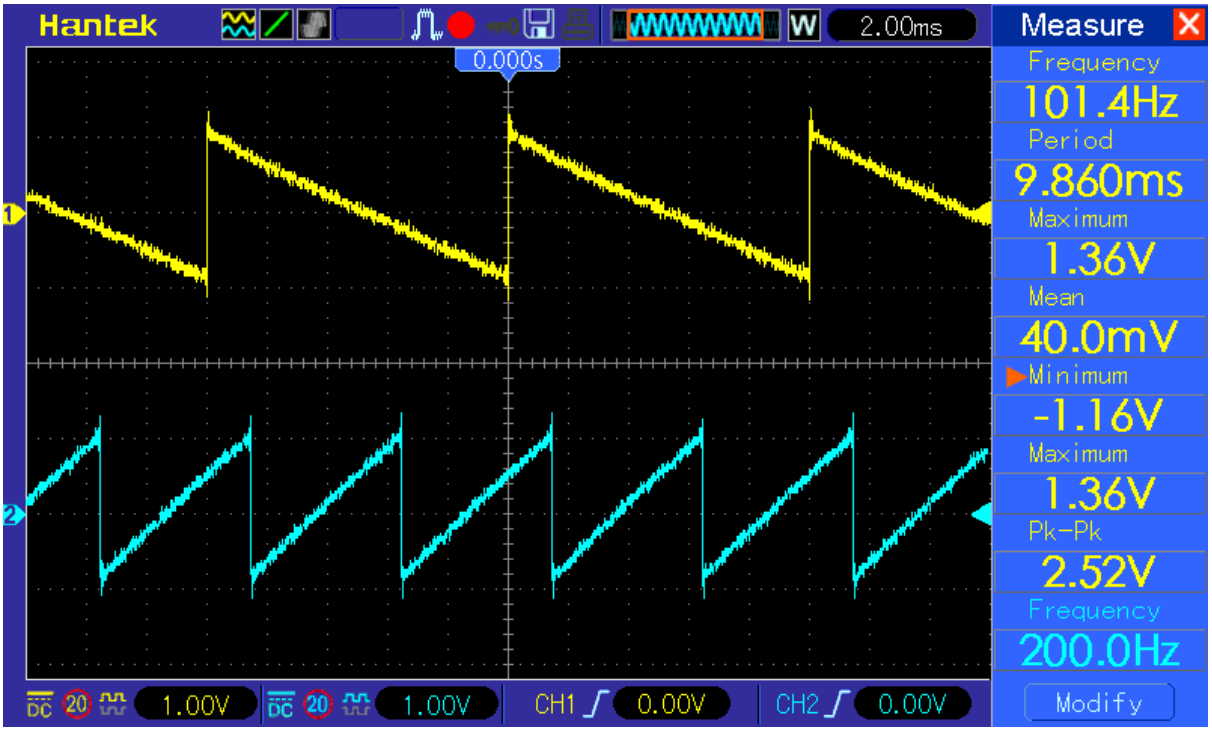
TEST1

Path R1/L1, everything single-ended
Mix DACL1 -> HPLOUT, DACL1 -> HPROUT
Mix DACR1 -> HPLCOM, DACR1 -> HPRCOM

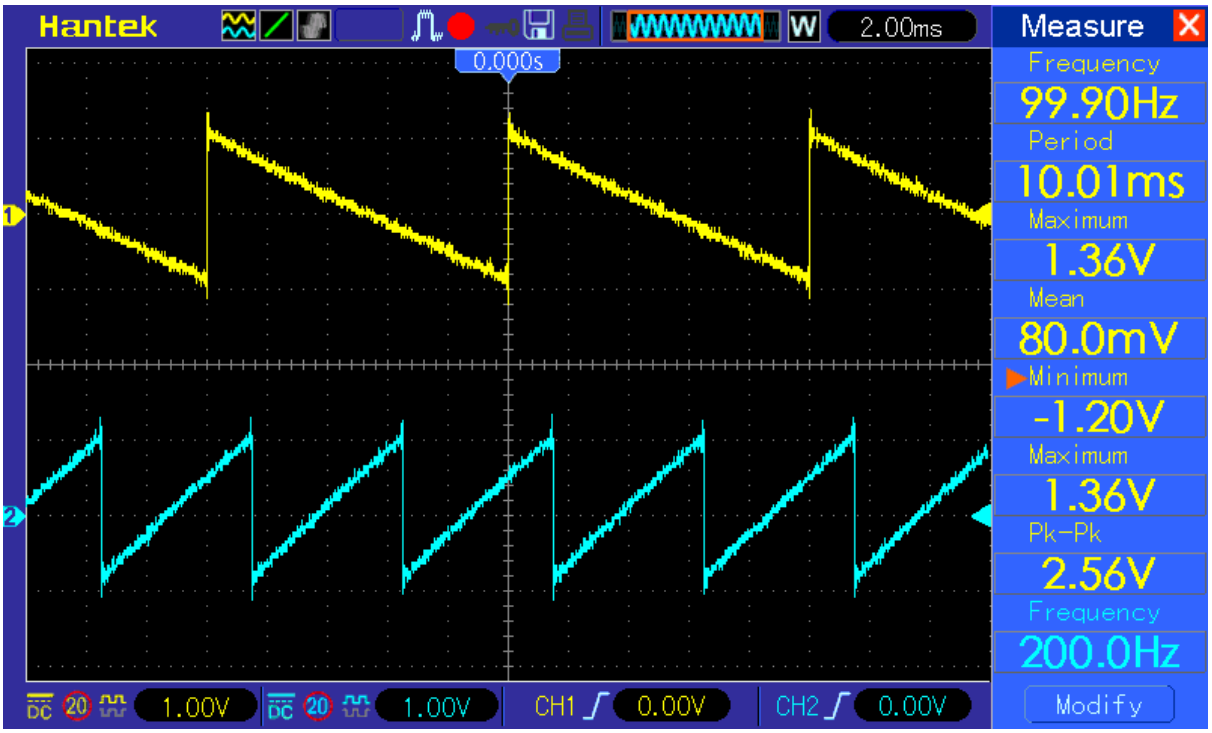


[00:00:00.895,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:102 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:101 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:02 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:07 VAL:0x0a
[00:00:00.948,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:08 VAL:0x00
[00:00:00.949,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:09 VAL:0x00
[00:00:01.000,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:41 VAL:0x00
[00:00:01.000,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:37 VAL:0xe0
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:38 VAL:0x14
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:47 VAL:0x80
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:57 VAL:0x80
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:61 VAL:0x80
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:71 VAL:0x80
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:43 VAL:0x00
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:44 VAL:0x00
[00:00:01.006,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:42 VAL:0x00
[00:00:01.006,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:40 VAL:0x41
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:14 VAL:0x80
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:51 VAL:0x09
[00:00:01.012,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:58 VAL:0x09
[00:00:01.013,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:72 VAL:0x09
[00:00:01.014,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:65 VAL:0x09

Mixers



Yellow signal : HPLOUT
Blue signal : HPLCOM



Yellow signal : HPROUT
Blue signal : HPRCOM

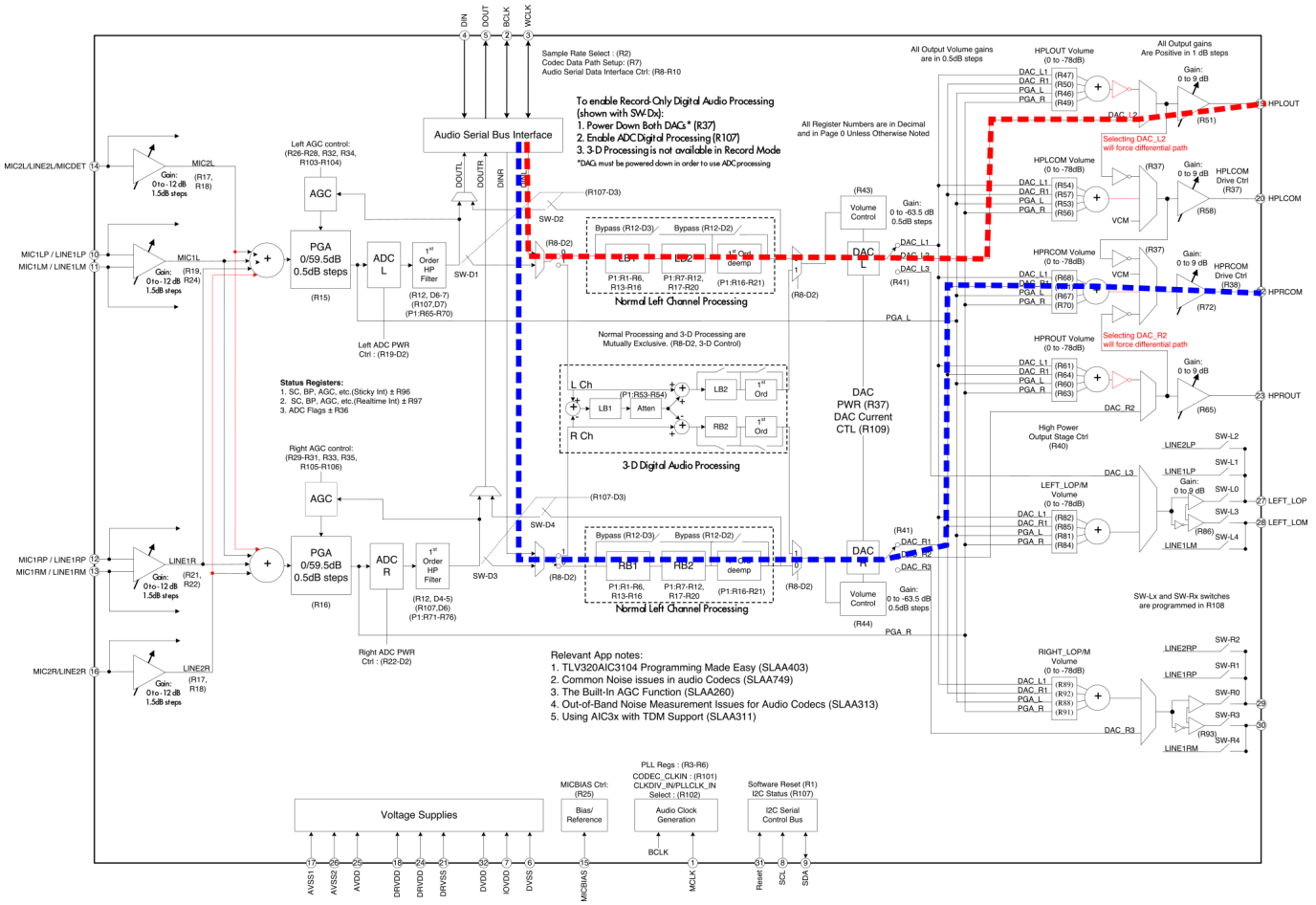
FINDINGS :
Signal is inverted on HPLOUT and HPROUT
Suggests INVERTERS after HPLOUT and HPROUT mixers
Suggests NO INVERTERS after HPLCOM and HPRCOM mixers

TEST2

Path R2/L1 path, everything single-ended

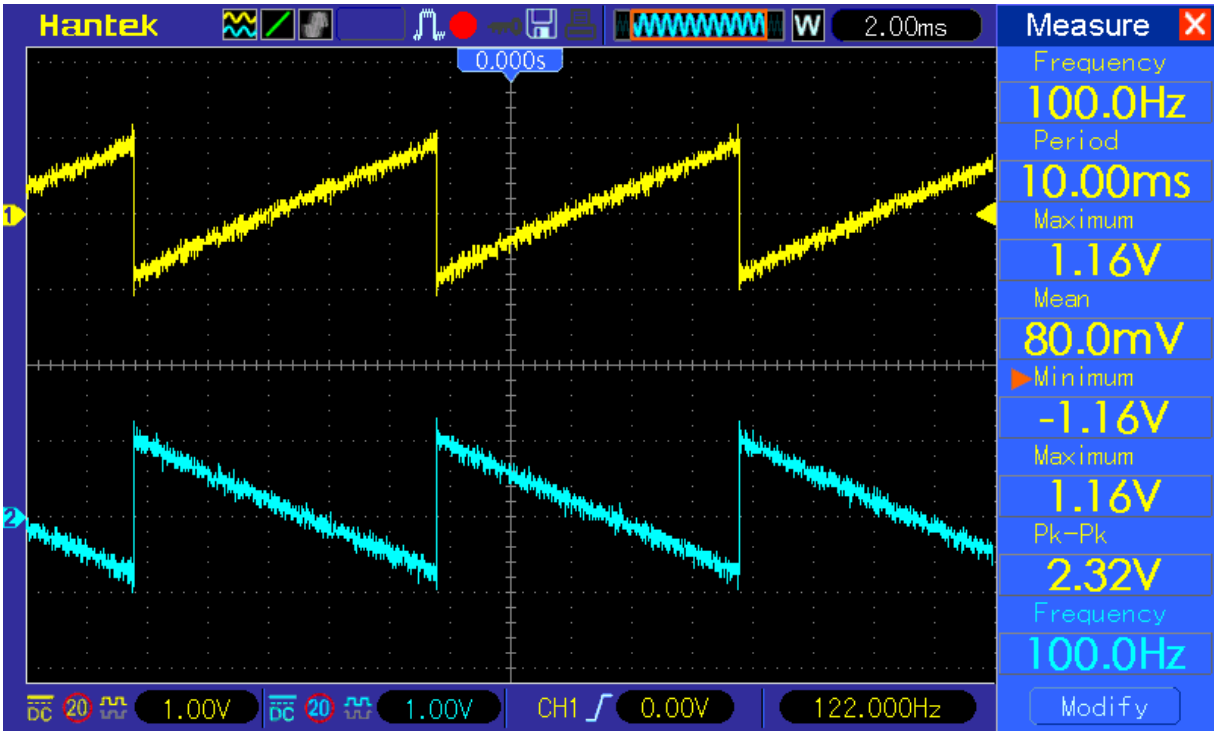
Mix 0 -> HPLOUT, 0 -> HPROUT

Mix 0 -> HPLCOM, DACR -> HPRCOM

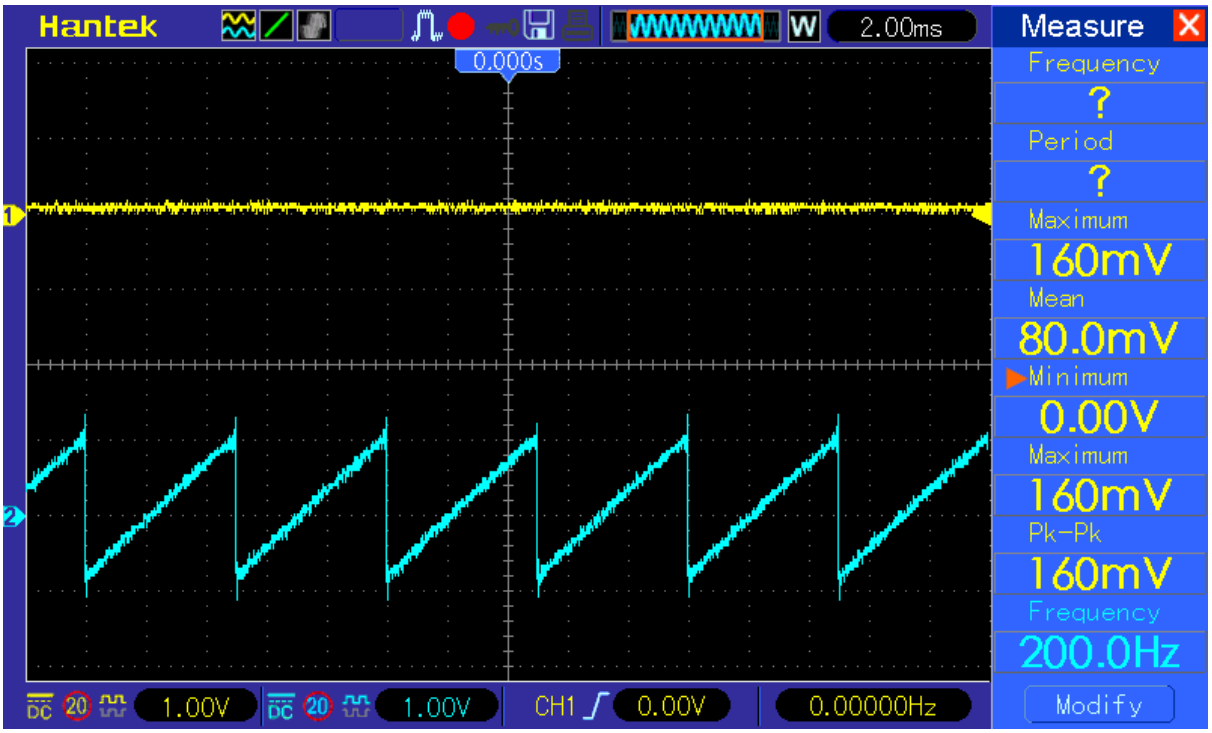


[00:00:00.895,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:102 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:101 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:02 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:07 VAL:0x0a
[00:00:00.948,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:08 VAL:0x00
[00:00:00.949,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:09 VAL:0x00
[00:00:00.999,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:41 VAL:0x80
[00:00:01.000,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:37 VAL:0xe0
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:38 VAL:0x14
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:71 VAL:0x80
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:43 VAL:0x00
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:44 VAL:0x00
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:42 VAL:0x00
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:40 VAL:0x41
[00:00:01.006,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:14 VAL:0x80
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:51 VAL:0x09
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:58 VAL:0x09
[00:00:01.013,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:72 VAL:0x09
[00:00:01.014,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:65 VAL:0x09

REG 47, 57 and 61 left as default



Yellow signal : HPLOUT
Blue signal : HPLCOM

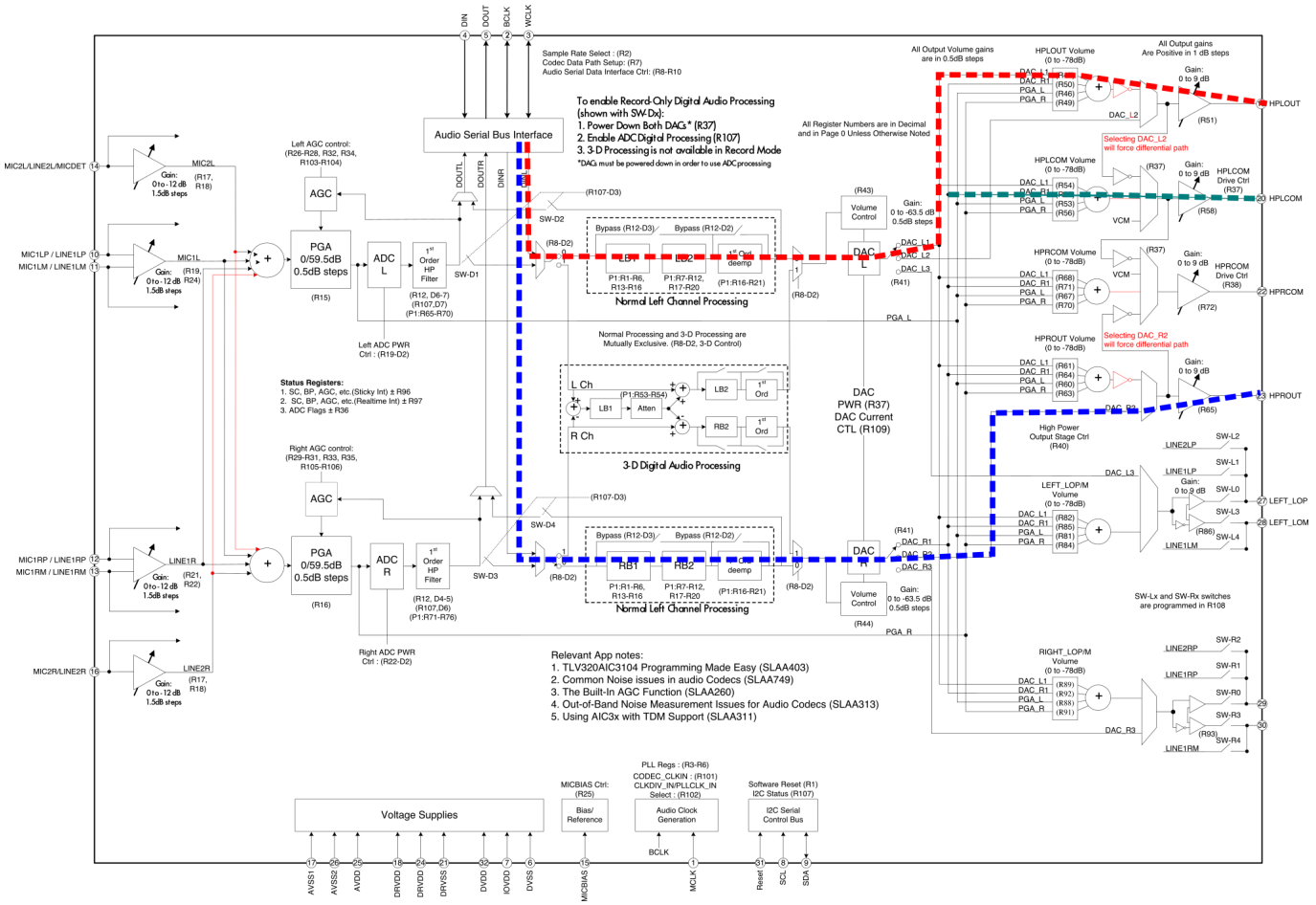


Yellow signal : HPROUT
Blue signal : HPRCOM

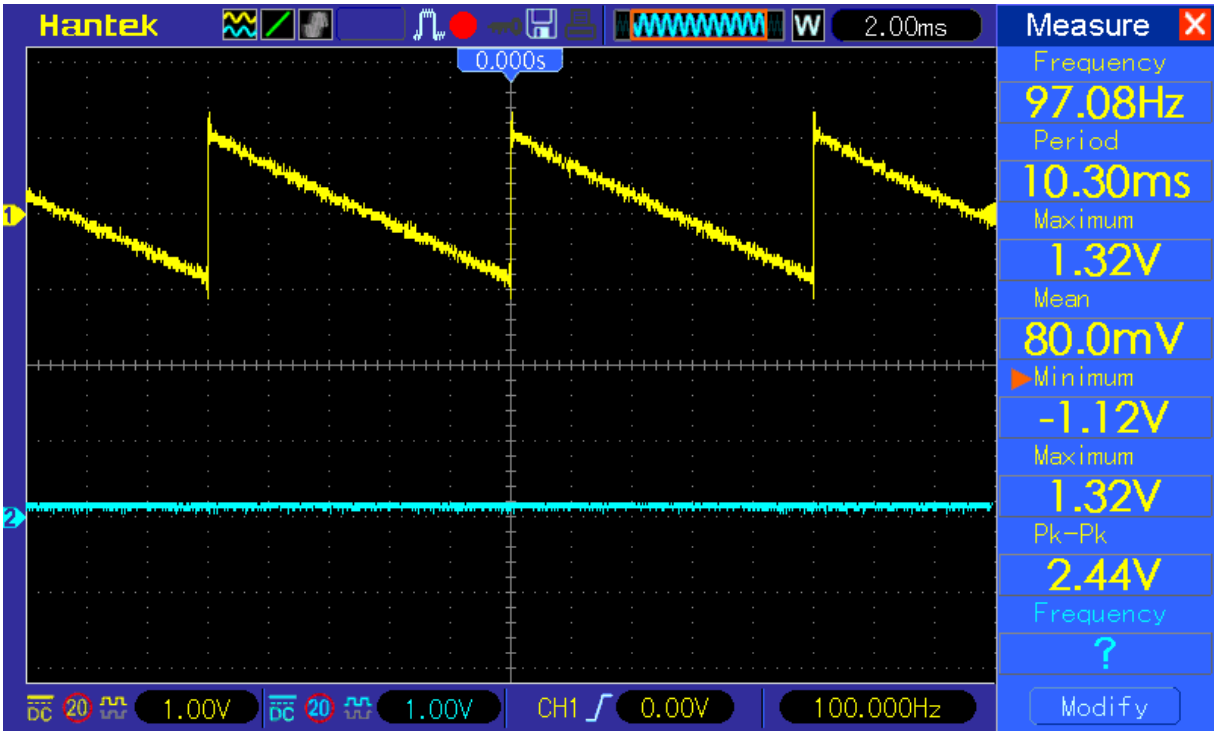
FINDINGS :
When using the L2 path, the signal is **no longer** inverted on HPLOUT, **HPLCOM shows inverted HPLOUT**, despite the fact that normally nothing is routed to it.
No signals on HPROUT.
HPRCOM unchanged.
More noise thru L2 path than L1, which was expected according to the datasheet.
Suggest choosing L2 path forces HPLCOM differential, overriding single ended mode
The inverter on HPLOUT path is located just after the mixer, since L2 path not affected

TEST3

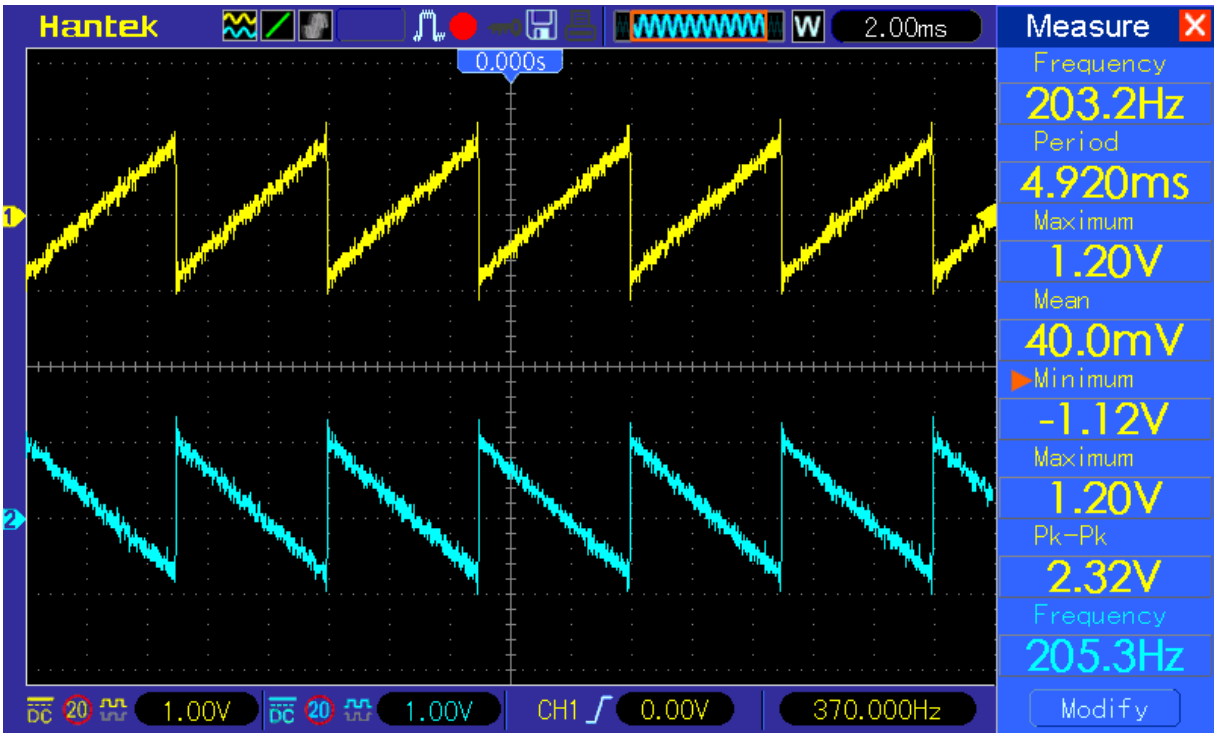
Path R1/L2 path, everything single-ended
DACL -> HPLOUT, 0 -> HPROUT
DACR1 -> HPLCOM, 0 -> HPRCOM



[00:00:00.895,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:102 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:101 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:02 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:07 VAL:0x0a
[00:00:00.948,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:08 VAL:0x00
[00:00:00.949,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:09 VAL:0x00
[00:00:00.999,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:41 VAL:0x20
[00:00:01.000,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:37 VAL:0xe0
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:38 VAL:0x14
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:47 VAL:0x80
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:57 VAL:0x80
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:43 VAL:0x00
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:44 VAL:0x00
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:42 VAL:0x00
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:40 VAL:0x41
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:14 VAL:0x80
[00:00:01.006,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:51 VAL:0x09
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:58 VAL:0x09
[00:00:01.017,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:72 VAL:0x09
[00:00:01.018,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:65 VAL:0x09
REG 61 and 71 left as default



Yellow signal : HPLOUT
Blue signal : HPLCOM

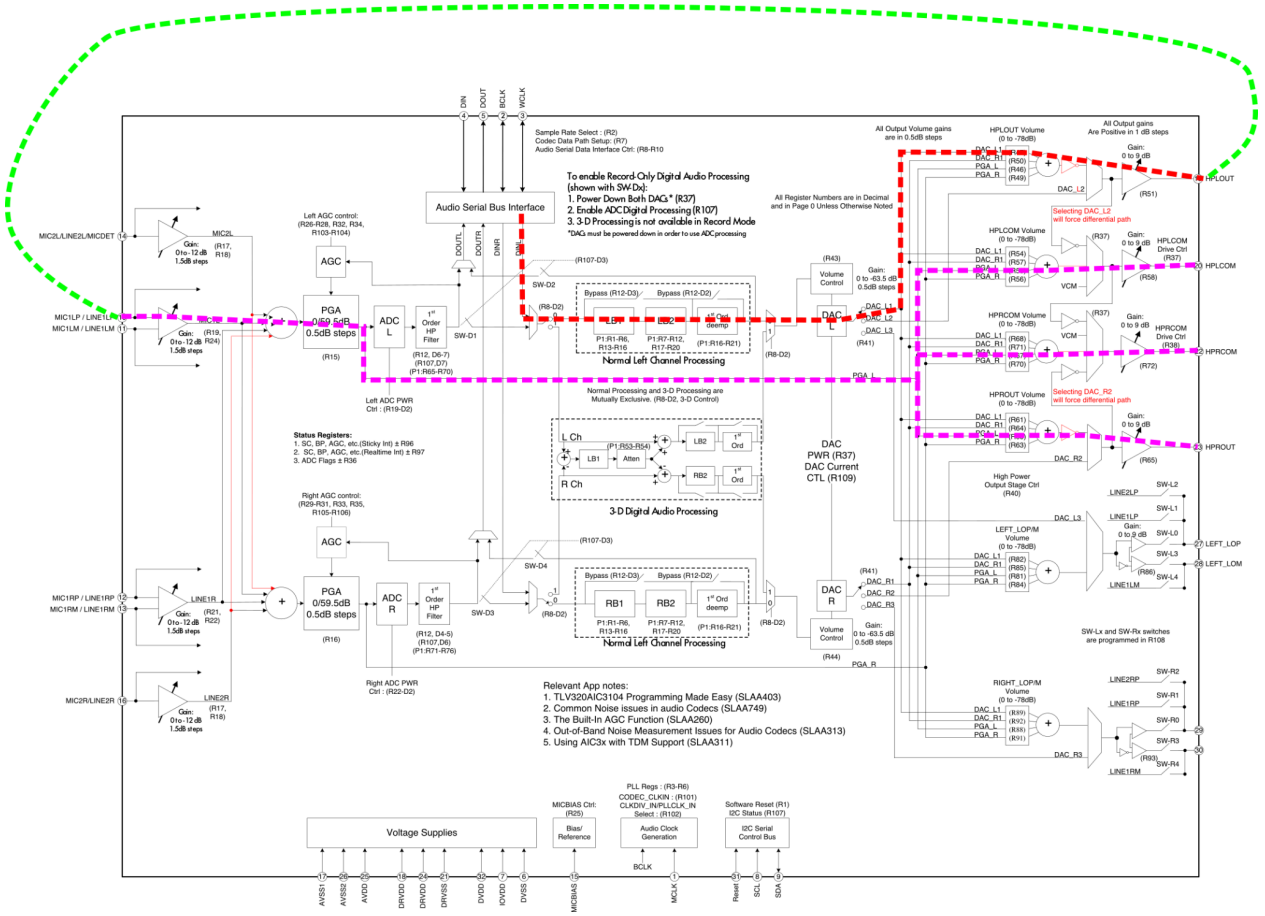


Yellow signal : HPROUT
Blue signal : HPRCOM

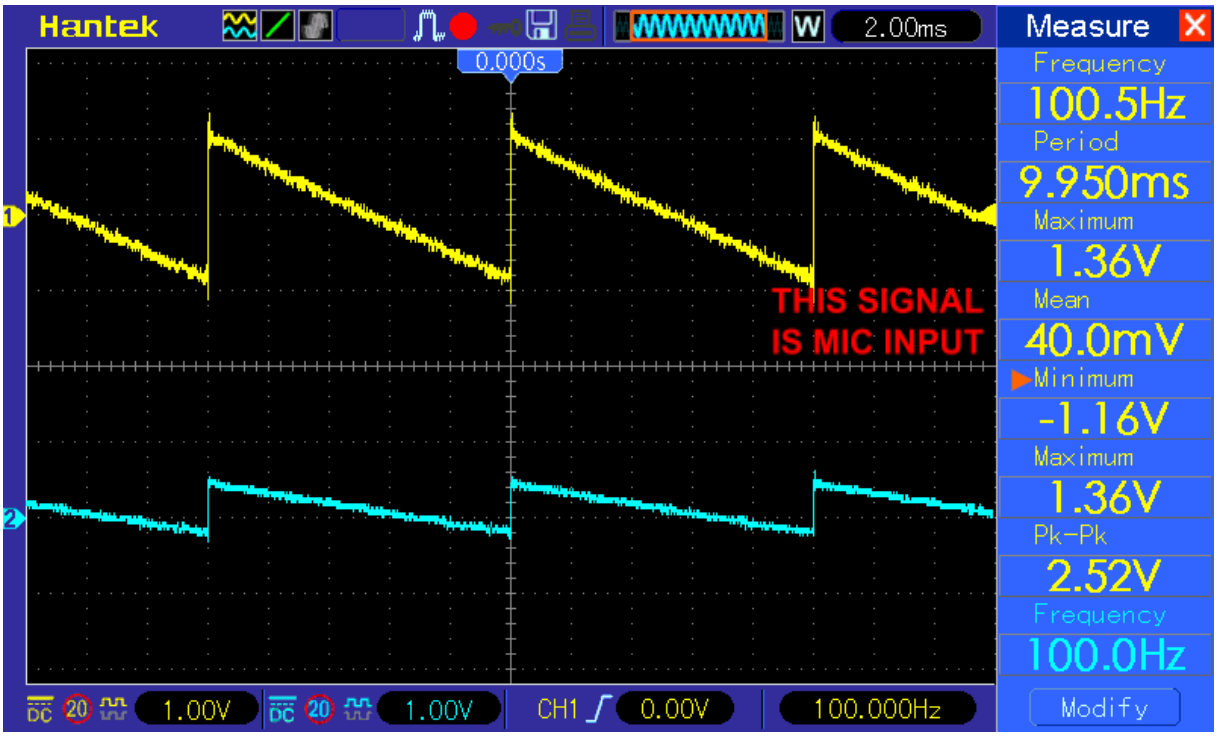
FINDINGS :
When using the R2 path, the signal is **no longer** inverted on HPROUT, **HPRCOM shows inverted HPROUT**, despite the fact that normally nothing is routed to it.
No signals on HPLCOM as expected as DAC_R1 is no longer available to the mixer.
HPLOUT unchanged (still inverted).
More noise thru R2 path than R1, which was expected according to the datasheet.
Suggest choosing R2 path forces HPRCOM differential, override single ended mode, similar behavior to L2 path on HPL

TEST4

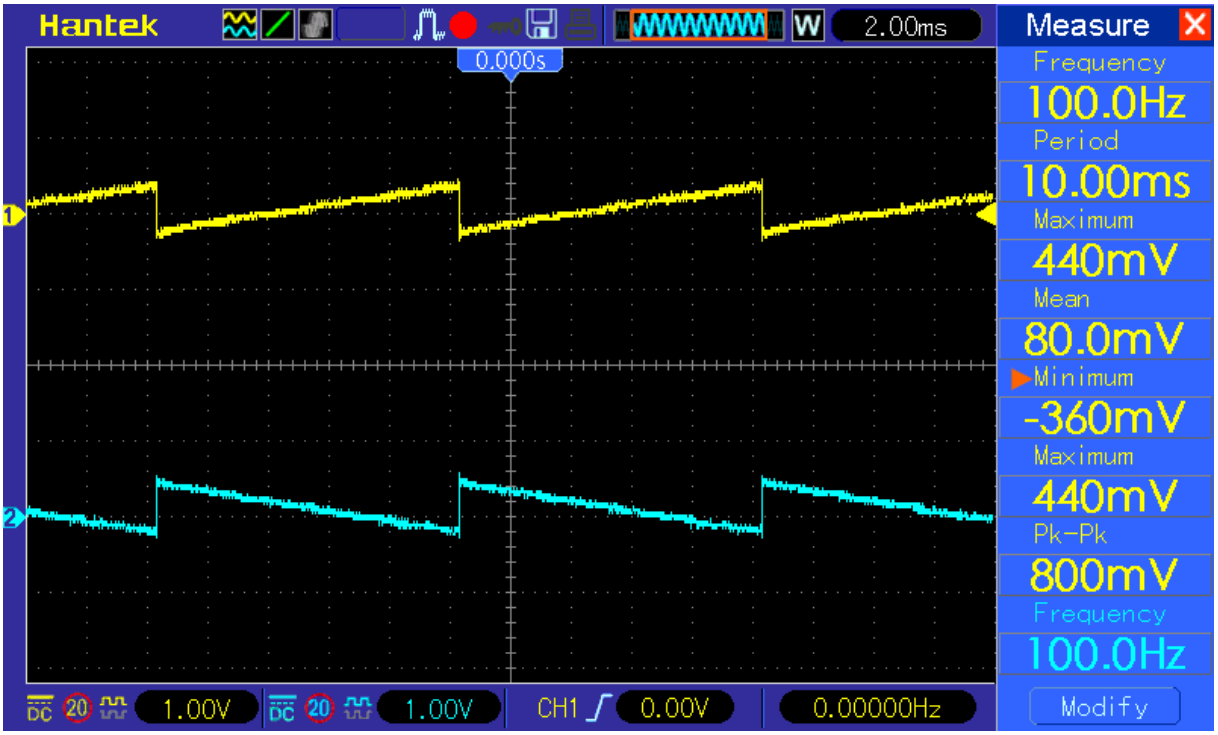
Path R1/L1 path, everything single-ended
DACL -> HPLOUT, PGAL -> HPROUT
PGAL -> HPLCOM, PGAL -> HPRCOM
External wiring of HPLOUT to MIC1LP. MIC1LP in single ended mode



[00:00:00.895,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:102 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:101 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:02 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:07 VAL:0x0a
[00:00:00.948,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:08 VAL:0x00
[00:00:00.949,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:09 VAL:0x00
[00:00:00.999,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:41 VAL:0x00
[00:00:01.000,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:37 VAL:0xe0
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:38 VAL:0x14
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:47 VAL:0x80
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:15 VAL:0x00
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:19 VAL:0x80
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:53 VAL:0x80
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:60 VAL:0x80
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:67 VAL:0x80
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:43 VAL:0x00
[00:00:01.006,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:44 VAL:0x00
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:42 VAL:0x00
[00:00:01.013,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:40 VAL:0x41
[00:00:01.013,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:14 VAL:0x80
[00:00:01.014,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:51 VAL:0x09
[00:00:01.015,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:58 VAL:0x09
[00:00:01.015,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:72 VAL:0x09
[00:00:01.016,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:65 VAL:0x09
REG 57, 61 and 71 left as default



Yellow signal : HPLOUT
Blue signal : HPLCOM



Yellow signal : HPROUT
Blue signal : HPRCOM

FINDINGS :
HPLOUT still inverted (in line with TEST1)
HPLCOM & HPLCOM, are inverted too, following HPLOUT (-> **no additional inversion** in PGA/HPLCOM path)
HPROUT, is not inverted, which suggest an additional inversion on HPROUT, which is in line with TEST1
Signal is divided by 2 in terms of amplitude when going thru the MIC1 path, which is probably linked to the fact that MIC1LP is used as single ended, so in fact, differential to VCM.
Suggest inverters on HPLOUT/HPROUT mixers, no inverters on HPROUT/HPLOUT (similar to TEST1). No inversion on PGAL path
Additional note : a quick test with same inputs but using PGAR path instead PGAL showed identical results

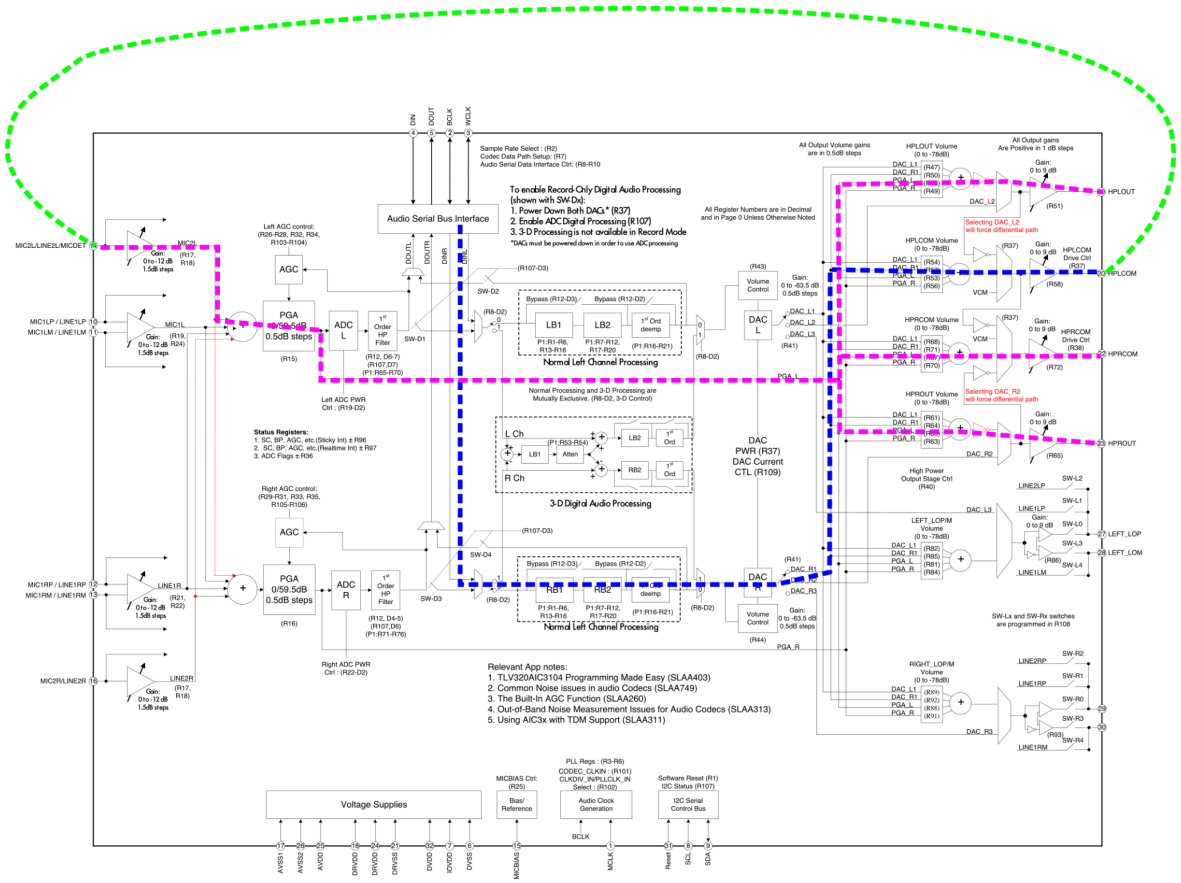
TEST5

Path R1/L1 path, everything single-ended

PGAL -> HPLOUT, PGAL -> HPROUT

DACR -> HPLCOM, PGAL -> HPRCOM

External wiring of HPLCOM to MIC2L



[00:00:00.895,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:102 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:101 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:02 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:07 VAL:0x0a
[00:00:00.948,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:08 VAL:0x00
[00:00:00.949,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:09 VAL:0x00
[00:00:00.999,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:41 VAL:0x00
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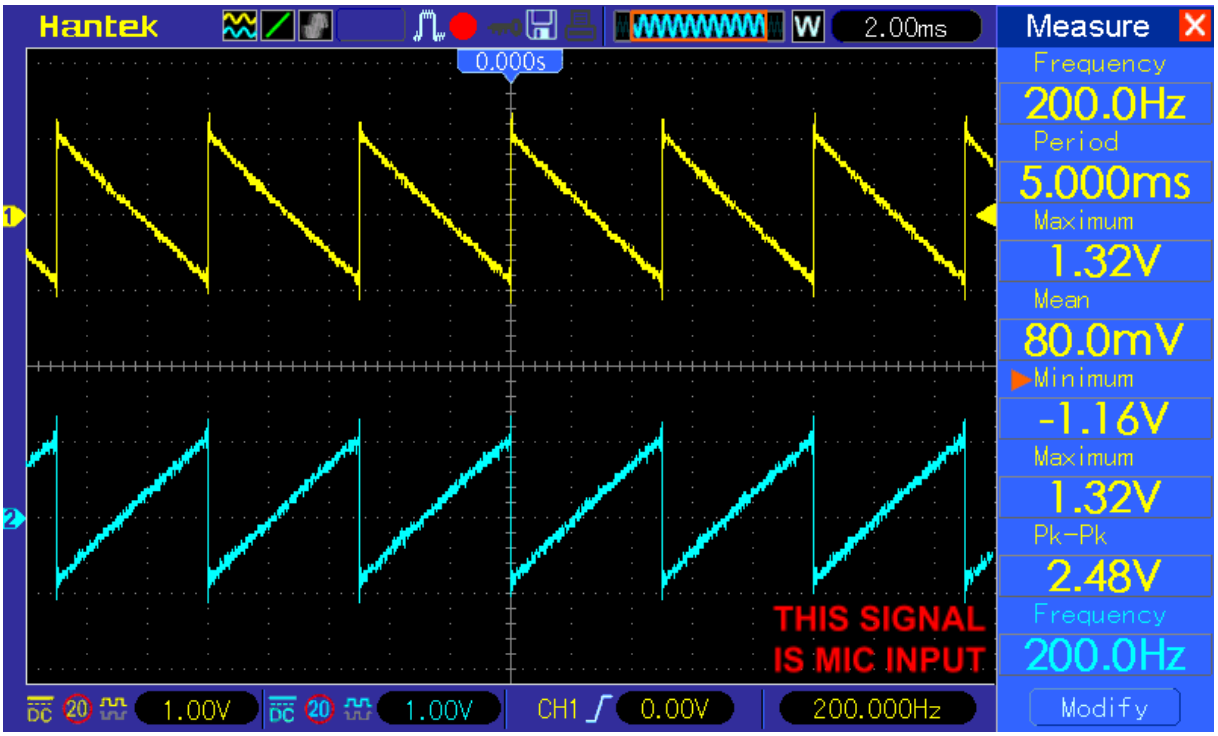
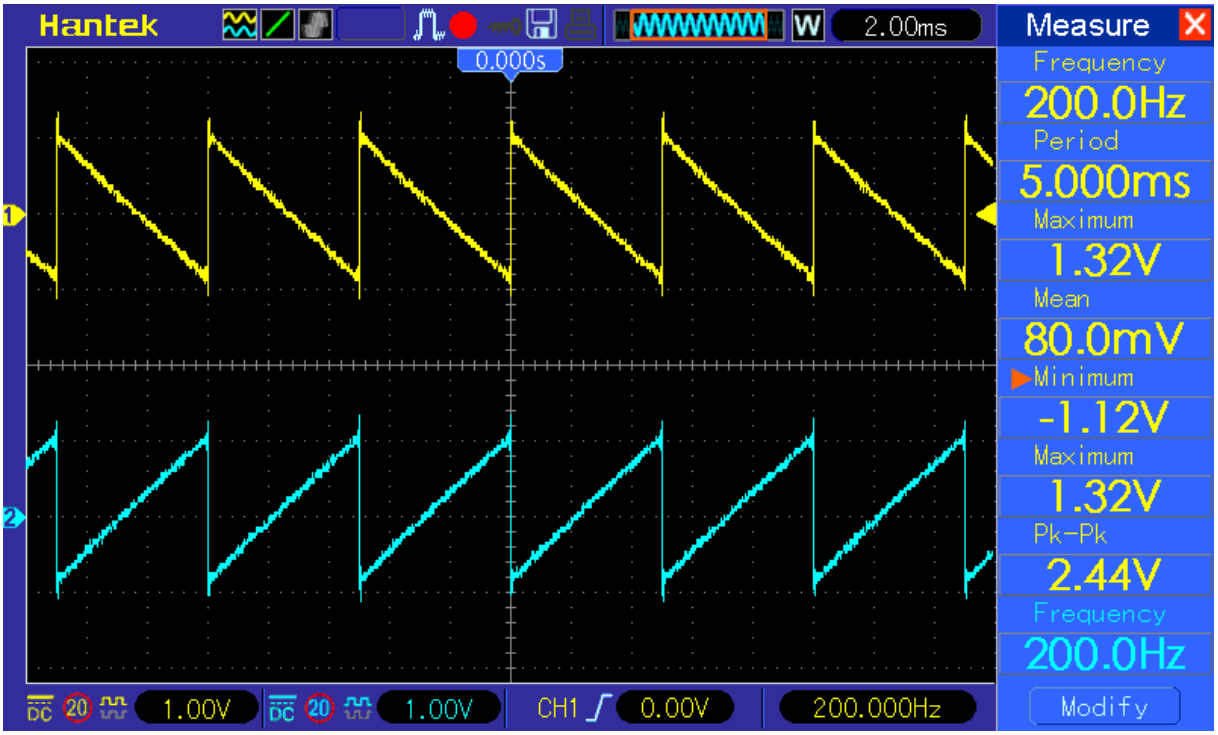
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:38 VAL:0x14
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:57 VAL:0x80
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:15 VAL:0x00
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:17 VAL:0x0f
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:46 VAL:0x80
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:60 VAL:0x80
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:67 VAL:0x80
[00:00:01.006,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:43 VAL:0x00
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:44 VAL:0x00
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:42 VAL:0x00
[00:00:01.023,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:40 VAL:0x41
[00:00:01.024,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:14 VAL:0x80
[00:00:01.024,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:51 VAL:0x09
[00:00:01.025,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:58 VAL:0x09
[00:00:01.026,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:72 VAL:0x09
[00:00:01.026,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:65 VAL:0x09

REG 47, 61 and 71 left as default



Yellow signal : HPLOUT
Blue signal : HPLCOM



Yellow signal : HPROUT
Blue signal : HPRCOM

FINDINGS :
HPRCOM is normal (in line with TEST1). HPLCOM, is normal, following HPRCOM
HPLOUT and HPROUT, are both inverted, which is in line with TEST1
Signal full amplitude when going thru the MIC2 path.
In line with all previous conclusions

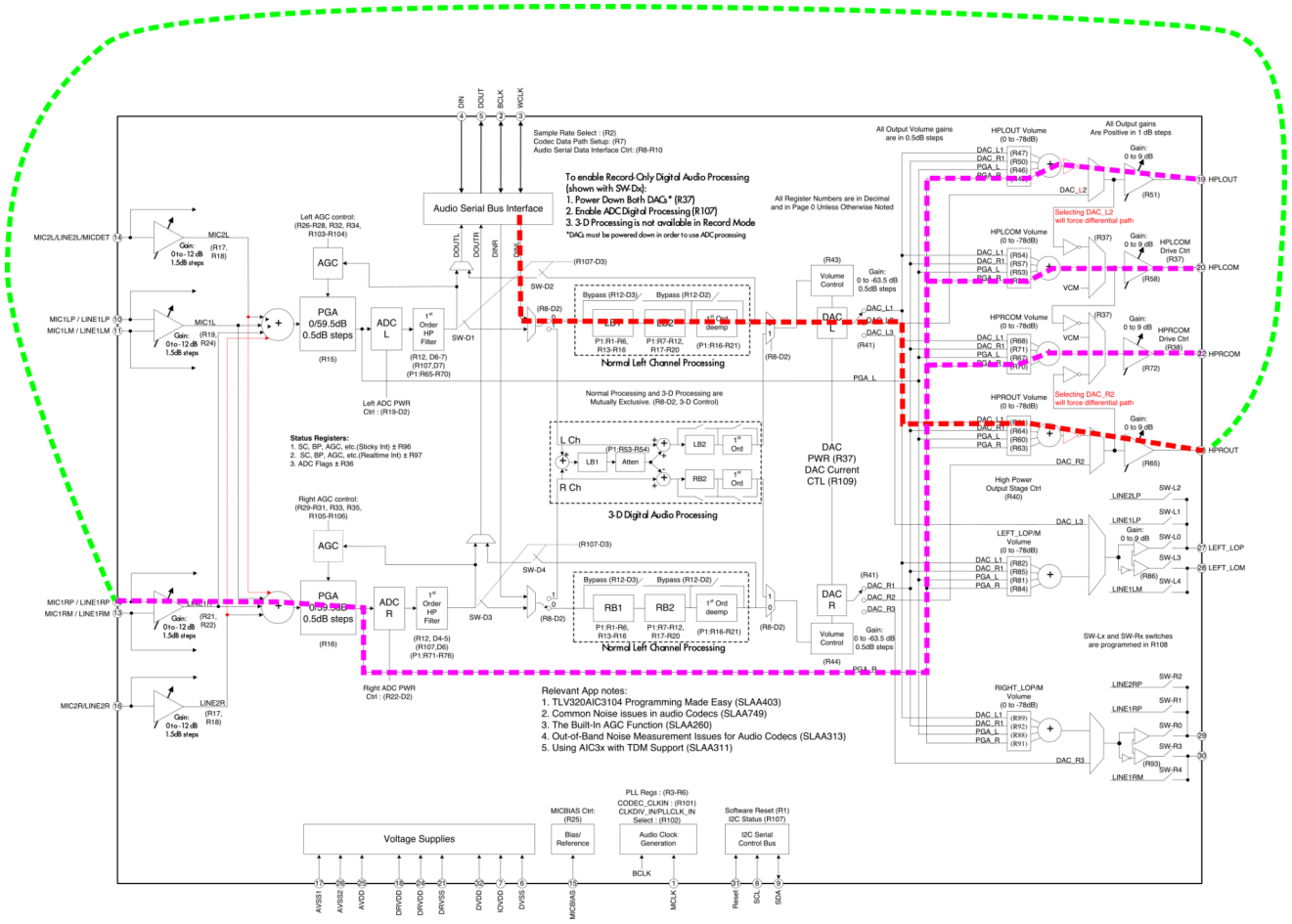
TEST6

Path R1/L1 path, everything single-ended

PGAR -> HPLOUT, DACL -> HPROUT

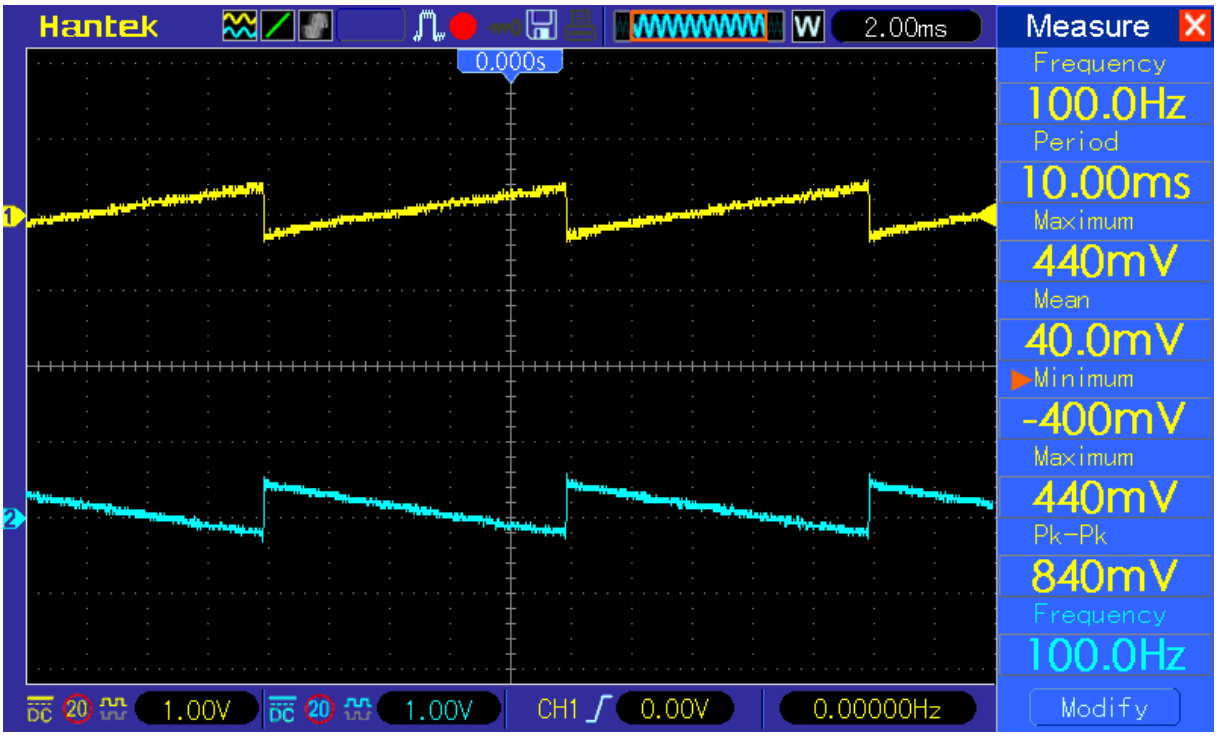
PGAR -> HPLCOM, PGAR -> HPRCOM

External wiring of HPROUT to MIC1RP. MIC1RP in single ended mode

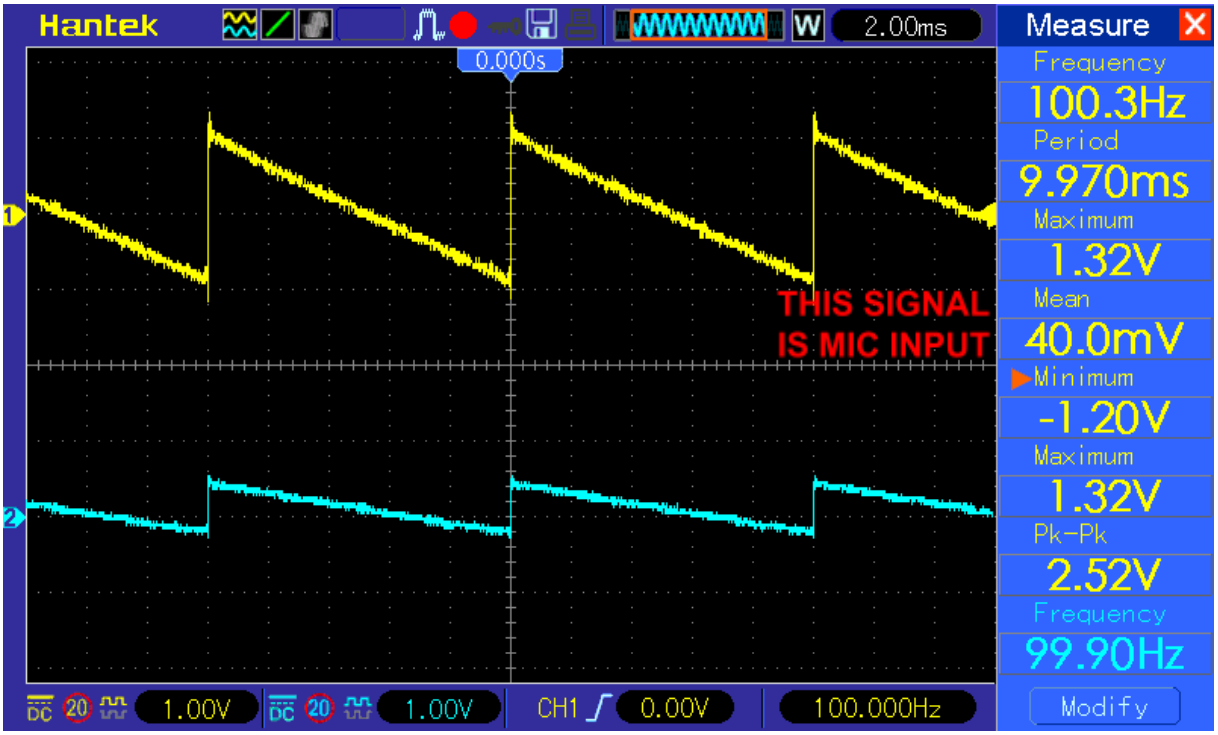


[00:00:00.895,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:102 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:101 VAL:0x00
[00:00:00.896,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:02 VAL:0x00
[00:00:00.897,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:07 VAL:0x0a
[00:00:00.948,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:08 VAL:0x00
[00:00:00.949,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:09 VAL:0x00
[00:00:00.999,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:41 VAL:0x00
[00:00:01.000,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:37 VAL:0xe0
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:38 VAL:0x14
[00:00:01.001,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:61 VAL:0x80
[00:00:01.002,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:16 VAL:0x00
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:22 VAL:0x80
[00:00:01.003,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:49 VAL:0x80
[00:00:01.004,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:56 VAL:0x80
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:70 VAL:0x80
[00:00:01.005,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:43 VAL:0x00
[00:00:01.006,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:44 VAL:0x00
[00:00:01.007,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:42 VAL:0x00
[00:00:01.017,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:40 VAL:0x41
[00:00:01.018,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:14 VAL:0x80
[00:00:01.019,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:51 VAL:0x09
[00:00:01.019,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:58 VAL:0x09
[00:00:01.020,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:72 VAL:0x09
[00:00:01.021,000] <dbg> tlv320aic310x: codec_write_reg: WR 0 PG:0 REG:65 VAL:0x09

REG 47, 57 and 71 left as default



Yellow signal : HPLOUT
Blue signal : HPLCOM

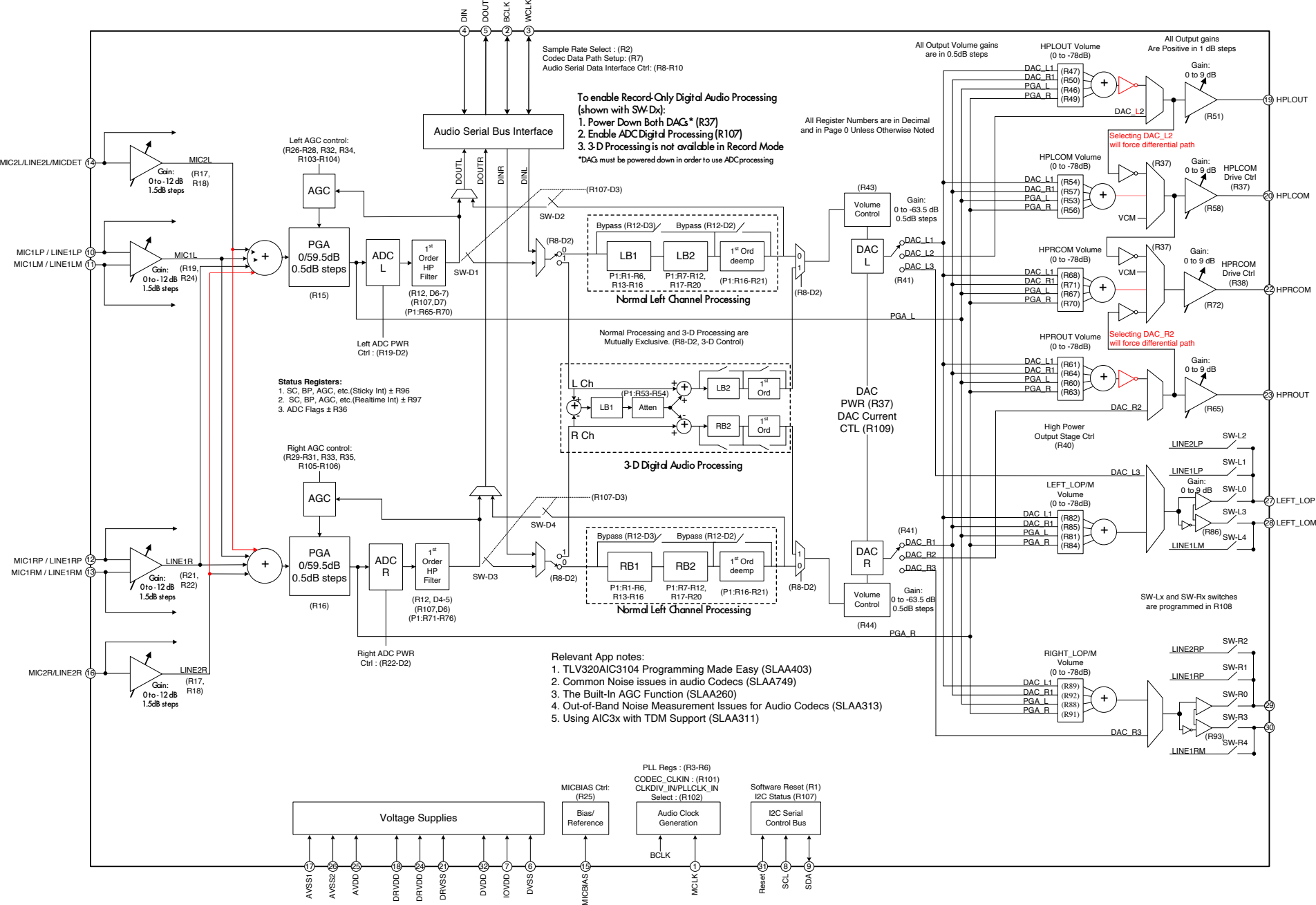


Yellow signal : HPROUT
Blue signal : HPRCOM

FINDINGS :
HPROUT, inverted as always in line with TEST1
HPRCOM and HPLCOM, both also inverted are following HPROUT, so again no additional inversion on PGAR path
HPLOUT is not inverted though, being inverted again from MIC input. (ie DAC -invert-> HPROUT -> PGA -invert-> HPLOUT)
In line with all previous conclusions

CORRECTED DATASHEET

Found on the next page, red is showing corrections.


DIN
DOUT
BCLK
WCLK
Sample Rate Select : (R2)
Codec Data Path Setup: (R7)
Audio Serial Data Interface Ctrl: (R8-R10
Audio Serial Bus Interface
DOUTL
DOUTR
DINR
DINL
To enable Record-Only Digital Audio Processing (shown with SW-Dx):
1. Power Down Both DACs* (R37)
2. Enable ADC Digital Processing (R107)
3. 3-D Processing is not available in Record Mode
*DACs must be powered down in order to use ADC processing
All Register Numbers are in Decimal and in Page 0 Unless Otherwise Noted
All Output Volume gains are in 0.5dB steps
All Output gains Are Positive in 1 dB steps
HPLOUT Volume (0 to -78dB)
Gain: 0 to 9 dB
(R51)
HPLOUT
DAC_L1
DAC_R1
PGA_L
PGA_R
(R47)
(R50)
(R46)
(R49)
DAC_L2
Selecting DAC_L2 will force differential path
HPLCOM Volume (0 to -78dB)
HPLCOM Drive Ctrl (R37)
(R37)
(R54)
(R57)
(R53)
(R56)
VCM
(R58)
HPLCOM
HPRCOM Volume (0 to -78dB)
HPRCOM Drive Ctrl (R38)
(R68)
(R71)
(R67)
(R70)
(R72)
HPRCOM
Selecting DAC_R2 will force differential path
HPROUT Volume (0 to -78dB)
(R61)
(R64)
(R60)
(R63)
DAC_R2
(R65)
HPROUT
High Power Output Stage Ctrl (R40)
LEFT_LOP/M Volume (0 to -78dB)
(R82)
(R85)
(R81)
(R84)
(R86)
LINE2LP
LINE1LP
LINE1LM
SW-L2
SW-L1
SW-L0
SW-L3
SW-L4
LEFT_LOP
LEFT_LOM
RIGHT_LOP/M Volume (0 to -78dB)
(R89)
(R92)
(R88)
(R91)
(R93)
LINE2RP
LINE1RP
LINE1RM
SW-R2
SW-R1
SW-R0
SW-R3
SW-R4
SW-Lx and SW-Rx switches are programmed in R108
MIC2L/LINE2L/MICDET
MIC2L
Gain: 0 to -12 dB 1.5dB steps
(R17, R18)
Left AGC control: (R26-R28, R32, R34, R103-R104)
AGC
MIC1LP / LINE1LP
MIC1LM / LINE1LM
MIC1L
(R19, R24)
PGA 0/59.5dB 0.5dB steps
(R15)
ADC L
1st Order HP Filter
(R12, D6-7) (R107,D7) (P1:R65-R70)
SW-D1
SW-D2
(R107-D3)
(R8-D2)
Bypass (R12-D3)
Bypass (R12-D2)
LB1
LB2
1st Ord deemp
P1:R1-R6, R13-R16
P1:R7-R12, R17-R20
(P1:R16-R21)
Normal Left Channel Processing
(R43)
Volume Control
Gain: 0 to -63.5 dB 0.5dB steps
DAC L
DAC_L1
DAC_L2
DAC_L3
(R41)
PGA_L
Left ADC PWR Ctrl : (R19-D2)
Normal Processing and 3-D Processing are Mutually Exclusive. (R8-D2, 3-D Control)
L Ch
R Ch
(P1:R53-R54)
LB1
Atten
LB2
RB2
1st Ord
3-D Digital Audio Processing
Status Registers:
1. SC, BP, AGC, etc.(Sticky Int) ± R96
2. SC, BP, AGC, etc.(Realtime Int) ± R97
3. ADC Flags ± R36
DAC PWR (R37) DAC Current CTL (R109)
Right AGC control: (R29-R31, R33, R35, R105-R106)
AGC
MIC1RP / LINE1RP
MIC1RM / LINE1RM
LINE1R
(R21, R22)
PGA 0/59.5dB 0.5dB steps
(R16)
ADC R
1st Order HP Filter
(R12, D4-5) (R107,D6) (P1:R71-R76)
SW-D3
SW-D4
(R107-D3)
(R8-D2)
Bypass (R12-D3)
Bypass (R12-D2)
RB1
RB2
1st Ord deemp
P1:R1-R6, R13-R16
P1:R7-R12, R17-R20
(P1:R16-R21)
Normal Left Channel Processing
(R41)
DAC_R1
DAC_R2
DAC_R3
DAC R
Volume Control
Gain: 0 to -63.5 dB 0.5dB steps
(R44)
PGA_R
Right ADC PWR Ctrl : (R22-D2)
MIC2R/LINE2R
LINE2R
(R17, R18)
Relevant App notes:
1. TLV320AIC3104 Programming Made Easy (SLAA403)
2. Common Noise issues in audio Codecs (SLAA749)
3. The Built-In AGC Function (SLAA260)
4. Out-of-Band Noise Measurement Issues for Audio Codecs (SLAA313)
5. Using AIC3x with TDM Support (SLAA311)
PLL Regs : (R3-R6)
CODEC_CLKIN : (R101)
CLKDIV_IN/PLLCLK_IN Select : (R102)
MICBIAS Ctrl: (R25)
Software Reset (R1)
I2C Status (R107)
Voltage Supplies
Bias/ Reference
Audio Clock Generation
I2C Serial Control Bus
BCLK
AVSS1
AVSS2
AVDD
DRVDD
DRVDD
DRVSS
DVDD
IOVDD
DVSS
MICBIAS
MCLK
Reset
SCL
SDA