

TLV320AIC3104 configuration from Modem EG91

Register #	Value	Configuration				
0	0x00					
1	0x00	Software Reset Bit 0 : Don't care				
2	0xAA	1010: ADC fS = fS(ref) / 6	1010: DAC fS = fS(ref) / 6			
3	0x91	1: PLL is enabled.	PLL Q Value = 2	PLL P Value = 8		
4	0xC0	PLL J Value = 48				
5	0x00	Default				
6	0x00	Default				
7	0x1E	ADC Dual-Rate Control 0: ADC dual-rate mode is disabled.	DAC Dual-Rate Control 0: DAC dual-rate mode is disabled.	11: Left-DAC data path plays mono mix of left- and right-channel input data.	11: Right-DAC data path plays mono mix of left- and right-channel input data.	
8	0x00	Default				
9	0x40	Audio Serial Data Interface Transfer Mode 01: Serial data bus uses DSP mode.	Audio Serial Data Word Length Control 00: Audio data word length = 16 bits	Bit Clock Rate Control This register only has effect when bit clock is programmed as an output. 0: Continuous-transfer mode used to determine master mode bit clock rate	DAC Re-Sync 0: Don't care ADC Re-Sync 0: Don't care	Re-Sync Mute Behavior 0: Re-sync is done without soft-muting the channel (ADC / DAC).
10	0x01	Audio Serial Data Word Offset Control 0000 0001: Data offset = 1 bit clock				
11	0x01	Default				
12	0x5F	Left-ADC High-Pass Filter Control 01: Left-ADC high-pass filter -3-dB frequency = 0.0045 × ADC f _S	Right-ADC High-Pass Filter Control 01: Right-ADC high-pass filter -3-dB frequency = 0.0045 × ADC f _S	1: Left-DAC digital effects filter enabled 1: Left-DAC de-emphasis filter enabled	1: Right-DAC digital effects filter enabled 1: Right-DAC de-emphasis filter enabled	
13	0x00	Default				
14	0x00	Default				
15	0x50	0: The left-ADC PGA is not muted	Left-ADC PGA Gain Setting = 80			
16	0x50	0: The Right-ADC PGA is not muted	Right-ADC PGA Gain Setting = 80			
17	0xFF	Default				
18	0xFF	Default				
19	0x04	1: Left-ADC channel is powered up.				
20	0x78	Default				
21	0x00	Default				
22	0x00	Default				
23	0x78	Default				

Register #	Value	Configuration				
24	0x00	Default				
25	0x86	10: MICBIAS output is powered to 2.5 V.				
26	0x00	Default				
27	0xFE	Default	Left-AGC Maximum Gain Allowed: 1110 111–111 111: Maximum gain = 59.5 dB			
28	0x00	Default				
29	0x00	Default				
30	0xFE	Default	Right-AGC Maximum Gain Allowed: 1110 111–111 111: Maximum gain = 59.5 dB			
31	0x00	Default				
32	0x00	Default				
33	0x00	Default				
34	0x00	Default				
35	0x00	Default				
36	0x44	1: Left ADC is in a power-up state.	1: Right ADC is in a power-up state.			
37	0xC0	1: Left DAC is powered up.	1: Right DAC is powered up.	00: HPLCOM configured as differential of HPLOUT		
38	0x00	Default				
39	0x00	Default				
40	0xC0	11: Output common-mode voltage = 1.8 V	00: Output soft-stepping = one step per sample period			
41	0xA0	10: Left-DAC output selects DAC_L2 path to left high-power output drivers.	10: Right-DAC output selects DAC_R2 path to right high-power output drivers.			
42	0x00	Default				
43	0x00	Default				
44	0x00	Default				
45	0x00	Default				
46	0x00	Default				
47	0x80	1: DAC_L1 is routed to HPLOUT.	DAC_L1 to HPLOUT Analog Volume Control: 0000000 = 0dB			
48	0x00	Default				
49	0x00	Default				
50	0x00	Default				

Register #	Value	Configuration				
51	0x97	HPLOUT Output Level Control 1001: Output level control = 9 dB	1: HPLOUT is high-impedance when powered down.	1: All programmed gains to HPLOUT have been applied.	1: HPLOUT is fully powered up.	
52	0x00	Default				
53	0x00	Default				
54	0x00	Default				
55	0x00	Default				
56	0x00	Default				
57	0x00	Default				
58	0x70	HPLCOM Output Level Control = 0111 : Output level control = 7dB	0: HPLCOM is muted.	0: HPLCOM is weakly driven to a common mode when powered down.	0: Not all programmed gains to HPLCOM have been applied yet.	
59	0x00	Default				
60	0x00	Default				
61	0x00	Default				
62	0x00	Default				
63	0x00	Default				
64	0x80	1: DAC_R1 is routed to HPROUT.	DAC_R1 to HPROUT Analog Volume Control: 0000000 = 0dB			
65	0x0F	HPROUT Output Level Control 0000: Output level control = 0 dB	1: HPROUT is not muted.	1: HPROUT is high-impedance when powered down.	1: All programmed gains to HPROUT have been applied.	1: HPROUT is fully powered up.
66	0x00	Default				
67	0x00	Default				
68	0x00	Default				
69	0x00	Default				
70	0x00	Default				
71	0x00	Default				
72	0x97	HPRCOM Output Level Control 1001: Output level control = 9 dB	1: HPRCOM is high-impedance when powered down.	1: All programmed gains to HPRCOM have been applied.	1: HPRCOM is fully powered up.	
73	0x00	Default				
74	0x00	Default				
75	0x00	Default				
76	0x00	Default				
77	0x00	Default				
78	0x00	Default				
79	0x00	Default				
80	0x00	Default				

Register #	Value	Configuration				
81	0x00	Default				
82	0x00	Default				
83	0x00	Default				
84	0x00	Default				
85	0x00	Default				
86	0x9B	LEFT_LOP/M Output Level Control 1001: Output level control = 9 dB	0: LEFT_LOP/M is muted.	1: All programmed gains to LEFT_LOP/M have been applied.	0: LEFT_LOP/M is not fully powered up.	
87	0x00	Default				
88	0x00	Default				
89	0x00	Default				
90	0x00	Default				
91	0x00	Default				
92	0x80	1: DAC_R1 is routed to RIGHT_LOP/M.	DAC_R1 to RIGHT_LOP/M Analog Volume Control = 0 dB			
93	0x9B	RIGHT_LOP/M Output Level Control 1001: Output level control = 9 dB	0: RIGHT_LOP/M is muted.	1: All programmed gains to RIGHT_LOP/M have been applied.	0: RIGHT_LOP/M is not fully powered up.	
94	0xC6	1: Left DAC is fully powered up.	1: Right DAC is fully powered up.	1: HPLOUT Driver is fully powered up.	1: HPROUT Driver is fully powered up.	
95	0x0C	1: HPLCOM is fully powered up.	1: HPRCOM is fully powered up.			
96	0x00	Default				
97	0x00	Default				
98	0x00	Default				
99	0x00	Default				
100	0x00	Default				
101	0x00	Default				
102	0xA2	10: CLKDIV_IN uses BCLK.	10: PLLCLK_IN uses BCLK.			
103	0x00	Default				
104	0x00	Default				
105	0x00	Default				
106	0x00	Default				
107	0x00	Default				
108	0x33	1: Signal is routed by a switch to RIGHT_LOM.	1: Signal is routed by a switch to RIGHT_LOP.	1: Signal is routed by a switch to LEFT_LOM.	1: Signal is routed by a switch to LEFT_LOP.	
109	0xC0	11: 100% increase in DAC reference current				

Register #	Value	Configuration				
110	0x00	Default				
111	0x00	Default				
112	0x00	Default				
113	0x00	Default				
114	0x00	Default				
115	0x00	Default				
116	0x00	Default				
117	0x00	Default				
118	0x00	Default				
119	0x00	Default				
120	0x00	Default				
121	0x00	Default				
122	0x00	Default				
123	0x00	Default				
124	0x00	Default				
125	0x00	Default				
126	0x00	Default				
127	0x00	Default				