I was going through the DAC3203 electrical specs and noticed that it doesn't list the PDM timing information. So I referred to the specification in the AIC3204 datasheet. Is the PDM block specs in DAC3203 similar to the one in AIC3204?

Also would like to get some clarification on some of the parameters to check on my understanding. The clock rise/fall time listed here in the AIC3204 spec sheet refers to the clock simulated performance from the codec pinout. So we would expect degradation that may go beyond the 4ns listed timing with extra capacitance coming from the PCB parasitics. Is this statement true?

7.16 Digital Microphone PDM Timing (see Figure 5)

Based on design simulation. Not tested in actual silicon.

		IOVDD = 1.8V		IOVDD = 3.3V		UNIT
		MIN	MAX	MIN	MAX	
t_s	DIN setup	20		20		ns
t_h	DIN hold	5		5		ns
t_r	CLK rise time		4		4	ns
t_f	CLK fall time		4		4	ns

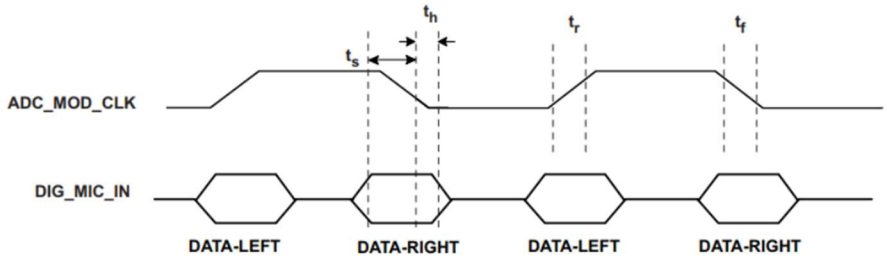

Figure 5. PDM Input Timing